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Chapter 1. Target Devices

"CubeSuite+ Simulator for V850E2 supporting OS Timer" supports both simulation of V850E2 CPU core and simulation of timer for real time operating system (OS Timer).

Below is a list of devices supported by this simulator.

Nickname	Device name
V850E2/Mx4	μPD70F3510, μPD70F3512
V850E2/Dx4	μPD70F3524, μPD70F3525, μPD70F3526, μPD70F3532, μPD70F3535, μPD70F3536, μPD70F3537
V850E2/Fx4	μPD70F3548, μPD70F3549, μPD70F3550, μPD70F3551, μPD70F3552, μPD70F3553, μPD70F3554, μPD70F3555, μPD70F3556, μPD70F3557, μPD70F3558, μPD70F3559, μPD70F3560, μPD70F4000, μPD70F4001, μPD70F4002, μPD70F4003, μPD70F4004, μPD70F4005, μPD70F4006, μPD70F4007, μPD70F4008, μPD70F4009, μPD70F4010, μPD70F4011, μPD70F4012
V850E2/Px4	μPD70F3502, μPD70F3503, μPD70F3504, μPD70F3505, μPD70F3506, μPD70F3507, μPD70F3508, μPD70F3509

Chapter 2. User's Manuals

Please read the following user's manuals together with this document.

Manual Name	Document Number
CubeSuite+ Ver.1.00.00 V850 Debug	R20UT0562EJ0100
CubeSuite+ Ver.1.00.00 Message	R20UT0407EJ0100

Chapter 3. Key Word for Uninstallation

To uninstall this product, use the integrated uninstaller (uninstalls CubeSuite+).

Chapter 4. Cautions

This section describes cautions for using the V850E2 supporting OS Timer simulator. The following two types of caution are described.

- Cautions for CPU core function
- Cautions for OS Timer

4.1 Cautions for CPU core function

4.1.1 CPU function

The simulator supports as following functions. Other functions are not supported.

- CPU instruction
- Exceptions
- System register protection
- Memory protection
- Timing supervision function
- Floating-point operation function

4.1.2 External memory bus

The access to external memory area is not supported.

4.1.3 Floating-point unit

A simulation result of the floating-point unit [FPU] has a margin of errors compared to real devices. The simulator uses the floating-point library of Visual C++, and store a result calculated by 80bit in a register.

4.1.4 Exceptions

Following exception is not supported.

System error exception, Memory error exception, Coprocessor unusable exception

4.1.5 Cache memory

The simulation of cache memory is not supported.

4.1.6 Instructions

The instructions (SYNCE/SYNCM/SYNCP) are not supported. If these were executed, the operation is same as NOP execution.

4.1.7 CPU operation clock

The operation clock of CPU is always 4MHz. The setting of main clock on property panel is ignored.

4.1.8 Data flash

It is impossible to use data flash area. If CPU accesses this area, CPU breaks and error is happen.

4.1.9 Option byte storage register

The value of Option byte storage register "OPBT" is always "0".

4.2 Cautions for OS Timer

4.2.1 P-bus peripheral I/O registers

The simulator supports following P-bus peripheral I/O registers for OS timer.

Nickname	P-bus peripheral I/O registers
V850E2/Mx4	ICOSTM0, IMR0, OSTM0CTL, OSTM0CMP, OSTM0CNT, OSTM0TE, OSTM0TS,OSTM0TT
V850E2/Dx4	ICOSTM0, IMR9, OSTM0CTL, OSTM0CMP, OSTM0CNT, OSTM0TE, OSTM0TS,OSTM0TT
V850E2/Fx4	ICOSTM0, IMR9, OSTM0CTL, OSTM0CMP, OSTM0CNT, OSTM0TE, OSTM0TS,OSTM0TT
V850E2/Px4	ICOSTM0, ICOSTM1, IMR2, OSTM0CTL, OSTM1CTL, OSTM0CMP, OSTM1CMP, OSTM0CNT, OSTM1CNT, OSTM0TE, OSTM1TE, OSTM0TS, OSTM1TS, OSTM0TT, OSTM1TT

4.2.2 The count clock of OS Timer

The count clock of OS Timer is always 4MHz.

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