CS+ Instruction Simulator for RH850 V5.00.00

Release Note

R20UT4550EJ0100
Rev.1.00
Jun.10.19

Thank you for using the CS+ integrated development environment.

This document describes restrictions on and points for caution regarding the simulator. Read this document before using the product.

Contents

Chapter 1. Target Devices

The simulator allows the simulation of instructions for the following RH850 CPU cores: RH850G4MH, RH850G3M, RH850G3MH, RH850G3K, and RH850G3KH.
The target devices the CS+ IDE supports are listed on the Web site.
Please see the URL below.

CS+ Product Page
http://www.renesas.com/cs+

Chapter 2. User's Manuals

Please read the following user's manuals together with this document.

Manual Name	Document Number
CS+ V8.02.00 Integrated Development Environment User's Manual: RH850 Debug Tool	R20UT4529EJ0100
CS+ V8.02.00 Integrated Development Environment User's Manual: Message	R20UT4533EJ0100

Chapter 3. Keyword for Uninstallation

To uninstall this product, use the integrated uninstaller (uninstalls CS+). There are two ways to uninstall CS+.

- Use the integrated uninstaller from Renesas (uninstalls all CS+ components)
- Use the Windows uninstaller (only uninstalls this product)

To use the Windows uninstaller, select the following from the Control panel:

- Programs and Features

Then select [CS+ for CC].

Chapter 4. Points for Caution

This chapter describes points you will need to note when you are using the instruction simulator for RH850.
For details, refer to section 2.3.3, [Simulator], in the CS+ V8.02.00 Integrated Development Environment User's Manual: RH850 Debug Tool.

4.1 CPU Operating Clock

The CPU clock operates at the frequency set up with the property "Main clock frequency [MHz]" of the RH850 simulator.

4.2 Access Latency

Since the latency of access to the various types of memory and peripheral modules is not considered, the execution times (numbers of cycles) will be different from those for the actual device.
Thus, the results of measuring the following items differ according to whether the instruction simulator or an actual device is in use.

- The results of measurement by the Run-Break timer
- The results of measurement of Timer Result events
- The [Pipeline] area of the Trace panel
- The [Time] area of the Trace panel
- Result of tracing when the trace target is selected as [All core] (timing between processor elements)
- Timestamps of the software trace data

4.3 Peripheral Functions

The instruction simulator for RH850 does not support simulation of the peripheral functions.

Chapter 5. Restrictions

This chapter describes restrictions on the use of the instruction simulator for RH850.

5.1 Simulation of the HALT Instruction

[Affected device] RH850G4MH

[Details] Execution of the HALT instruction is not reflected in the results of tracing. However, the results of tracing in the processor elements for which the HALT instruction was not executed are not affected.

[Workaround] There is no workaround.

[Schedule for fixing the problem] We will fix this problem in the next and subsequent versions.

5.2 Trace Data Acquired from Current Addresses when Interrupts Occurred

[Affected device] RH850G4MH

[Details] Acquired trace data may not correctly indicate the instruction (disassembled code) at an address that was current when an interrupt occurred. Specifically, the values of the following items may not be correct.

- The instruction (disassembled code) displayed in the [Source / Disassemble] area of the Trace panel
- The member variable *Mnemonic* of class *TraceInfo*, an object of which is acquired by executing the *debugger.Trace.Get* or *debugger.XTrace.Dump* function in the Python console

Note, however, that this phenomenon does not affect the normal execution of programs.

[Workaround] There is no workaround.

[Schedule for fixing the problem] We will fix this problem in the next and subsequent versions.

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