ClockMatrix Firmware Version v4.9.6

Contents

1. Overview

This document describes changes in the functionality and register map between firmware version 4.9.6 and version 4.9.5.

Table 1. Related Documents

Document Title	Document Description
Device Datasheet	Contains a functional overview of a specific device and hardware design related details including pinouts, AC and DC specifications, and applications information related to power filtering and terminations.
8A3xxx Family Programming Guide v4.9 dated Apr 6, 2023	Contains detailed register descriptions and address maps for all members of the family of devices. All devices use some subset of this register map.

2. Firmware Version Number

The firmware version can be read from the GENERAL_STATUS registers as shown in the following table.

Register Module Base Address: C014h			Firmware Version v4.9.5	Firmware Version v4.9.6
Offset Address (Hex)	**Individual Register Name**	**Register Description**	**Default Value**	**Default Value**
010h	GENERAL_STATUS.MAJ_REL	Major release number	09h	09h
011h	GENERAL_STATUS.MIN_REL	Minor release number	09h	09h
012h	GENERAL_STATUS.HOTFIX_REL	Hotfix release number	05h	06h

3. Firmware Version 4.9.6 Functions Added Since Version 4.9.5

Issue Number	Description of Function
BRMBXR-3605 BRMBXR-3653 BRMBXR-3663 BRMBXR-3635 BRMBXR-3642 BRMBXR-3654 BRMBXR-3657 BRMBXR-3658 BRMBXR-3659 BRMBXR-3661 BRMBXR-3669	Added function to align 8kHz via PWM sync.

4. Improvements in Version 4.9.6 Added Since Version 4.9.5

Issue Number: BRMBXR-3639

Firmware	Functional Difference
v4.9.5	The DPLL_PHASE_PULL_IN function uses the configured DPLL_PHASE_PULL_IN_ OFFSET, and DPLL_PHASE_PULL_IN_SLOPE_LIMIT to estimate the time duration required for a frequency offset to achieve the desired phase pull-in.
v4.9.6	The accuracy of the estimated time duration is improved vs v4.9.5 so that the residual phase error after a pull-in completes is reduced.

Issue Number: BRMBXR-3650

Firmware	Functional Difference
v4.9.5	When a ClockMatrix device is configured with a satellite channel it implements an auto-alignment algorithm that uses the output time-to-digital converters (TDC) to align the satellite channel output clock with the source channel output clock. The auto-alignment algorithm applies temporary frequency offsets to the satellite channel output clock to accomplish phase adjustments.
v4.9.6	For v4.9.6, the minimum duration of the temporary frequency offsets is increased from 50ms to 100ms so that the magnitude of temporary frequency offsets for small phase adjustments is reduced versus v4.9.5.

Issue Number: BRMBXR-3673

Firmware	Functional Difference
v4.9.5	When PWM_OUTPUT_SQUELCH is enabled for a PWM_SYNC_DECODER then, if the squelch criteria are met, the outputs of the destination payload channel will be squelched.
v4.9.6	When PWM_OUTPUT_SQUELCH is enabled for a PWM_SYNC_DECODER then, if the squelch criteria are met, the outputs of the destination payload channel will be squelched, unless the destination payload channel DPLL is locked to an input reference.

5. Register Differences Between Version 4.9.6 and Version 4.9.5

Register Module Base Address: C014h		
Offset Address (Hex)	**Individual Register Name**	**Change**
012h	GENERAL_STATUS. HOTFIX_REL	Default value is 6.

6. Revision History

Revision	Date	Description
1.00	Sep 7, 2023	Initial release.

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