

## Applilet3 for RL78 V1.14.00

### **Release Note**

Thank you for using the Applilet3 for RL78.

This document describes the restrictions and points for caution. Read this document before using the product.

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# Chapter 1. Introduction

Applilet3 for RL78 is a software tool to generate control programs (device driver programs) for peripheral modules (timers, UART, A/D, etc.). It generates device driver codes using user settings through GUI. Initialize code and API (Application Programming Interface) functions are provided.



# Chapter 2. Target Devices

PIN		Device name		
20pin	R5F1076C	R5F1076C		
30pin	R5F107AC, R5F107AE	R5F107AC, R5F107AE		
32pin	R5F107BC	R5F107BC		
38pin	R5F107DE			
The Applilet3 is based on the following documents.				
I	Manual Name	Document Number		
RL78/I1A User's Manual: Hardware		R01UH0169JJ0210 Rev.2.10		
		R01UH0169EJ0210 Rev.2.10		

Below is a list of d	levices supported by the Applilet	3 for RL78/G12 V2.04.01.04	
PIN		Device name	
20pin	R5F10266, R5F10267, R5F10268, R5F10269, R5F1026A R5F10366, R5F10367, R5F10368, R5F10369, R5F1036A		
24pin	R5F10277, R5F10278, R5F10279, R5F1027A R5F10377, R5F10378, R5F10379, R5F1037A		
30pin	R5F102A7, R5F102A8, R5F102A9, R5F102AA R5F103A7, R5F103A8, R5F103A9, R5F103AA		
The Applilet3 is ba	ased on the following documents	S.	
Manual Name		Document Number	
RL78/G12 User's Manual: Hardware		R01UH0200JJ0200 Rev.2.10	
		R01UH0200EJ0200 Rev.2.10	



PIN	Device name		
	R5F1006A, R5F1006C, R5	F1006D, R5F1006E	
20pin	R5F1016A, R5F1016C, R5		
<b>2</b> 4 ·	R5F1007A, R5F1007C, R5	F1007D, R5F1007E	
24pin	R5F1017A, R5F1017C, R5	F1017D, R5F1017E	
25 nin	R5F1008A, R5F1008C, R5		
25pin	R5F1018A, R5F1018C, R5	F1018D, R5F1018E	
20nin	R5F100AA, R5F100AC, R5	F100AD, R5F100AE, R5F100AF, R5F100AG	
30pin	R5F101AA, R5F101AC, R5	F101AD, R5F101AE, R5F101AF, R5F101AG	
00 i	R5F100BA, R5F100BC, R5	F100BD, R5F100BE, R5F100BF, R5F100BG	
32pin	R5F101BA, R5F101BC, R5	F101BD, R5F101BE, R5F101BF, R5F101BG	
	R5F100CA, R5F100CC, R5	5F100CD, R5F100CE, R5F100CF, R5F100CG	
36pin	R5F101CA, R5F101CC, R5	5F101CD, R5F101CE, R5F101CF, R5F101CG	
	R5F100EA, R5F100EC, R5	F100ED, R5F100EE, R5F100EF, R5F100EG, R5F100EH	
40pin	R5F101EA, R5F101EC, R5	F101ED, R5F101EE, R5F101EF, R5F101EG, R5F101EH	
	R5F100FA, R5F100FC, R5F100FD, R5F100FE, R5F100FF, R5F100FG, R5F100FH		
4.4	R5F100FJ, R5F100FK, R5F100FL		
44pin	R5F101FA, R5F101FC, R5F101FD, R5F101FE, R5F101FF, R5F101FG, R5F101FH		
	R5F101FJ, R5F101FK, R5F101FL		
	R5F100GA, R5F100GC, R5F100GD, R5F100GE, R5F100GF, R5F100GG, R5F100GH		
48pin	R5F100GJ, R5F100GK, R5F100GL		
торії	R5F101GA, R5F101GC, R5F101GD, R5F101GE, R5F101GF, R5F101GG, R5F101GH		
	R5F101GJ, R5F101GK, R5		
		F100JE, R5F100JF, R5F100JG, R5F100JH	
52pin	R5F100JJ, R5F100JK, R5F100JL		
	R5F101JC, R5F101JD, R5F101JE, R5F101JF, R5F101JG, R5F101JH		
	R5F101JJ, R5F101JK, R5F101JL		
	R5F100LC, R5F100LD, R5F100LE, R5F100LF, R5F100LG, R5F100LH		
64pin	R5F100LJ, R5F100LK, R5F100LL		
	R5F101LC, R5F101LD, R5F101LE, R5F101LF, R5F101LG, R5F101LH R5F101LJ, R5F101LK, R5F101LL		
80pin	R5F100MF, R5F100MG, R5F100MH, R5F100MJ, R5F100MK, R5F100ML R5F101MF, R5F101MG, R5F101MH, R5F101MJ, R5F101MK, R5F101ML		
	R5F100PF, R5F100PG, R5F100PH, R5F100PJ, R5F100PK, R5F100PL		
100pin	R5F101PF, R5F101PG, R5F101PH, R5F101PJ, R5F101PK, R5F101PL		
	R5F100SH, R5F100SJ, R5F100SK, R5F100SL		
128pin	R5F101SH, R5F101SJ, R5F101SK, R5F101SL		
e Applilet3 is ba	sed on the following documents		
Ν	lanual Name	Document Number	
	· · · · · · · · ·	R01UH0146JJ0330 Rev.3.30	
RL78/G13 User's Manual: Hardware		R01UH0146EJ0330 Rev.3.30	



Below is a list of c	levices supported by the Appl	ilet3 for RL78/G14 V2.05.01.05		
PIN	Device name			
30pin	R5F104AA, R5F104AC,	R5F104AA, R5F104AC, R5F104AD, R5F104AE, R5F104AF, R5F104AG		
32pin	R5F104BA, R5F104BC,	R5F104BA, R5F104BC, R5F104BD, R5F104BE, R5F104BF, R5F104BG		
36pin	R5F104CA, R5F104CC,	R5F104CD, R5F104CE, R5F104CF, R5F104CG		
40pin	R5F104EA, R5F104EC,	R5F104ED, R5F104EE, R5F104EF, R5F104EG, R5F104EH		
44pip	R5F104FA, R5F104FC, R5F104FD, R5F104FE, R5F104FF, R5F104FG, R5F104FH			
44pin	R5F104FJ	R5F104FJ		
19pip	R5F104GA, R5F104GC, R5F104GD, R5F104GE, R5F104GF, R5F104GG, R5F104GH			
48pin	R5F104GJ, R5F104GK, R5F104GL			
EQuin	R5F104JC, R5F104JD, R5F104JE, R5F104JF, R5F104JG, R5F104JH			
52pin	R5F104JJ, R5F104JK, R5F104JL			
64pip	R5F104LC, R5F104LD, F	R5F104LC, R5F104LD, R5F104LE, R5F104LF, R5F104LG, R5F104LH		
64pin	R5F104LJ, R5F104LK, R5F104LL			
80pin	R5F104MF, R5F104MG,	R5F104MF, R5F104MG, R5F104MH, R5F104MJ		
100pin	R5F104PF, R5F104PG, R5F104PH, R5F104PJ			
The Applilet3 is b	ased on the following docume	nts.		
Manual Name Document Number				
RI 78/G14 I	Jser's Manual: Hardware	R01UH0186JJ0330 Rev.3.30		
		R01UH0186EJ0330 Rev.3.30		

Below is a list of devices supported by the Applilet3 for RL78/G1A V2.04.01.02			
PIN	Device name		
25pin	R5F10E8A, R5F10E8C, R5F10E8D, R5F10E8E		
32pin	R5F10EBA, R5F10EBC, R5F10EBD, R5F10EBE		
48pin	R5F10EGA, R5F10EGC, R5F10EGD, R5F10EGE		
64pin	R5F10ELC, R5F10ELD, R5F10ELE		
The Applilet3 is based on the following documents.			
Manual Name Document Number			
RL78/G1A Use	er's Manual: Hardware	R01UH0305JJ0200 Rev.2.00	
		R01UH0305EJ0200 Rev.2.00	



Below is a list of devices supported by the Applilet3 for RL78/F12 V2.04.01.06			
PIN	Device name		
20pin	R5F1096E, R5F1096D, R5F1096C, R5F1096B, R5F1096A, R5F10968		
30pin	R5F109AE, R5F109AD, R5F109AC, R5F109AB, R5F109AA		
32pin	R5F109BE, R5F109BD, R5F109BC, R5F109BB, R5F109BA		
48pin	R5F109GE, R5F109GD, R5F109GC, R5F109GB, R5F109GA		
64pin	R5F109LE, R5F109LD, R5F109LC, R5F109LB, R5F109LA		
The Applilet3 is based on the following documents.			
Manual Name		Document Number	
RL78/F12 Use	er's Manual: Hardware	R01UH0231JJ0111 Rev.1.11	
		R01UH0231EJ0111 Rev.1.11	

Below is a list of devices supported by the Applilet3 for RL78/L12 V2.04.01.02			
PIN	Device name		
32pin	R5F10RBC, R5F10RBA, R5F10RB8		
44pin	R5F10RFC, R5F10RFA, R5F10RF8		
48pin	R5F10RGC, R5F10RGA, R5F10RG8		
52pin	R5F10RJC, R5F10RJA, R5F10RJ8		
64pin	R5F10RLC, R5F10RLA		
The Applilet3 is based on the following documents			
Ма	nual Name	Document Number	
RL78/L12 User's Manual: Hardware		R01UH0330JJ0200 Rev.2.00	
		R01UH0330EJ0200 Rev.2.00	



Below is a list of devices supported by the Applilet3 for RL78/D1A V2.04.01.02			
PIN	Device name		
48pin	R5F10CGB, R5F10CGC, R5F10DGC, R5F10DGD, R5F10DGE		
64pin	R5F10CLD, R5F10DLD, R5F10DLE		
80pin	R5F10CMD, R5F10CME R5F10DMD, R5F10DME, R5F10DMF, R5F10DMG, R5F10DMJ		
100pin	R5F10DPE, R5F10DPF, R5F10DPG, R5F10DPJ, R5F10TPJ		
Applilet3 for RL78_D1A is based on the following documents			
Manual Name Document Number			
RL78/D1A User's Manual: Hardware		R01UH0317EJ0003 Rev.0.03	

Below is a list of devices supported by the Applilet3 for RL78/F13 V2.03.01.06				
PIN		Device name		
20pin	R5F10A6A, R5F10A6C, R5	R5F10A6A, R5F10A6C, R5F10A6D, R5F10A6E		
30pin	, , ,	R5F10AAA, R5F10AAC, R5F10AAD, R5F10AAE R5F10BAC, R5F10BAD, R5F10BAE, R5F10BAF, R5F10BAG		
32pin	, , ,	R5F10ABA, R5F10ABC, R5F10ABD, R5F10ABE R5F10BBC, R5F10BBD, R5F10BBE, R5F10BBF, R5F10BBG		
48pin		R5F10AGA, R5F10AGC, R5F10AGD, R5F10AGE, R5F10AGF, R5F10AGG R5F10BGC, R5F10BGD, R5F10BGE, R5F10BGF, R5F10BGG		
64pin	R5F10BLC, R5F10ALD, R5F10ALE, R5F10ALF, R5F10ALG R5F10BLC, R5F10BLD, R5F10BLE, R5F10BLF, R5F10BLG			
80pin	R5F10AME, R5F10AMF, R5F10AMG R5F10BME, R5F10BMF, R5F10BMG			
The Applilet3 is ba	ased on the following documents	5.		
Manual Name Document Number				
RL78/F13,F14 User's Manual: Hardware		R01UH0368JJ0210 Rev.2.10		
		R01UH0368EJ0210 Rev.2.10		



Below is a list of devices supported by the Applilet3 for RL78/F14 V2.03.01.06			
PIN	Device name		
30pin	R5F10PAD, R5F10PAE		
32pin	R5F10PBD, R5F10PBE		
48pin	R5F10PGD, R5F10PGE, R5F10PGF, R5F10PGG, R5F10PGH, R5F10PGJ		
64pin	R5F10PLE, R5F10PLF, R5F10PLG, R5F10PLH, R5F10PLJ		
80pin	R5F10PME, R5F10PMF, R5F10PMG, R5F10PMH, R5F10PMJ		
100pin	R5F10PPE, R5F10PPF, R5F10PPG, R5F10PPH, R5F10PPJ		
The Applilet3 is based on the following documents.			
Manual Name Document Number			
R01UH0368JJ0210 Rev.2.10 RL78/F13,F14 User's Manual: Hardware			
		R01UH0368EJ0210 Rev.2.10	

Below is a list of devices supported by the Applilet3 for RL78/F15 V1.01.01.01						
PIN		Device name				
48pin	R5F113GL, R5F113GK	5F113GL, R5F113GK				
64pin	R5F113LL, R5F113LK	5F113LL, R5F113LK				
80pin	R5F113ML, R5F113MK	R5F113ML, R5F113MK				
100pin	R5F113PL, R5F113PK, R5	R5F113PL, R5F113PK, R5F113PJ, R5F113PH, R5F113PG				
144pin	R5F113TL, R5F113TK, R5F113TJ, R5F113TH, R5F113TG					
The Code Generator	The Code Generator is based on the following documents					
Manual Name		Document Number				
RL78/F15 Use	er's Manual: Hardware	R01UH0559JJ0090 Rev.0.90				
		R01UH0559EJ0090 Rev.0.90				



# Chapter 3. Operating Environment

#### Host machine

- IBM PC/AT compatibles (Windows® 10, Windows® 8.1, Windows® 7)
- Processor: 1 GHz or higher (must support hyper-threading, multi-core CPUs)
- Memory capacity: 2 GB or more recommended. Minimum requirement is 1 GB or more (64-
- bit Windows requires 2 G or more)
  - Hard disk capacity: 200 MB or more spare capacity
  - Display: 1024 x 768 or higher resolution, 65,536 or more colors
  - All other necessary software environments in addition to WindowsOS
  - .NET Framework version4.5

#### Development Environments

Product Name	Version
IAR Embedded Workbench for Renesas RL78	V2.21 or later
GNURL78	V15.02 or later
Renesas Electronics Compiler for 78K0R [CA78K0R]	V1.72 or later
Renesas Electronics Compiler for RL78 [CC-RL]	V1.05 or later



## Chapter 4. Changes

This chapter describes change to the Applilet3 for RL78 V1.14.00.

						Ve	rsior	า *1				
No	Description	RL78/F15	RL78/F14	RL78/F13	RL78/L12	RL78/F12	RL78/G1A	RL78/G12	RL78/G13	RL78/G14	RL78/I1A	RL78/D1A
		V1.01.01.01	V2.03.01.06	V2.03.01.06	V2.04.01.02	V2.04.01.06	V2.04.01.02	V2.04.01.04	V2.05.00.06	V2.05.01.05	V2.04.01.03	V2.04.01.02
1	The latest device user's manual is supported	/	0	0	/	0	/	0	0	0	/	/

•: Applicable, /: Not Applicable

Note 1: Version is described in the generated code.

## 4.1 Details of Changes

#### 4.1.1 The latest device user's manual is supported

The contents of the currently-issued Device User's Manual has been reflected in the tool as the design materials of the code generator.



# Chapter 5. Points for Caution

This section describes the cautions on the Applilet3 for RL78 V1.14.00.

## 5.1 List of Cautions

	Version *1										
Description		RL78/F14	RL78/F13	RL78/L12	RL78/F12	RL78/G1A	RL78/G12	RL78/G13	RL78/G14	RL78/11A	RL78/D1A
	V1.01.00.01	V2.03.00.02	V2.03.00.02	V2.04.00.01	V2.04.00.02	V2.04.00.02	V2.04.00.02	V2.04.00.03	V2.05.00.03	V2.04.00.01	V2.04.00.02
Online Help	0	0	0	0	0	0	0	0	0	0	0
The coding rule of MISRA-C.	0	0	0	0	0	0	0	0	0	0	0
Restrictions of High-speed on-chip oscillator frequency select register	0	0	0	0	0	0	0	0	0	/	0
Restrictions of internal low-speed or internal high-speed oscillator trimming	0	0	0	0	0	0	0	0	0	0	0
Restriction of a serial array unit	/	/	/	/	/	/	/	/	/	0	/
Restrictions of Flash memory CRC operation function (high-speed CRC)	0	0	0	/	0	0	0	0	0	0	0
Restrictions of Port mode select register (PMS)	0	0	0	/	/	0	0	0	0	0	0
Restrictions of the LIN-bus function of UART	0	0	0	0	0	0	0	0	0	0	0
Restrictions of extension code, wakeup function and multimaster of serial interface IICA or IIC0	0	0	0	0	0	0	0	0	0	0	0
Restriction of CAN	0	0	0	/	/	/	/	/	/	/	/
Cautions of Safety Functions	0	0	0	0	0	0	0	0	0	0	0
Cautions when using a DTC function	0	0	/	/	/	/	/	/	0	/	/
Cautions of timer array unit input clock sauce	0	0	0	/	/	/	/	/	/	/	/
Fast Mode Plus setting in IICA slave	0	0	0	0	0	0	0	0	0	0	0
	The coding rule of MISRA-C. Restrictions of High-speed on-chip oscillator frequency select register Restrictions of internal low-speed or internal high-speed oscillator trimming Restriction of a serial array unit Restrictions of Flash memory CRC operation function (high-speed CRC) Restrictions of Port mode select register (PMS) Restrictions of the LIN-bus function of UART Restrictions of extension code, wakeup function and multimaster of serial interface IICA or IICO Restriction of CAN Cautions of Safety Functions Cautions when using a DTC function Cautions of timer array unit input clock sauce	Online Help       ○         The coding rule of MISRA-C.       ○         Restrictions of High-speed on-chip oscillator frequency select register       ○         Restrictions of internal low-speed or internal high-speed oscillator frequency select register       ○         Restrictions of a serial array unit       /         Restrictions of Flash memory CRC operation function (high-speed CRC)       ○         Restrictions of Port mode select register (PMS)       ○         Restrictions of the LIN-bus function of UART       ○         Restriction of CAN       ○         Cautions of Safety Functions       ○         Cautions of timer array unit input clock sauce       ○         Fast Mode Plus setting in IICA slave       ○	DescriptionY 2000Online Help0The coding rule of MISRA-C.0Restrictions of High-speed on-chip oscillator frequency select register0Restrictions of internal low-speed or internal high-speed oscillator trimming0Restrictions of a serial array unit1Restrictions of Flash memory CRC operation function (high-speed CRC)0Restrictions of Port mode select register (PMS)0Restrictions of extension code, wakeup function and multimaster of serial interface IICA or IICO0Restriction of Safety Functions00Cautions of Safety Functions00Cautions of timer array unit input clock sauce00Cautions of timer array unit input clock sauce00	DescriptionYY2 <t< td=""><td>DescriptionImage: Section of the section of CANImage: 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○: Applicable, -: Not Applicable, /: Outside of function.

Note 1: Version is described in the generated code.



## 5.2 Restrictions Details

#### 5.2.1 Online Help

Applilet3 is not supporting online help.

#### 5.2.2 Restrictions of the coding rule of MISRA-C

Compliance with the MISRA-C (Guidelines for the Use of the C Language in Vehicle Based Software) coding convention is not supported for source code output by the Applilet3.

#### 5.2.3 Restrictions of High-speed on-chip oscillator frequency select register

Applilet3 is not equivalent to a setup of high-speed on-chip oscillator frequency select register

#### 5.2.4 Restrictions of internal low-speed or internal high-speed oscillator trimming

Applilet3 is not equivalent to a setup of internal low-speed or internal high-speed oscillator trimming register.

#### 5.2.5 Restriction of a serial array unit

Applilet3 is not equivalent to a setup of single-wire UART mode and DMX512 communication.

#### 5.2.6 Restrictions of Flash memory CRC operation function (high-speed CRC)

Applilet3 does not correspond to a flash memory CRC operation function (high-speed CRC). Please refer to application note r01an0736ej. https://www.renesas.com/search/keyword-search.html#genre=document&g=r01an0736ej

#### 5.2.7 Restrictions of Port mode select register (PMS)

Applilet3 does not supporting a port mode select register (PMS).

#### 5.2.8 Restrictions of the LIN-bus function of UART

The Applilet3 is not supporting the LIN-bus functions of serial interface UART0, UART2, UART3, UART6 or UARTF.

# 5.2.9 Restrictions of extension code, wakeup function and multimaster of serial interface IICA or IIC0

The Applilet3 is not supporting the extension code, multimaster, wakeup function of serial interface IIC.

#### 5.2.10 Restriction of CAN

Applilet3 is not supporting CAN.

#### 5.2.11 Restriction of Safety functions

RAM parity error detection function of Safety Functions is not supported.



#### 5.2.12 Cautions when using a DTC function

When DTC is used, the following warning message is displayed and an object file is not generated. CC78K0R warning W0837: Output assembler source file , not object file

Workard	lhaur
IVVOIKard	Junai

Set up the following individual option of building.

🍄 Property 📲 Code Generator 🐹 Code Generator Preview 🔹 💌					
🗐 r_dtc.c Property					
🗆 Build					
Set as build-target	Yes				
Set individual compile option	Yes				
File type					
The type	C source				
Set individual compile option Selects whether to set a compile option that di	ffers from the project settings to this C source.				
Build Settings 🔏 Individual Compile Optio	ons 🖌 File Information 🖊 🛛 👻				
🔄 r_cg_dtab Property	<b>a ø</b> -+				
A Debug Information					
Add debug information	Yes(Add to both assembly and object file)(-g2)				
✓ Optimization					
Perform optimization	Yes(Standard)(-qx2)				
Preprocess     Additional include paths	Additional include paths[0]				
Additional include paths Use whole include paths specified for build tool	Yes				
<ul> <li>Macro definition</li> </ul>	Macro definition[0]				
Macro undefinition	Macro undefinition[0]				
Macro undefinition     Macro undefinition[U]     Macro undefinition[U]					
Extension					
Output File					
A Assembly File					
Output assembly file	No				
Data Control	Yes(With no C source info)(-a)				
⊳ List File	Yes(With C source into(unexpanded include file contents))(-sa)				
> Others	Yes(With C source info(expanded include file contents))(-sa,-li)				
Output assembly file Selects whether to output an assemble file. This option corresponds to the -a, -sa, and -li option					
Build Settings A Individual Compile Option	s File Information -				

#### 5.2.13 Cautions of timer array unit input clock sauce

When the clock sauce of a timer input is set as a RTC1HZ output by setup of a timer array unit, a setup about the output of the RTC1HZ terminal of a real-time clock becomes invalid. The code which outputs RTC1HZ then is not generated.

[Workaround] When you set to a RTC1HZ signal by setup of a timer array unit, please choose a setup which uses a real-time clock and add the code which outputs RTC1HZ.

#### 5.2.14 Fast Mode Plus setting in IICA slave

If the Fast Mode Plus is set when using the IICA slave, IICA Low level range setting register (IICWLn, n= channel number), and IICA High level range setting register (IICWHLn) are not set correctly.

[Workaround] There is no workaround.

After doing code generator, please rewrite the numerical value of the register setting of IICWLn, IICWHn in the R\_IICAn\_Create function. I depend on a system for the numerical value. Please change device UM to reference.



# Chapter 6. Correction History

This section describes correction history of RENESAS TOOL NEWS.

## 6.1 List of RENESAS TOOL NEWS

Issue Date	Document No.	Description	Device Concerned	Fixed version
Aug. 01, 2012	120801/tn8	Problems arising in Applilet3 for RL78/G13 and Applilet3 for RL78/G14	RL78/G13, RL78/G14	V1.00.00
Oct. 01, 2012	121001/tn1	With generating code that make setting of using Multiple PWM	RL78/D1A	V1.00.00
Feb. 01, 2013	130201/tn6	With making settings of RD timer in PWM mode	RL78/G14	V1.00.00
Feb. 01, 2013	130201/110	Making settings of RJ timer in pulse period measurement mode	RL78/G14	V1.00.00
Oct. 16, 2013	131016/tn4	With the key input interrupt setting	RL78/L12	V1.00.00
000. 10, 2010		With A/D converter operation setting	RL78/G1A	V1.00.00
	140416/tn8	With selecting the 20-pin, 30-pin, or 32-pin package for the RL78/F13 or RL78/F14 group	RL78/F13, RL78/F14	V1.00.00
Apr. 16, 2014		With using the remote control carrier wave mask signal in the RL78/L12 group	RL78/L12	V1.00.00
		With the case when ports that are not available in the MCU are displayed in the RL78/G14 group	RL78/G14	V1.00.00
Aug. 16, 2014	140816/tn6	With setting of port 1	RL78/G14	V1.06.00
Dec. 16, 2014	141216/tn5	3. Saving Projects with Settings for the A/D Convertor	RL78/L1C	V1.07.00
		1. Clock Generation Circuit (PLL Circuit Operation)	RL78/D1A, RL78/F13, RL78/F14	V1.10.00
Jul. 16, 2015	150716/tn2	2. Setting P40 of Port 4	RL78/D1A, RL78/F12, RL78/F13, RL78/F14, RL78/G12, RL78/G13, RL78/G14, RL78/G1A, RL78/I1A, RL78/I1A, RL78/L12	V1.10.00
		3. Code Generated for UART0 and UARTF	RL78/F12	V1.10.00



Issue Date	Document No.	Description	Device Concerned	Fixed version
		1. Indication of Channels of Serial Interface IICA	RL78/G14	V1.10.00
Nov. 16, 2015	151116/tn2	2. Procedure for Setting the PLL Clock	RL78/F13, RL78/F14, RL78/F15	V1.10.00
Jan. 16, 2016	160116/tn5	Transfer of data with a length of 10 or more bits through an element of a serial array unit configured as a CSI or data with a length of 16 bits through an element configured as a UART	RL78/F12, RL78/F13, RL78/F14, RL78/F15, RL78/D1A	V1.10.00
Feb. 16, 2016	2016 160216/tn5 1. Using the error interrupt of serial array un 4 as UART4 or DALI4		RL78/I1A	V1.10.00
		2. Using serial array unit 4 as DALI4	RL78/I1A	V1.10.00
Mar. 16, 2016	160316/tn1	Pin settings for the IICA serial interface when setting the PIOR to change the assignment of pin functions	RL78/G12	V1.10.00
Jun. 16, 2016	R20TS0038EJ 0100	Scan Mode of A/D Converter	RL78/F12, RL78/F13, RL78/F14, RL78/F15, RL78/G1A	V1.11.00
Mar. 4, 2047	R20TS0139EJ	1. Input of Ports P10 and P11	RL78/G13 (20/24/25pin product.)	V1.13.00
Mar. 1, 2017	0100	0100 2. Port Settings Related to Reset Processing	RL78/F12 (20pin product)	V1.13.00



## 6.2 Details of RENESAS TOOL NEWS

#### 6.2.1 RENESAS TOOL NEWS Document No.120801/tn8

This issue has been corrected in Applilet3 for RL78 V1.00.00.

#### (1) In Applilet3 for RL78/G13 V1.03.01

a. If code is generated so that timers TAUx (x is 1 to 7) of an 80-, 100-, or 128-pin MCU can output square waves, the values of the TOM1 and TOL1 registers, which control TAUx, are not set but those of the TOM0 and TOL0 registers are set.

b. If you make settings of ports, the TTL checkboxes for the P10 and P11 pins are not displayed.

(2) In Applilet3 for RL78/G14 V1.01.01

a. In the code for setting registers PIOR01 and PIOR04 to 1s in an arrangement of pin assignments, incorrect pins are assigned to INTP10 and INTP11 as follows:

Incorrect:	Correct:
P110 assigned to INTP10	P100 assigned to INTP10
P111 assigned to INTP11	P110 assigned to INTP11

b. If code is generated in an 80- or 100-pin MCU, no functions except "interval" can be selected in the functional selection of timer TAU1.

c. If the code is generated for making settings of UART2 and any of the ports except 13 and 14, an error arises in building it.

d. In the settings of DTC, the following error is found in the pulldown list of source and destination addresses of data transfer:

Erroneous statement: Address decremented It must be read as Address incremented

For details of the problem, refer to the URL below. https://www.renesas.com/doc/toolnews/eng/2012/120801tn8 e.pdf

#### 6.2.2 RENESAS TOOL NEWS Document No.121001/tn1

This issue has been corrected in Applilet3 for RL78 V1.00.00.

• With generating code that make setting of using Multiple PWM

If the code is generated for making setting of using Multiple PWM on the TAU2 register in timer array unit 2, data is output on undefined channels in error.

For details of the problem, refer to the URL below. https://www.renesas.com/doc/toolnews/eng/2012/121001tn1\_e.pdf



#### 6.2.3 RENESAS TOOL NEWS Document No.130201/tn6

This issue has been corrected in Applilet3 for RL78 V1.00.00.

• With making settings of RD timer in PWM mode

(1) With generating incorrect code for cyclic register

If you select PWM from among the operating modes of the RD timer and 64 MHz from among the clock frequencies of the high-speed on-chip oscillator, the code generator generates incorrect code; that is, the value (duty ratio) of the cyclic register is erroneous. (2) With using alternate-function pins

When the PWM mode is used, every pin for the PWM output, which is an alternate-function pin, cannot be used for the other function. So if you make settings for using these pins for the other functions than PWM, Applilet express an alarm (symbol "!"). However, if you have selected the PWM mode in the RD timer, this alarm is not expressed on the information setting area of the [Port].

· Making settings of RJ timer in pulse period measurement mode

If you select the Pulse Period Measurement Mode from among the operating modes of the RJ timer, the code generator generates erroneous code.

For details of the problem, refer to the URL below. https://www.renesas.com/doc/toolnews/eng/2013/130201tn6 e.pdf

#### 6.2.4 RENESAS TOOL NEWS Document No.131016/tn3

This issue has been corrected in Applilet3 for RL78 V1.00.00.

· When the timer KB20 is in Use

When the timer KB20 is in use, the settings for Standalone mode (period controlled by external trigger input) and Interleave PFC (power factor correction) output mode may prevent the correct output of the API functions.

For details of the problem, refer to the URL below. https://www.renesas.com/doc/toolnews/eng/2013/131016tn3\_e.pdf



#### 6.2.5 RENESAS TOOL NEWS Document No.131016/tn4

This issue has been corrected in Applilet3 for RL78 V1.00.00.

• With the key input interrupt setting (RL78/L12 Group)

The setting of Key interrupt flag and Detection edge may not be saved. When saving the project after making the new setting and then reloading the project, the setting reverts to the original setting as the new one had not been saved.

• With A/D converter operation setting (RL78/G1A Group)

The Conversion time mode of the Conversion time setting may not be saved. When saving the project after making the new setting and then reloading the project, the setting reverts to the original setting as the new one had not been saved.

For details of the problem, refer to the URL below. https://www.renesas.com/doc/toolnews/eng/2013/131016tn4 e.pdf

#### 6.2.6 RENESAS TOOL NEWS Document No.140416/tn8

This issue has been corrected in Applilet3 for RL78 V1.00.00.

· With selecting the 20-pin, 30-pin, or 32-pin package for the RL78/F13 or RL78/F14 group

When the 20-pin, 30-pin, or 32-pin package is selected for the RL78/F13 or RL78/F14 group and a divided frequency is selected for CPU and peripheral clock (fCLK) in the clock generator settings, the register settings are not output.

· With using the remote control carrier wave mask signal in the RL78/L12 group

There is an error in the R\_TAU0\_Channel2\_Stop function for output when PWM output (remote control carrier wave mask signal) is selected in timer channel 2.

• With the case when ports that are not available in the MCU are displayed in the RL78/G14 group

When an RL78/G14 group MCU in the 80-pin package is selected, the settings for the P80 and P81 ports, which are not available in the selected MCU, are displayed.

For details of the problem, refer to the URL below. https://www.renesas.com/doc/toolnews/eng/2014/140416tn8 e.pdf



#### 6.2.7 RENESAS TOOL NEWS Document No.140816/tn6

This issue has been corrected in Applilet3 for RL78 V1.06.00.

• With setting of port 1 (target: RL78/G14 group)

When the port pins listed below are selected for port 1, the Code Generator outputs the unnecessary operator and value "| \_33\_PMC1\_DEFAULT". This is because the initial settings for unused bits in the PMC1 register are incorrect.

- P12
- P13
- P16
- P17

For details of the problem, refer to the URL below. https://www.renesas.com/doc/toolnews/eng/2014/140816tn6\_e.pdf

#### 6.2.8 RENESAS TOOL NEWS Document No.141216/tn5

This issue has been corrected in Applilet3 for RL78 V1.07.00.

3. Saving Projects with Settings for the A/D Convertor (Applicable Products: RL78/L1C Group)

When a project configured with the below settings for the A/D convertor is read, the "A fatal error occurred" dialog box is displayed, after which CS+ operation is terminated.

- Selection of analog input pin from among ANI0-ANI2, ANI5, and ANI6: ANI0-ANI1
- VREF(+)setting:
- AVREFP
- VREF(-)setting:
- AVREFM

For details of the problem, refer to the URL below. https://www.renesas.com/doc/toolnews/eng/2014/141216tn5\_e.pdf



#### 6.2.9 RENESAS TOOL NEWS Document No.150716/tn2

This issue has been corrected in Applilet3 for RL78 V1.10.00.

1. Clock Generation Circuit (PLL Circuit Operation)

(Applicable MCUs: RL78/D1A, RL78/F13, and RL78/F14 groups) Generated code includes an error when the PLL circuit is operating as the clock generation circuit. A wait is required immediately after setting the PLL control register (PLLCTL).

2. Setting P40 of Port 4

(Applicable MCUs: RL78/D1A, RL78/F12, RL78/F13, RL78/F14, RL78/G12, RL78/G13, RL78/G14, RL78/G1A, RL78/I1A, and RL78/L12 groups)

Generated code has an error when P40 is set such that the on-chip pull-up resistor for P40 is not connected even though this is included in the settings of the on-chip pull-up resistors for port 4. The code to set the pull-up resistor option register (PU4) of P40 is not generated.

3. Code Generated for UART0 and UARTF (Applicable MCUs: RL78/F12 group)

(a) Generated code has an error when unit 0 of the serial array unit is used as UART0 and its configuration is set to transmission or transmission and reception. Unnecessary code is output to the function void R\_UART0\_Creat(void) which is in r\_cg\_serial.c

(b) Generated code has an error in the setting of the LTXD0 pin when the asynchronous serial interface LIN-UART (UARTF) is set for transmission or transmission and reception. Incorrect code is output to the function void R\_UARTF0\_Create(void) which is in r\_cg\_serial.c.

For details of the problem, refer to the URL below. https://www.renesas.com/doc/toolnews/eng/2015/150716tn2\_e.pdf

#### 6.2.10 RENESAS TOOL NEWS Document No.151116/tn2

This issue has been corrected in Applilet3 for RL78 V1.10.00.

1. Indication of Channels of Serial Interface IICA (Applicable MCUs: RL78/G14 group R5F104MK, R5F104PK, R5F104ML, and R5F104PL)

Since the GUI does not indicate the channel 1 IICA serial interface for the above products, graphically setting up its operation is impossible. Accordingly, code for channel 1 cannot be generated.

2. Procedure for Setting the PLL Clock (Applicable MCUs: RL78/F13, RL78/F14, and RL78/F15 groups)

The generated code for setting the PLL clock in the clock generation circuit differs from the example of PLL settings in User's Manual: Hardware for the MCUs and is thus incorrect.

For details of the problem, refer to the URL below. https://www.renesas.com/doc/toolnews/eng/2015/151116tn2\_e.pdf



#### 6.2.11 RENESAS TOOL NEWS Document No.160116/tn5

This issue has been corrected in Applilet3 for RL78 V1.10.00.

Transfer of data with a length of 10 or more bits through an element of a serial array unit configured as a CSI or data with a length of 16 bits through an element configured as a UART (Applicable MCUs: RL78/F12, RL78/F13, RL78/F14, RL78/F15, and RL78/D1A groups)

Generated code has an error when an element of a serial array unit is set up for use as a 3-line serial (CSI) port and the length of data is specified as 10 or more bits, or the unit is set up for use as a UART and the length of data is specified as 16 bits.

For details of the problem, refer to the URL below. https://www.renesas.com/doc/toolnews/eng/2016/160116tn5\_e.pdf

#### 6.2.12 RENESAS TOOL NEWS Document No.160216/tn5

This issue has been corrected in Applilet3 for RL78 V1.10.00.

1. Using the error interrupt of serial array unit 4 as UART4 or DALI4 (Applicable products: RL78/I1A group)

Since the generated code has an error when error interrupts from serial array unit 4 as UART4 or DALI4 (digital addressable lighting interface) are selected, errors cannot be detected.

2. Using serial array unit 4 as DALI4 (Applicable products: RL78/I1A group)

Since the generated code has an error when the length of units for sending is set to 16 bits or the length for reception is set to 16, 17, or 24 bits, and serial array unit 4 is to be used as DALI4, transfer will not operate correctly.

For details of the problem, refer to the URL below. https://www.renesas.com/doc/toolnews/eng/2016/160216tn5\_e.pdf



#### 6.2.13 RENESAS TOOL NEWS Document No.160316/tn1

This issue has been corrected in Applilet3 for RL78 V1.10.00.

 Pin settings for the IICA serial interface when setting the PIOR to change the assignment of pin functions

(Applicable MCUs: RL78/G12 group (20- and 24-pin products))

When the IICA pin functions are redirected in the following way by setting the peripheral I/O redirection register (PIOR) to change the pin assignment, the generated code for the pin setting will have an error. This makes the IICA clock and data pins unusable with this setting.

(1) In setting the arrangement of pins for the clock generation circuit, select peripheral I/O redirection by checking PIOR2 bit = 1, and click on the button to fix the given pins as the pins to use.

(2) Operation as a single master or as a slave is selected on the IICA0 tabbed page.

For details of the problem, refer to the URL below. https://www.renesas.com/doc/toolnews/eng/2016/160316tn1\_e.pdf

#### 6.2.14 RENESAS TOOL NEWS Document R20TS0038EJ0100

This issue has been corrected in Applilet3 for RL78 V1.11.00.

• Scan Mode of A/D Converter RL78 family: RL78/F12, RL78/F13, RL78/F14, RL78/F15, and RL78/G1A groups

The following error dialog boxes might be displayed when the A/D converter is used in serial scan mode or one-shot scan mode, and three or fewer analog input pins are selected.

For details of the problem, refer to the URL below. https://www.renesas.com/en-us/doc/toolnews/eng/2016/r20ts0038ej0100\_cstnno.pdf

#### 6.2.15 RENESAS TOOL NEWS Document R20TS0139EJ0100

This issue has been corrected in Applilet3 for RL78 V1.13.00.

Input of Ports P10 and P11.
 RL78 family: RL78/G13 group (20, 24 and 25-pin products)
 In the port settings for applicable products, Ports P10 and P11 cannot be set for the TTL input buffer because the TTL buffer setting column is not provided for these ports.

2. Port Settings Related to Reset Processing
RL78 family: RL78/F12 group (20-pin products)
The products do not support software processing for port P120 described in the RL78/F12 user's manual.
For details of the problem, refer to the LIPL below.

For details of the problem, refer to the URL below. https://www.renesas.com/en-us/doc/toolnews/eng/2017/r20ts0139ej0100-cstnn.pdf



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