

Thank you for using the AP4 for RL78.

This document describes the restrictions and points for caution. Read this document before using the product.

Contents

Chapter 1. Introduction	2
Chapter 2. Target Devices	3
Chapter 3. Operating Environment.....	9
Chapter 4. Changes	10
4.1 Details of Changes	10
4.1.1 RL78/I1C has been updated according to update the common-part.....	10
Chapter 5. Restrictions	11
5.1 List of Restrictions	11
5.2 Restrictions Details.....	12
5.2.1 Online Help.....	12
5.2.2 Restrictions of the coding rule of MISRA-C	12
5.2.3 Restrictions of High-speed on-chip oscillator frequency select register(HOCODIV)	12
5.2.4 Restrictions of internal low-speed or internal high-speed oscillator trimming register	12
5.2.5 Restrictions of Flash memory CRC operation function (high-speed CRC).....	12
5.2.6 Restrictions of Port mode select register (PMS)	12
5.2.7 Cautions of the LIN-bus function of UART	12
5.2.8 Cautions of extension code, wakeup function and multimaster of serial interface IICA or IIC0	12
5.2.9 Cautions of Safety Functions	12
5.2.10 Restriction of USB.....	13
5.2.11 Fast Mode Plus setting in IICA slave	13
5.2.12 24-pin device TAU0 channel 1 setting restriction.....	13
5.2.13 Restriction on setting value of option byte C1H	13
5.2.14 Restriction on real-time clock API function	14
5.2.15 Restriction on real-time clock API function	14
Chapter 6. Correction History.....	15
6.1 List of RENESAS TOOL NEWS.....	15
6.2 Details of RENESAS TOOL NEWS	16
6.2.1 RENESAS TOOL NEWS Document No.150716/tn2	16
6.2.2 RENESAS TOOL NEWS Document No. R20TS0045EJ0100.....	16
6.2.3 RENESAS TOOL NEWS Document No. R20TS0290EJ0100.....	16
6.2.4 RENESAS TOOL NEWS Document No. R20TS0313EJ0100.....	17

Chapter 1. Introduction

The AP4 for RL78 is a software tool to generate control programs (device driver programs) for peripheral modules (timers, UART, A/D, etc.). It generates device driver codes using user settings through GUI. Initialize code and API (Application Programming Interface) functions are provided.

Chapter 2. Target Devices

Below is a list of devices supported by the AP4 for RL78/L13 V1.04.02.03	
PIN	Device name
64pin	R5F10WLA, R5F10WLC, R5F10WLD, R5F10WLE, R5F10WLF, R5F10WLG
80pin	R5F10WMA, R5F10WMC, R5F10WMD, R5F10WME, R5F10WMF, R5F10WMG
Following documents.	
Manual Name	Document Number
RL78/L13 User's Manual: Hardware	R01UH0382JJ0100 Rev.1.00
	R01UH0382EJ0100 Rev.1.00

Below is a list of devices supported by the AP4 for RL78/G1E V1.04.02.04	
PIN	Device name
64pin	R5F10FLC, R5F10FLD, R5F10FLE
80pin	R5F10FMC, R5F10FMD, R5F10FME
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/G1E User's Manual: Hardware	R01UH0353JJ0101 Rev.1.01

Below is a list of devices supported by the AP4 for RL78/G10 V1.05.02.03	
PIN	Device name
10pin	R5F10Y14, R5F10Y16, R5F10Y17
16pin	R5F10Y44, R5F10Y46, R5F10Y47
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/G10 User's Manual: Hardware	R01UH0384JJ0311 Rev.3.11
	R01UH0384EJ0311 Rev.3.11

Below is a list of devices supported by the AP4 for RL78/G1C V1.03.02.01	
PIN	Device name
32pin	R5F10JBC, R5F10KBC
48pin	R5F10JGC, R5F10KGC
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/G1C User's Manual: Hardware	R01UH0348JJ0100 Rev.1.00
	R01UH0348EJ0100 Rev.1.00

Below is a list of devices supported by the AP4 for RL78/H1D V1.00.00.05	
PIN	Device name
48pin	R5F11NGG, R5F11NGF
64pin	R5F11NLG, R5F11PLG, R5F11NLF, R5F11PLF
80pin	R5F11RMG, R5F11NMG, R5F11NMF, R5F11NME
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/H1D User's Manual: Hardware	R01UH0756JJ0080 Rev.0.80
	R01UH0756EJ0080 Rev.0.80

Below is a list of devices supported by the AP4 for RL78/L1C V1.03.01.04	
PIN	Device name
80pin	R5F110MJ, R5F110MH, R5F110MG, R5F110MF, R5F110ME, R5F111MJ, R5F111MH, R5F111MG, R5F111MF, R5F111ME
100pin	R5F110PJ, R5F110PH, R5F110PG, R5F110PF, R5F110PE, R5F111PJ, R5F111PH, R5F111PG, R5F111PF, R5F111PE
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/L1C User's Manual: Hardware	R01UH0409JJ0100 Rev.1.00
	R01UH0409EJ0100 Rev.1.00

Below is a list of devices supported by the AP4 for RL78/I1B V1.03.02.03	
PIN	Device name
80pin	R5F10MME, R5F10MMG
100pin	R5F10MPE, R5F10MPG
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/I1B User's Manual: Hardware	R01UH0407JJ0100 Rev.1.00
	R01UH0407EJ0100 Rev.1.00

Below is a list of devices supported by the AP4 for RL78/I1D V1.01.02.05	
PIN	Device name
20pin	R5F11768, R5F1176A
24pin	R5F11778, R5F1177A
30pin	R5F117A8, R5F117AA, R5F117AC
32pin	R5F117BA, R5F117BC
48pin	R5F117GA, R5F117GC
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/I1D User's Manual: Hardware	R01UH0474JJ0100 Rev.1.00
	R01UH0474EJ0100 Rev.1.00

Below is a list of devices supported by the AP4 for RL78/G1G V1.01.01.03	
PIN	Device name
30pin	R5F11EA8, R5F11EAA
32pin	R5F11EB8, R5F11EBA
44pin	R5F11EF8, R5F11EFA
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/G1G User's Manual: Hardware	R01UH0499JJ0100 Rev.1.00
	R01UH0499EJ0100 Rev.1.00

Below is a list of devices supported by the AP4 for RL78/G1F V1.01.02.03	
PIN	Device name
24pin	R5F11B7C, R5F11B7E
32pin	R5F11BBC, R5F11BBE
36pin	R5F11BCC, R5F11BCE
48pin	R5F11BGC, R5F11BGE
64pin	R5F11BLC, R5F11BLE
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/G1F User's Manual: Hardware	R01UH0516JJ0100 Rev.1.00
	R01UH0516EJ0100 Rev.1.00

Below is a list of devices supported by the AP4 for RL78/G1D V1.01.02.03	
PIN	Device name
48pin	R5F11AGG, R5F11AGH, R5F11AGJ
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/G1D User's Manual: Hardware	R01UH0515JJ0100 Rev.1.00
	R01UH0515EJ0100 Rev.1.00

Below is a list of devices supported by the AP4 for RL78/I1E V1.03.02.03	
PIN	Device name
32pin	R5F11CBC
36pin	R5F11CCC
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/I1E User's Manual: Hardware	R01UH0524JJ0100 Rev.1.00
	R01UH0524EJ0100 Rev.1.00

Below is a list of devices supported by the AP4 for RL78/I1C V1.01.03.02	
PIN	Device name
64pin	R5F11NLE, R5F11NLG
80pin	R5F11NME, R5F11NMG, R5F11NMJ
100pin	R5F11NPJ
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/I1C User's Manual: Hardware	R01UH0587JJ0051 Rev.0.51
	R01UH0587EJ0051 Rev.0.51

Below is a list of devices supported by the AP4 for RL78/G1H V1.01.02.03	
PIN	Device name
64pin	R5F11FLJ, R5F11FLK, R5F11FLL
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/G1H User's Manual: Hardware	R01UH0575JJ0100 Rev.1.00
	R01UH0575EJ0100 Rev.1.00

Below is a list of devices supported by the AP4 for RL78/G11 V1.02.02.04	
PIN	Device name
10pin	R5F1051A
16pin	R5F1054A
20pin	R5F1056A
24pin	R5F1057A
25pin	R5F1058A
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/G11 User's Manual: Hardware	R01UH0637JJ0110 Rev.1.10
	R01UH0637EJ0110 Rev.1.10

Below is a list of devices supported by the AP4 for RL78/L1A V1.01.02.03	
PIN	Device name
80pin	R5F11MMD, R5F11MME, R5F11MMF
100pin	R5F11MPE, R5F11MPF, R5F11MPG
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/L1A User's Manual: Hardware	R01UH0636JJ0100 Rev.1.00
	R01UH0636EJ0100 Rev.1.00

Below is a list of devices supported by the AP4 for RL78/F1E V1.01.02.01	
PIN	Device name
64pin	R5F11KLE, R5F11LLE, R5F11KLF, R5F11LLF, R5F11KLG, R5F11LLG
The Code Generator is based on the following documents	
Manual Name	Document Number
RL78/F1E User's Manual: Hardware	R01UH0611JJ0050 Rev.0.50
	R01UH0611EJ0050 Rev.0.50

Chapter 3. Operating Environment

▪ Host machine

- IBM PC/AT compatibles (Windows® 10, Windows® 8.1, Windows® 7)
- Processor: 1 GHz or higher (must support hyper-threading, multi-core CPUs)
- Memory capacity: 2 GB or more recommended. Minimum requirement is 1 GB or more (64-bit Windows requires 2 G or more)
- Hard disk capacity: 200 MB or more spare capacity
- Display: 1024 x 768 or higher resolution, 65,536 or more colors
- All other necessary software environments in addition to WindowsOS
 - .NET Framework version4.5.2

▪ Development Environments

Product Name	Version
IAR Embedded Workbench for Renesas RL78	V2.21 or later
Renesas GCC for RL78	V4.9 or later
Renesas electronics Compiler for 78K0R [CA78K0R]	V1.30 or later
Renesas electronics Compiler for RL78 [CC-RL]	V1.07 or later

Chapter 4. Changes

This chapter describes change to the AP4 for RL78 V1.14.00.

No	Description	Version *1
		RL78/I1C V1.01.03.02
1	RL78/I1C has been updated according to update the common-part	○

○ : Applicable, -: Not Applicable(finish of correction), /: Outside of function

Note 1: Version is described in the generated code.

4.1 Details of Changes

4.1.1 RL78/I1C has been updated according to update the common-part

RL78/I1C has been updated according to update the common-part.

Chapter 5. Restrictions

This section describes the cautions on the AP4 for RL78 V1.16.00.

5.1 List of Restrictions

No	Description	version *1															
		RL78/L1A	RL78/G11	RL78/I1C	RL78/G1H	RL78/I1E	RL78/G1D	RL78/G1F	RL78/G1G	RL78/I1D	RL78/I1B	RL78/L1C	RL78/G1C	RL78/G10	RL78/G1E	RL78/L13	RL78/H1D
		V1.01.02.03	V1.02.02.04	V1.01.02.04	V1.01.02.03	V1.03.02.03	V1.01.02.03	V1.01.01.03	V1.01.02.05	V1.03.02.03	V1.03.01.04	V1.03.02.01	V1.05.02.03	V1.04.02.04	V1.04.02.03	V1.00.00.05	V1.01.02.01
1	Online Help	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
2	Restrictions of the coding rule of MISRA-C.	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
3	Restrictions of High-speed on-chip oscillator frequency select register	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
4	Restrictions of internal low-speed or internal high-speed oscillator trimming	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
5	Restrictions of Flash memory CRC operation function (high-speed CRC)	○	○	○	○	○	○	○	○	○	○	○	/	○	○	○	○
6	Restrictions of Port mode select register (PMS)	○	○	○	○	○	○	○	○	○	○	○	/	○	○	○	○
7	Cautions of the LIN-bus function of UART	○	○	○	○	○	○	○	○	○	○	○	/	○	○	○	○
8	Cautions of extension code, wakeup function and multimaster of serial interface IICA or IIC0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
9	Cautions of Safety Functions	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
10	Restriction of USB	/	/	/	/	/	/	/	/	/	/	○	○	/	/	/	/
11	Fast Mode Plus setting in IICA slave	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
12	24-pin device TAU0 channel 1 setting restriction	/	/	/	/	/	/	○	/	/	/	/	/	/	/	/	
13	Restriction on setting value of option byte C1H	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	○
14	Restriction on real-time clock API function	/	/	/	○	○	/	○	/	/	/	/	/	/	/	/	/
15	Mistake in unit for 'Gain setting' of $\Delta\Sigma$ A/D CONVERTER																

○: Applicable, /: Not Applicable

Note 1: Version is described in the generated code.

5.2 Restrictions Details

5.2.1 Online Help

AP4 is not supporting online help.

5.2.2 Restrictions of the coding rule of MISRA-C

Compliance with the MISRA-C (Guidelines for the Use of the C Language in Vehicle Based Software) coding convention is not supported for source code output by AP4.

5.2.3 Restrictions of High-speed on-chip oscillator frequency select register(HOCODIV)

AP4 is not equivalent to a setup of high-speed on-chip oscillator frequency select register

5.2.4 Restrictions of internal low-speed or internal high-speed oscillator trimming register

AP4 is not equivalent to a setup of internal low-speed or internal high-speed oscillator trimming register.

5.2.5 Restrictions of Flash memory CRC operation function (high-speed CRC)

AP4 is not correspond to a flash memory CRC operation function (high-speed CRC). Please refer to application note r01an0736ej.

<https://www.renesas.com/search/keyword-search.html#genre=document&q=r01an0736ej>

5.2.6 Restrictions of Port mode select register (PMS)

AP4 is not supporting a port mode select register (PMS).

5.2.7 Cautions of the LIN-bus function of UART

AP4 is not supporting the LIN-bus functions of serial interface UART0, UART2, UART3, UART6 or UARTF.

5.2.8 Cautions of extension code, wakeup function and multimaster of serial interface IICA or IIC0

AP4 is not supporting the extension code, multimaster, and wakeup function of serial interface IICA or IC0.

5.2.9 Cautions of Safety Functions

AP4 is not supporting RAM parity error detection function of Safety Functions.

5.2.10 Restriction of USB

AP4 is not supporting USB host/function.

5.2.11 Fast Mode Plus setting in IICA slave

If the Fast Mode Plus is set when using the IICA slave, IICA Low level range setting register (IICWLn, n= channel number), and IICA High level range setting register (IICWHLn) are not set correctly.

[Workaround] There is no workaround.

After doing code generator, please rewrite the numerical value of the register setting of IICWLn, IICWHn in the R_IICAn_Create function. I depend on a system for the numerical value. Please change device UM to reference.

5.2.12 24-pin device TAU0 channel 1 setting restriction

In the 24-pin device, interval timer is only selectable for the TAU0 channel 1 setting.

[Workaround] There is no workaround.

In the 32-pin device, other timer functions besides "Interval timer" are selectable for the TAU0 channel 1 setting. Refer to the setting to make a correction.

5.2.13 Restriction on setting value of option byte C1H

The set value of option byte C1H is wrong.

1. In the case of the CA78K0R compiler, there is an wrong in the option byte value of the "r_option_ca.txt" file.

In the case of the CCRL compiler, there is an wrong in the option byte value of the "r_option_cc.txt" file.

```
/* Linker option for on-chip debug option byte and user option byte*/
-SECURITY_ID=00000000000000000000
-OCDBG=04
-USER_OPT_BYTE=FFFCA
```

2. In the case of the EWR78 compiler, there is an wrong in the option byte value of the "r_cg_main.c" file.

```
/* Set option bytes */
#pragma location = "OPTBYTE"
__root const uint8_t opbyte0 = 0xFFU;
#pragma location = "OPTBYTE"
__root const uint8_t opbyte1 = 0xFFU;
#pragma location = "OPTBYTE"
__root const uint8_t opbyte2 = 0xCAU;
```

3. In the case of the GCCRL78 compiler, there is an wrong in the option byte value of the "r_cg_vector_table.c" file.

```
/* Set option bytes */
const uint8_t Option_Bytes[] __attribute__((section(".option_bytes")))
{0xFFU, 0xFFU, 0xCAU, 0x04U};
```

Wrong: CLKMB = 0 when " Unused" is set, CLKMB = 1 when "Used" is set.

Right: CLKMB = 1 when " Unused" is set, CLKMB = 0 when "Used" is set.

[Workaround] There is no workaround.

After generating the code, correct the option byte value setting (CLKMB of C1H) to the correct value.

5.2.14 Restriction on real-time clock API function

An unnecessary wait time code is output in the R_RTC_Set_AlarmOn().

```

/* Change the waiting time according to the system */
for (w_count = 0U; w_count < RTC_WAITTIME_2FRTC; w_count++)
{
    NOP();
}

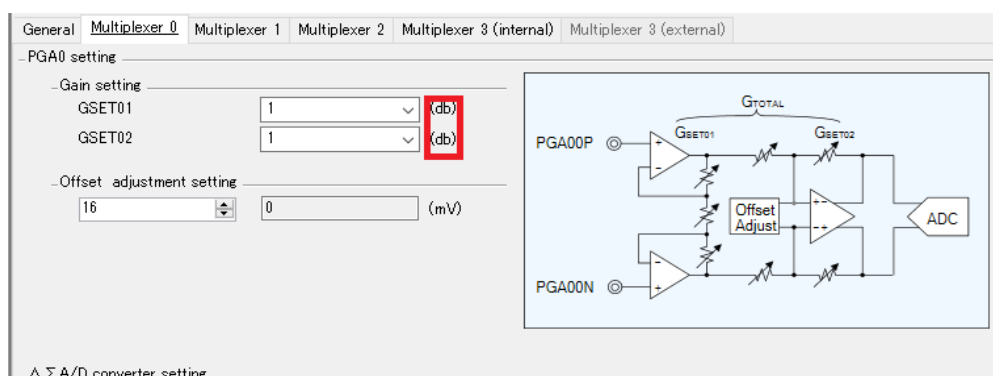
```

[Workaround] There is no workaround.

Delete the wait time code in the R_RTC_Set_AlarmOn () function after generating the code.

5.2.15 Restriction on real-time clock API function

The unit of Multiplexer 0/1/2/3(Internal)/3(external) are 'db' but it should be 'Gain'.



[Workaround] Please interpret 'db' as 'Gain' when use GSET01 and/or GSET02.

Chapter 6. Correction History

This section describes correction history of RENESAS TOOL NEWS.

6.1 List of RENESAS TOOL NEWS

Issue Date	Document No.	Description	Device Concerned	Fixed version
Jul. 16, 2015	150716/tn2	1. Clock Generation Circuit (PLL Circuit Operation)	RL78/G1C, RL78/L1C	V1.10.00
		2. Setting P40 of Port 4	RL78/G10, RL78/G1C, RL78/G1E, RL78/G1F, RL78/G1G, RL78/I1D, RL78/L1C, RL78/L13	V1.10.00
Aug. 01, 2016	R20TS0045EJ 0100	Peripheral I/O redirection register 0 (PIOR0)	RL78/G1F	V1.11.00
Mar. 16, 2018	R20TS0290EJ 0100	When Opening a Project for RL78/G11 Created by a Previous Version of Code Generator	RL78/G11 (20-pin R5F1056A)	V1.15.00
May. 16, 2018	R20TS0313EJ 0100	Writing to Port-Related Registers for Unused Pins	RL78/I1D	V1.15.00

6.2 Details of RENESAS TOOL NEWS

6.2.1 RENESAS TOOL NEWS Document No.150716/tn2

This issue has been corrected in AP4 for RL78 V1.10.00.

1. Clock Generation Circuit (PLL Circuit Operation)
(Applicable MCUs: RL78/G1C, and RL78/L1C groups)

Generated code includes an error when the PLL circuit is operating as the clock generation circuit. A wait is required immediately after setting the PLL control register (PLLCTL).

2. Setting P40 of Port 4
(Applicable MCUs: RL78/G10, RL78/G1C, RL78/G1E, RL78/G1F, RL78/G1G, RL78/I1D, RL78/L1C, and RL78/L13 groups)

Generated code has an error when P40 is set such that the on-chip pull-up resistor for P40 is not connected even though this is included in the settings of the on-chip pull-up resistors for port 4. The code to set the pull-up resistor option register (PU4) of P40 is not generated.

For details of the problem, refer to the URL below.

https://www.renesas.com/doc/toolnews/eng/2015/150716tn2_e.pdf

6.2.2 RENESAS TOOL NEWS Document No. R20TS0045EJ0100

This issue has been corrected in AP4 for RL78 V1.11.00.

1. Peripheral I/O redirection register 0 (PIOR0)
(Applicable MCUs: RL78/G1F group (32- and 36-pin products))

Regarding the common and clock generation circuit pin assignments, code generated by the tools listed above will have an error when the pin assignment setting of bit PIOR02 in the PIOR register should assign the SCLA0 and SDAA0 functions to pins P14 and P15. Thus, the serial interface IICA cannot be used.

For details of the problem, refer to the URL below.

<https://www.renesas.com/doc/toolnews/eng/2016/r20ts0045ej0100-cstnno.pdf>

6.2.3 RENESAS TOOL NEWS Document No. R20TS0290EJ0100

This issue has been corrected in AP4 for RL78 V1.15.00.

1. When Opening a Project for RL78/G11 Created by a Previous Version of Code Generator

1.1 Applicable Products

- V2.15.00 of the CS+ Code Generator for RL78 (V6.01 of CS+ for CC)
- V2.15.00 of the CS+ Code Generator for RL78 (V6.01 of CS+ for CA,CX)

1.2 Applicable MCUs

RL78 family: RL78/G11 group (20-pin R5F1056A)

When an attempt is made to open a project for RL78/G11 (R5F1056A) created by any of the following previous versions of code generator using a product shown in section 1.1, an error occurs and the project cannot be opened.

For details of the problem, refer to the URL below.

<https://www.renesas.com/doc/toolnews/eng/2018/r20ts0290ej0100-cstnno.pdf>

6.2.4 RENESAS TOOL NEWS Document No. R20TS0313EJ0100

This issue has been corrected in AP4 for RL78 V1.15.00.

1. Writing to Port-Related Registers for Unused Pins

RL78 family: RL78/I1D group

When using the applicable products to generate code for the port function, the following unnecessary register settings are made for the unused pins in a port when the mode (input or output) of each pin in the port is set. Because of this, the unused pins in the port output unintended data.

For details of the problem, refer to the URL below.

<https://www.renesas.com/doc/toolnews/eng/2018/r20ts0313ej0100-cstnno.pdf>

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
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 5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
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