ISL75055SLHMF

Low Dose Rate Total Ionizing Dose Testing of the ISL75055SLHMF 3A Source and Sink DDR Terminator/LDO

Introduction

This report summarizes the results of low dose rate (LDR) total ionizing dose (TID) testing of the ISL75055SLHMF, a radiation-hardened 3A source and sink DDR terminator/low dropout regulator (LDO) with buffered reference. The test was conducted to provide an assessment of the total dose hardness of the part and to provide an estimate of the bias sensitivity. Parts were irradiated either under bias or with all pins grounded at a LDR (0.01rad(Si)/s) to 100krad(Si) followed by a 168-hour biased anneal at 100ºC. The ISL75055SLHMF is rated to 75krad(Si) at LDR and is acceptance tested on a wafer-by-wafer basis to the datasheet limits.

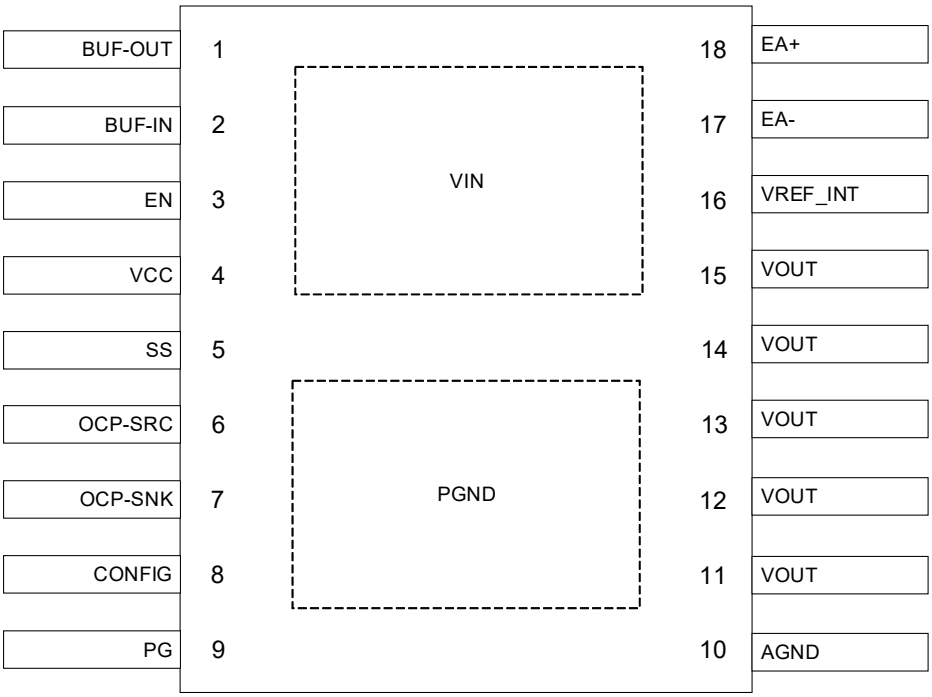
Product Description

The ISL75055SLHMF is a radiation-hardened 0.75V to 5.5V input, 3A sourcing and sinking low dropout linear regulator designed for powering the VTT termination rail of DDR memory modules. A buffered reference amplifier provides an accurate VREF reference supply for the DDR. Individual adjustable overcurrent protection (OCP) for sourcing and sinking allows the current limit of the LDO to be configured down to 300mA.

The ISL75055SLHMF features external error amplifier inputs to set VDDQ/2 as the reference voltage in DDR applications. It also features an internal 0.5V reference for standard LDO applications.

Separate VCC bias and LDO VIN pins, combined with an ultra-low dropout voltage, minimize internal power losses while ensuring highly accurate output voltage regulation.

The ISL75055SLHMF is available in an 18-lead ceramic metal-seal flatpack (CDFP) package with dual bottom heat slugs (CDFP) and operates across the full military temperature range of -55°C to +125°C. The device pin configuration is shown in Figure 1, and detailed pin descriptions are provided in Table 1.



Note: Pin 1 has a protrusion in the package lead. See Package Outline Drawing.

Figure 1. ISL75055SLHMF Pin Assignments

Table 1. ISL75055SLHMF Pin Descriptions

Pin Number	Pin Name	Description
1	BUF-OUT	Buffered reference output voltage 50% of BUF-IN for DDR applications. This pin can source or sink up to 10mA. Place a minimum of 100nF, maximum of 2.2µF capacitor on this pin to AGND for filtering. A minimum of 1µF is recommended for SEE mitigation. Buffered reference output is independent of EN input and active when BUF-IN is above 0.78V.
2	BUF-IN	Buffered reference input voltage VDDQ for DDR applications. An internal voltage divider outputs 50% of the input signal (VDDQ/2) on BUF-OUT pin. When VIN directly supplies BUF-IN, a 1kΩ/1µF filter is recommended at the input of BUF-IN for SEE mitigation.
3	EN	Enable pin for the LDO output.
4	VCC	Analog bias pin with 2.7V to 5.5V input range. Place a minimum 1µF capacitor on this pin to AGND for filtering.
5	SS	Soft-start pin. Place a capacitor on this pin for soft-start power up. A 20µA current source charges capacitor for ramping the reference of the error amplifier for a controlled start-up.
6	OCP-SRC	Sourcing overcurrent protection setting pin. A resistor on this pin to GND sets the Sourcing OCP level from 300mA to 3A. Short this pin to AGND for 4A typical sourcing OCP level.
7	OCP-SNK	Sinking overcurrent protection setting pin. A resistor on this pin to GND sets the Sinking OCP level from 300mA to 3A. Short this pin to AGND for 4.1A typical sourcing OCP level.
8	CONFIG	LDO VOUT and BUF-OUT discharge control pin. When low, discharge function disabled. When high, discharge function enabled. Internal switch discharges VOUT when EN = low. Internal switch discharges BUF-OUT when BUF-IN is below BUF-IN UVLO threshold
9	PG	Open-drain, power-good indicator pin. Place a resistor from PG to VCC. When VOUT is in overvoltage or undervoltage, PG pin pulls low.
10	AGND	Analog ground pin.
11, 12, 13, 14, 15	VOUT	LDO output pin. Refer to section 6.5 for more information on output capacitor selection
16	VREF_INT	Internal 500mV reference. Place a 0.1µF ceramic capacitor on this pin to AGND.
17	EA-	Inverting input to the error amplifier.
18	EA+	Non-inverting input to the error amplifier. Connect to VREF_INT for the 500mV internal reference or connect to BUF-OUT for DDR applications.
EPADU	VIN	LDO input voltage. A single 150µF tantalum capacitor and 2x10µF ceramic capacitor is recommended close to VIN and PGND connections. This is the upper EPAD on the backside of package. Connect EPADU to the PCB on multiple layers with thermal vias underneath the EPADU to maximize thermal performance.
EPADL	PGND	LDO power ground connection. Connect common to AGND pin. The lid of the part is internally connected to this pin. This is the lower EPAD on the backside of package. Connect EPADL to the PCB on multiple layers with thermal vias underneath the EPADL to maximize thermal performance.

Contents

1. Test Description 4
1.1 Irradiation Facility 4
1.2 Test Fixturing 4
1.3 Characterization Equipment and Procedures 4
1.4 Experimental Matrix 4
1.5 Downpoints 4
2. Results 5
2.1 Attributes Data 5
2.2 Variables Data 5
3. Discussion and Conclusion 49
4. Revision History 49
A. Appendix 50

1. Test Description

1.1 Irradiation Facility

LDR testing was performed at 0.01rad(Si)/s using a Hopewell Designs N40 vault-type LDR irradiator located in the Palm Bay, Florida Renesas facility. A PbAl box was used to shield the test fixture and devices under test against low energy, secondary gamma radiation. Post-irradiation anneals were performed under bias in a small temperature chamber.

1.2 Test Fixturing

Figure 2 shows the configuration used for the biased LDR testing and for the anneals.

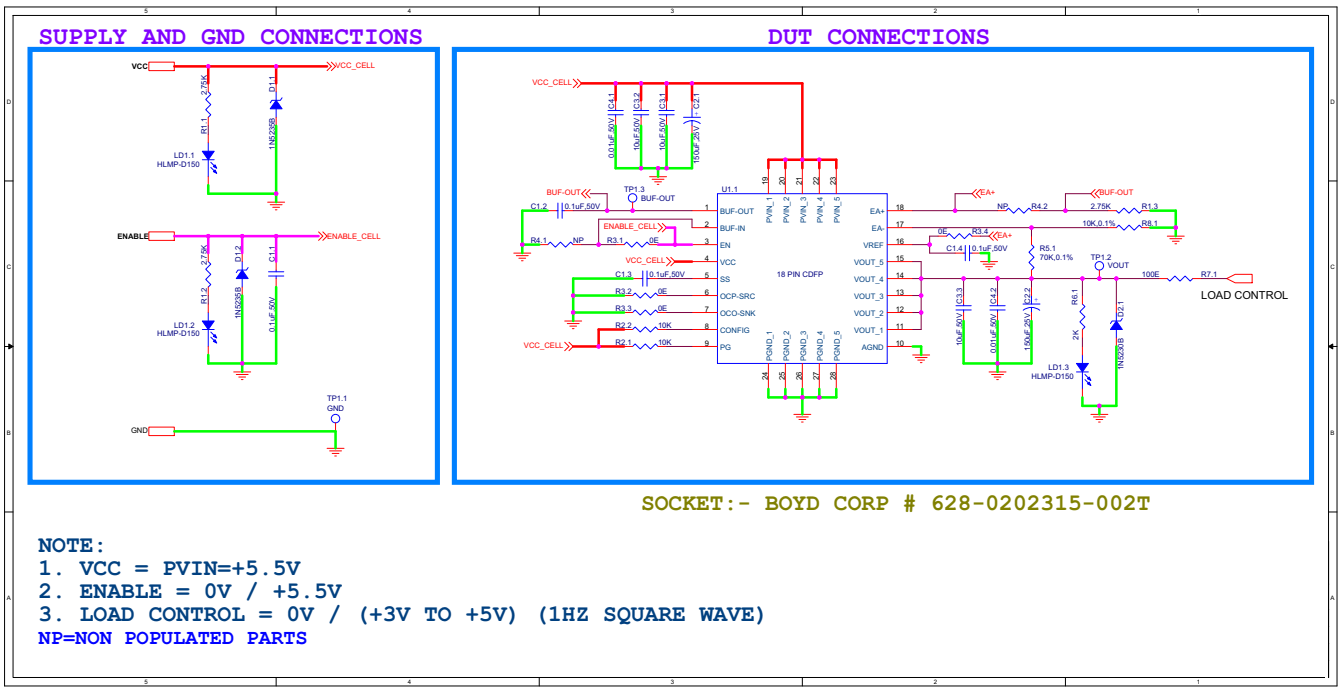


Figure 2. ISL75055SLHMF LDR Bias Configuration

1.3 Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using the production Automated Test Equipment (ATE) with data logging at each downpoint. Downpoint electrical testing was performed at room temperature.

1.4 Experimental Matrix

Irradiation was performed in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 18 samples irradiated at LDR under bias and 18 samples irradiated at LDR with all pins grounded. Eight of the units that were irradiated under bias and eight of the units that were irradiated with all pins grounded were also subject to a 168-hour, 100ºC biased anneal. Two control units were used.

The ISL75055SLHMF samples were drawn from wafer lot F6XR21. All samples were package in the standard 18-Ld hermetically sealed CDFP.

1.5 Downpoints

The planned irradiation downpoints for the LDR test were 0krad(Si), 10krad(Si), 15krad(Si), 30krad(Si), 40krad(Si), 50krad(Si), 75krad(Si), and 100krad(Si). Following irradiation, the LDR samples underwent a 168-hour high-temperature anneal at 100°C under bias.

2. Results

LDR TID testing of the ISL75055SLHMF is complete. All tested parameters passed the datasheet limits. Table 2 summarizes the results.

2.1 Attributes Data

Table 2. ISL75055SLHMF Attributes Data

Dose Rate (rad(Si)/s)	Condition	Sample Size	Downpoint	Pass[1]	Fail
0.01	Biased (Figure 2)	18	Pre-irradiation	18	0
			10krad(Si)	18	0
			15krad(Si)	18	0
			30krad(Si)	18	0
			40krad(Si)	18	0
			50krad(Si)	18	0
			75krad(Si)	18	0
			100krad(Si)	18	0
		8	Anneal	8	0
0.01	Grounded	18	Pre-irradiation	18	0
			10krad(Si)	18	0
			15krad(Si)	18	0
			30krad(Si)	18	0
			40krad(Si)	18	0
			50krad(Si)	18	0
			75krad(Si)	18	0
			100krad(Si)	18	0
		8	Anneal	8	0

1. A Pass indicates a sample that passes all datasheet limits.

2.2 Variables Data

The plots in Figure 3 to Figure 88 illustrate the LDR response of the parameters shown in Table 3 in the Appendix. The plots present average measured values of the parameters as a function of total dose under each irradiation condition, biased and grounded, and a 168-hour, 100ºC biased anneal. The plots also include error bars at each downpoint, representing the minimum and maximum measured values of the samples. In some plots, the error bars may not be visible due to their small magnitude relative to the graph scale.

All samples passed the datasheet limits after irradiation to each level up to 100krad(Si) and the subsequent anneal.

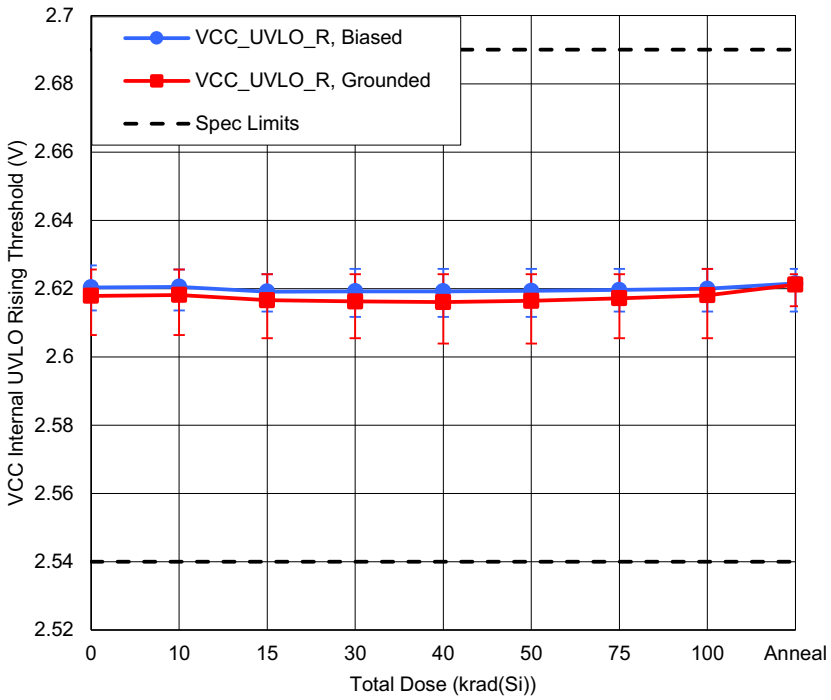


Figure 3. ISL75055SLHMF VCC Internal UVLO Rising Threshold (VCC_{UVLO_R}) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 2.54V and a maximum of 2.69V.

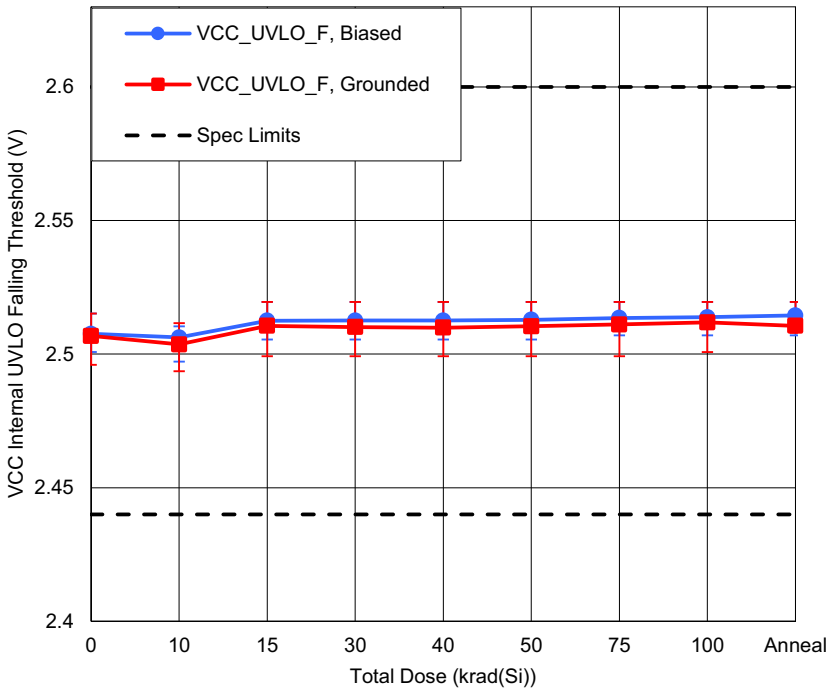


Figure 4. ISL75055SLHMF VCC Internal UVLO Falling Threshold (VCC_{UVLO_F}) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a 2.44V and a maximum of 2.6V.

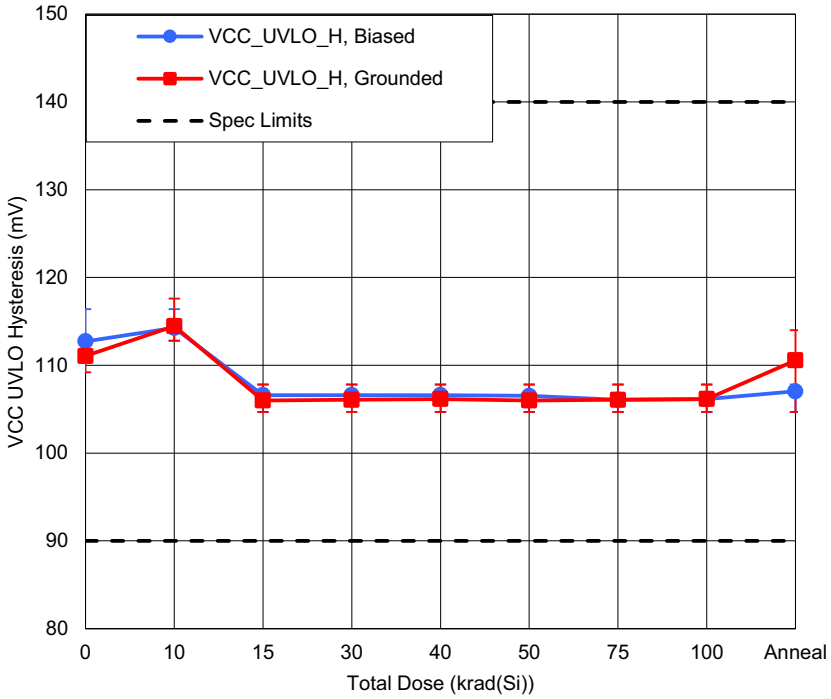


Figure 5. ISL75055SLHMF VCC UVLO Hysteresis (VCC_{UVLO_H}) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 90mV and a maximum of 140mV.

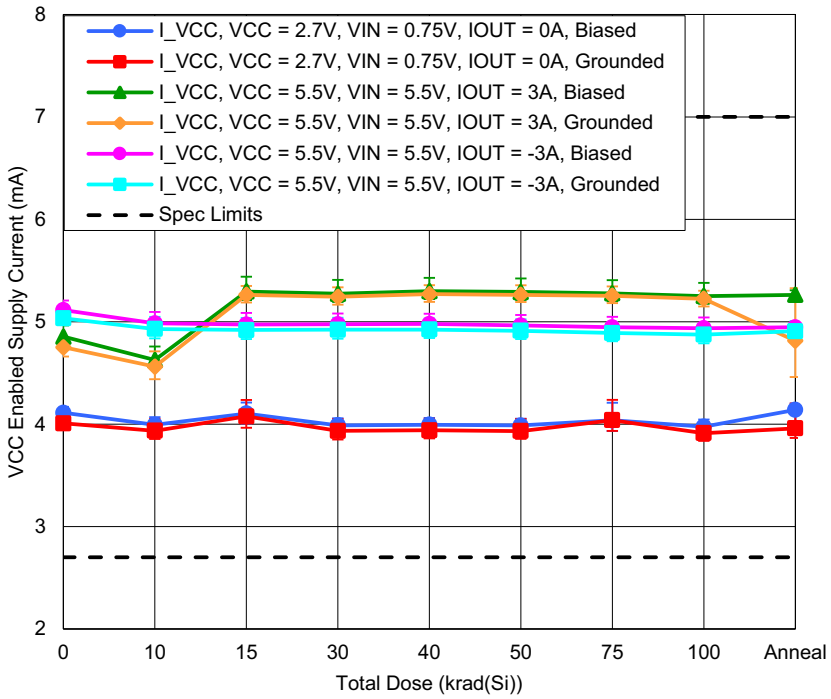


Figure 6. ISL75055SLHMF VCC Enabled Supply Current (I_{VCC}) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 2.7mA and a maximum of 7mA.

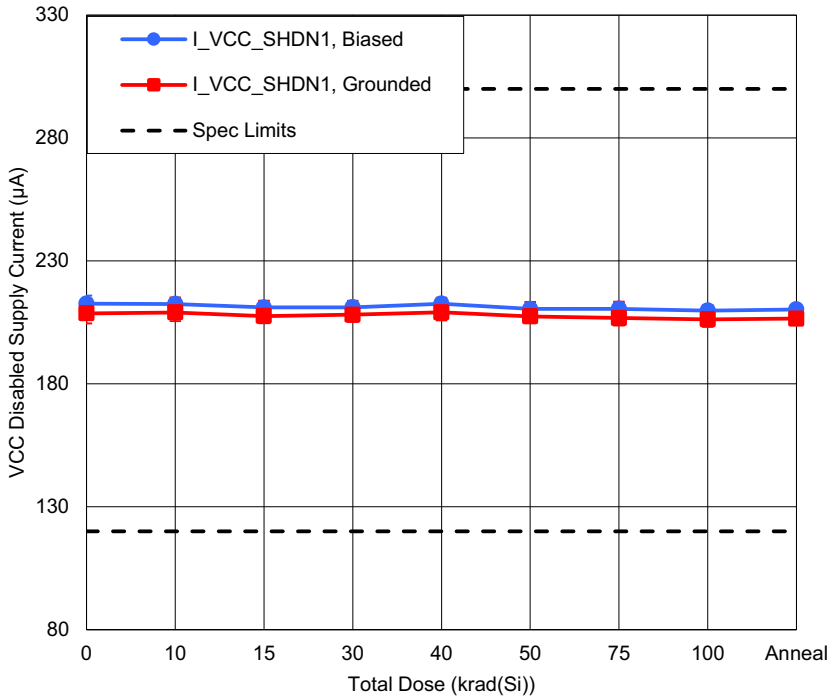


Figure 7. ISL75055SLHMF VCC Disabled Supply Current (I_{VCC_SHDN1}) with EN = 0V, V_{CC} = 5.5V, BUF-IN = 0V, EA+ = VREF_INT as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 120µA and a maximum of 300µA.

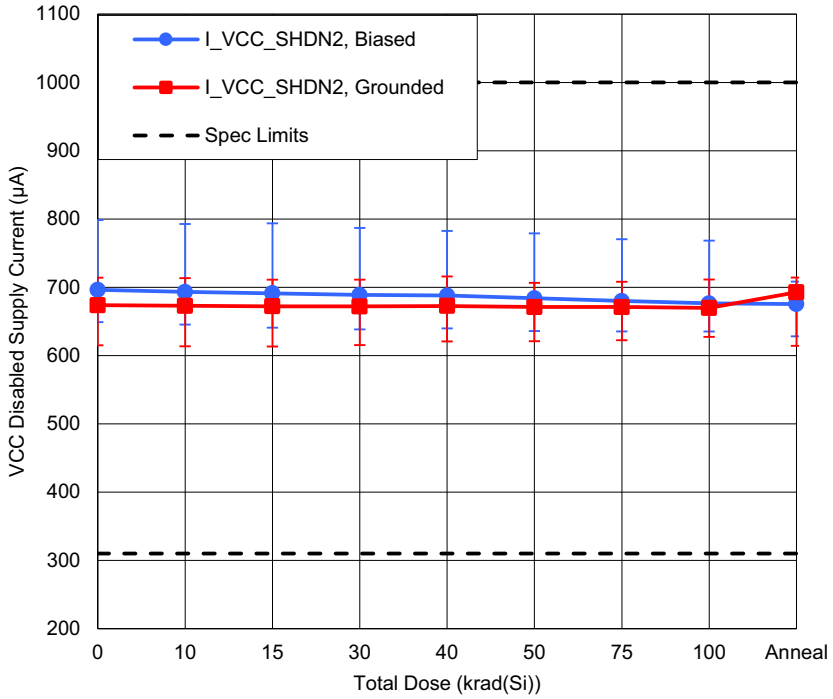


Figure 8. ISL75055SLHMF VCC Disabled Supply Current (I_{VCC_SHDN2}) with EN = 0V, V_{CC} = 5.5V, BUF-IN = 1V, EA+ = VREF_INT as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 310µA and a maximum of 1000µA.

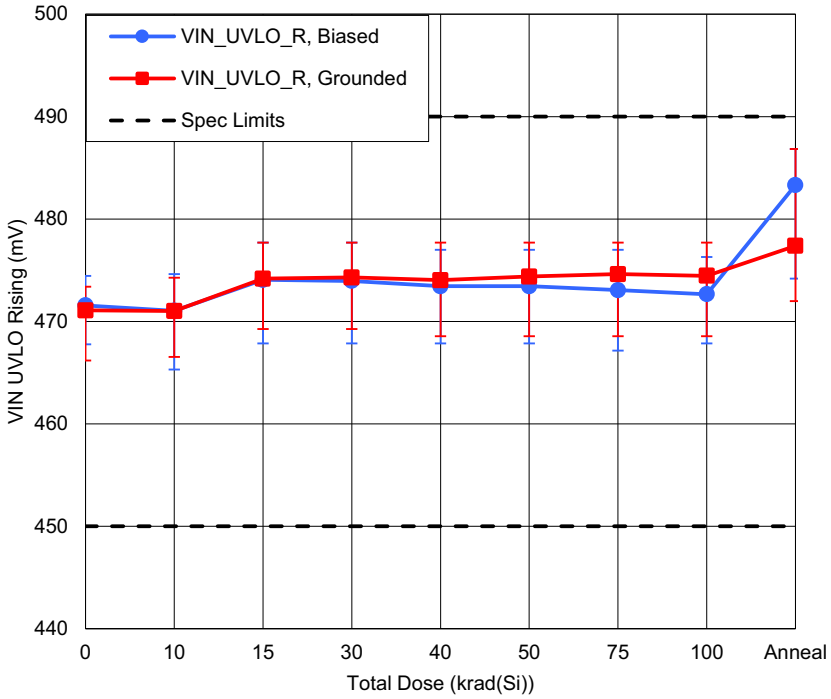


Figure 9. ISL75055SLHMF VIN UVLO Rising (VIN_{UVLO_R}) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 450mV and a maximum of 490mV.

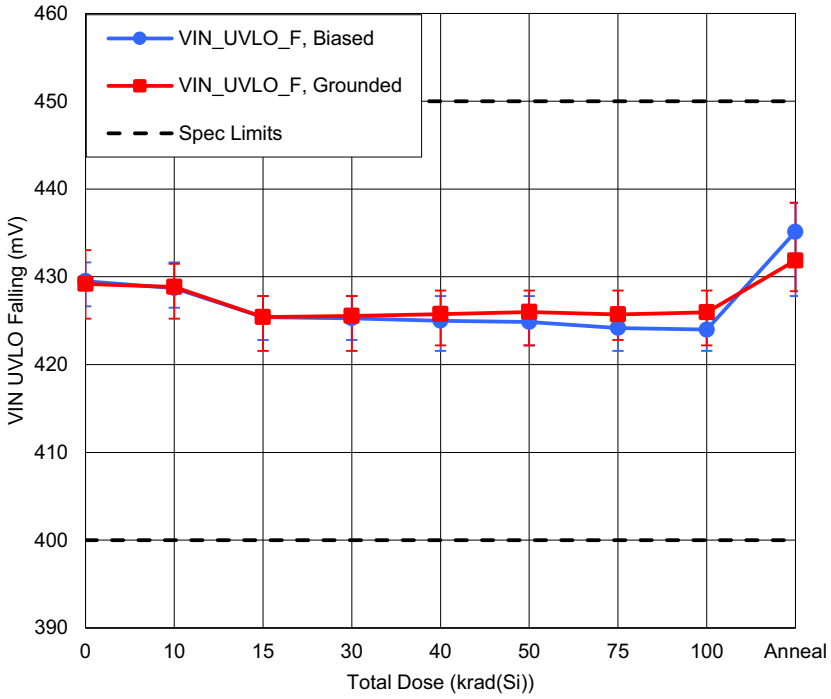


Figure 10. ISL75055SLHMF VIN UVLO Falling (VIN_{UVLO_F}) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 400mV and a maximum of 450mV.

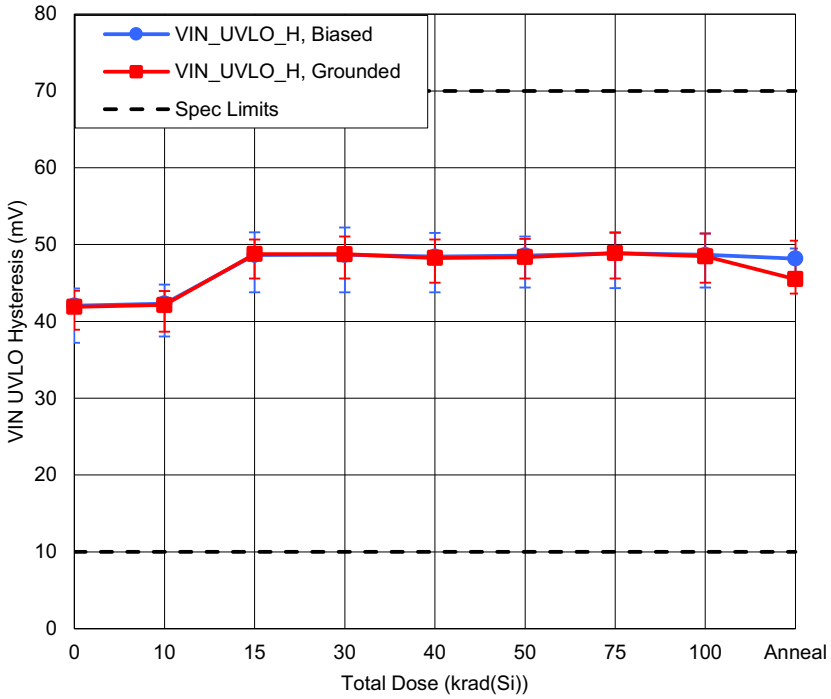


Figure 11. ISL75055SLHMF VIN UVLO Hysteresis (VIN_{UVLO_H}) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 10mV and a maximum of 70mV.

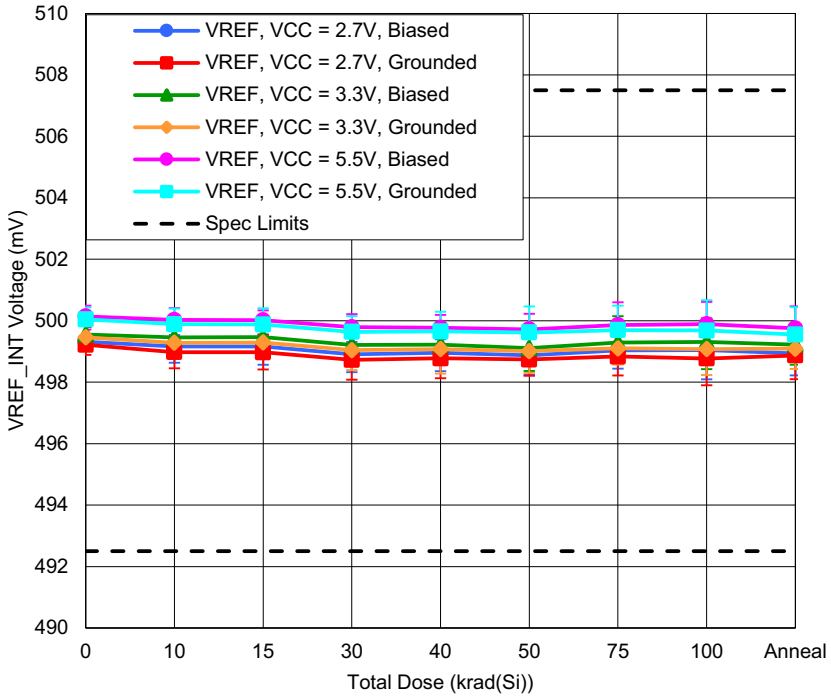


Figure 12. ISL75055SLHMF VREF_INT Voltage (V_{REF}) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 492.5mV and a maximum of 507.5mV.

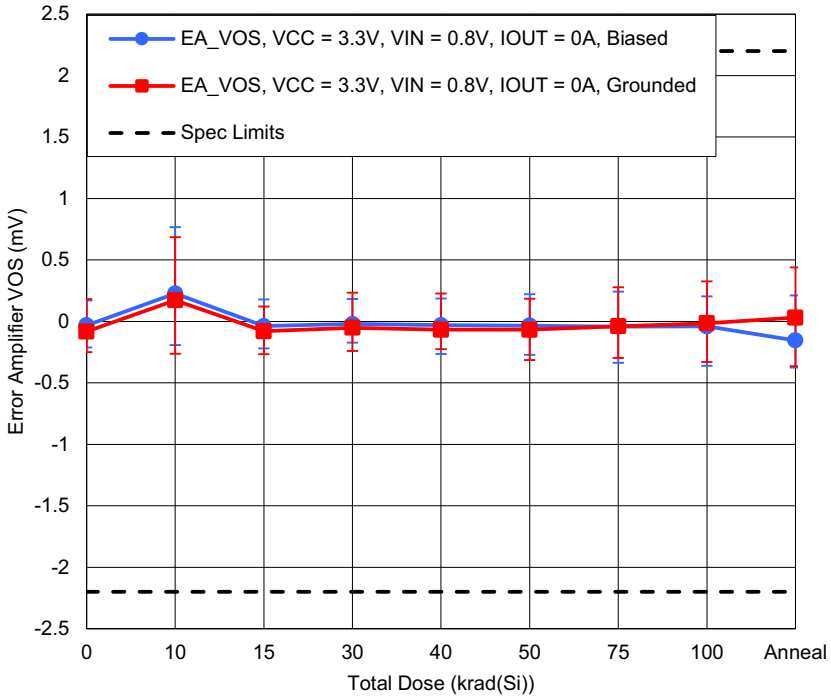


Figure 13. ISL75055SLHMF Error Amplifier VOS (EA_VOS) with V_{CC} = 3.3V, V_{IN} = 0.8V, I_{OUT} = 0A as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -2.2mV and a maximum of 2.2mV.

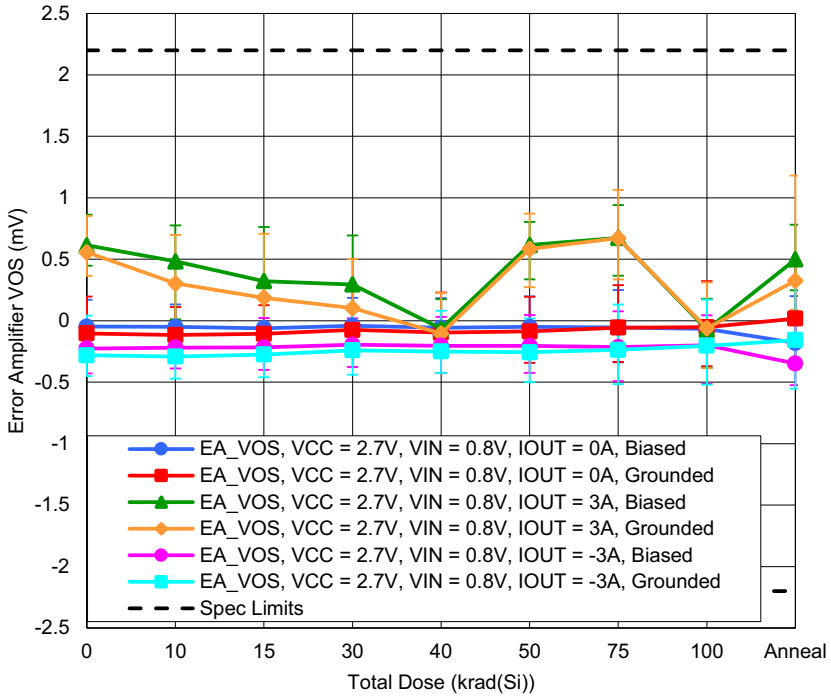


Figure 14. ISL75055SLHMF Error Amplifier VOS (EA_VOS) with V_{CC} = 2.7V, V_{IN} = 0.8V, I_{OUT} = 0A, 3A, or -3A as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -2.2mV and a maximum of 2.2mV.

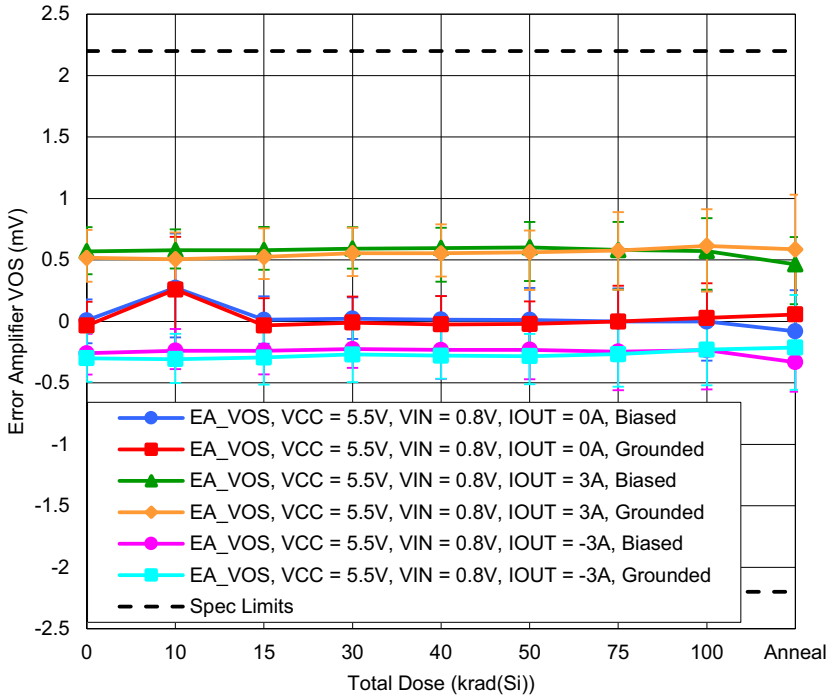


Figure 15. ISL75055SLHMF Error Amplifier VOS (EA_VOS) with V_{CC} = 5.5V, V_{IN} = 0.8V, I_{OUT} = 0A, 3A, or -3A as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -2.2mV and a maximum of 2.2mV.

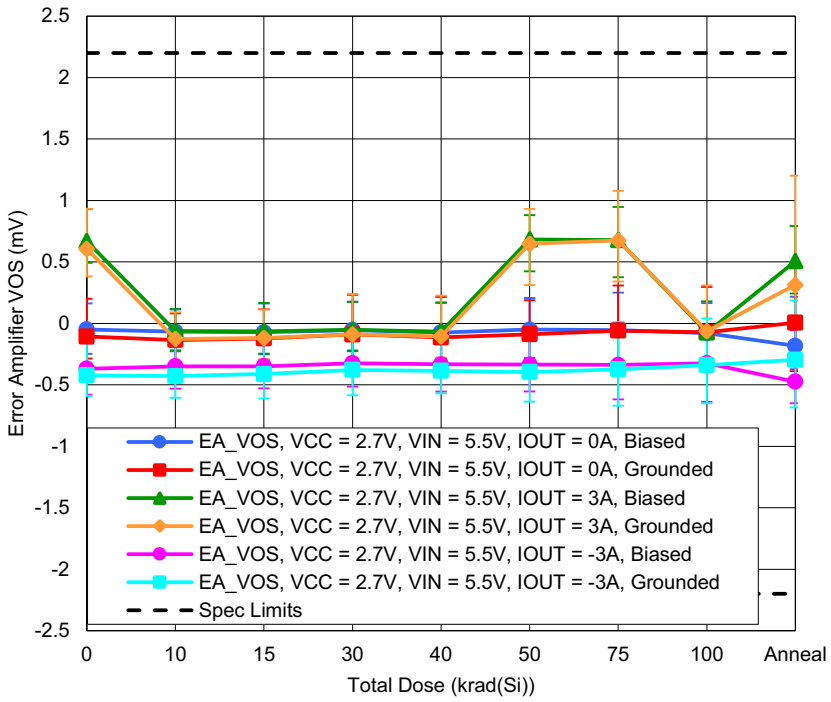


Figure 16. ISL75055SLHMF Error Amplifier VOS (EA_VOS) with V_{CC} = 2.7V, V_{IN} = 5.5V, I_{OUT} = 0A, 3A, or -3A as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -2.2mV and a maximum of 2.2mV.

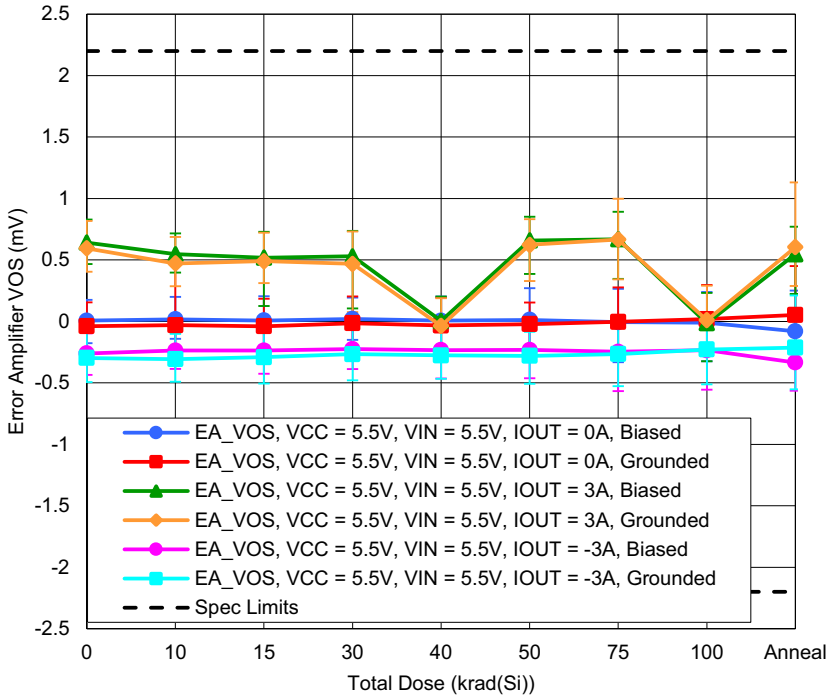


Figure 17. ISL75055SLHMF Error Amplifier VOS (EA_VOS) with V_{CC} = 5.5V, V_{IN} = 5.5V, I_{OUT} = 0A, 3A, or -3A as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -2.2mV and a maximum of 2.2mV.

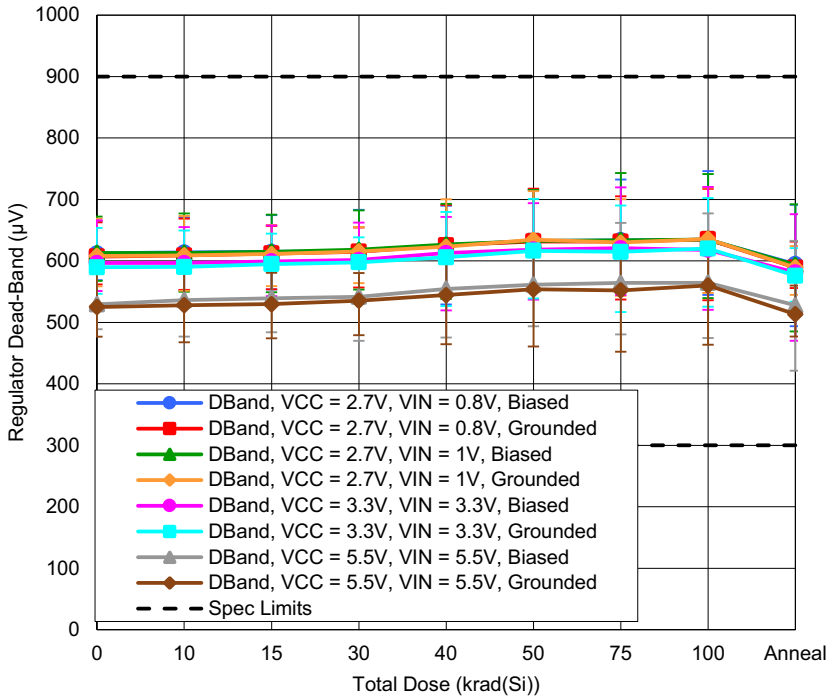


Figure 18. ISL75055SLHMF Regulator Dead-Band (DBand) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 300µV and a maximum of 900µV.

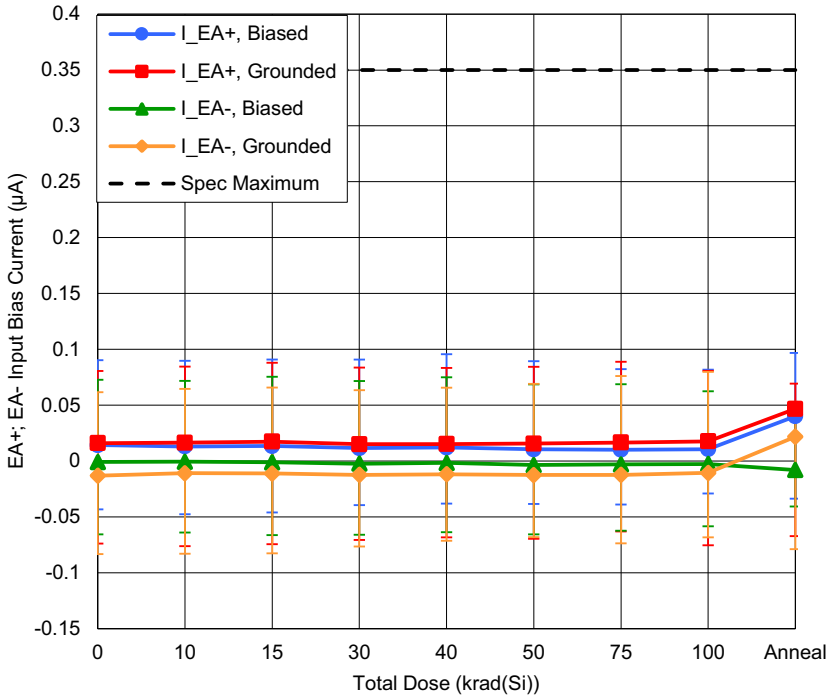


Figure 19. ISL75055SLHMF EA+; EA- Input Bias Current (I_EA+; I_EA-) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 0.35µA.

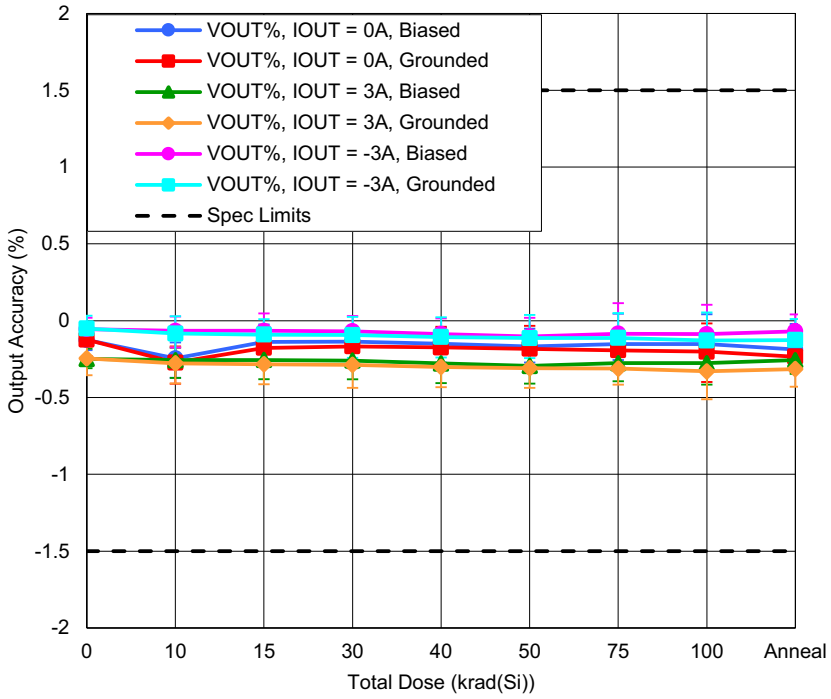


Figure 20. ISL75055SLHMF Output Accuracy (VOUT%) with V_{IN} = 0.75V, V_{CC} = 2.7V, V_{OUT} = 0.5V, and I_{OUT} = 0A, 3A or -3A as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a minimum of -1.5% and a maximum of 1.5%.

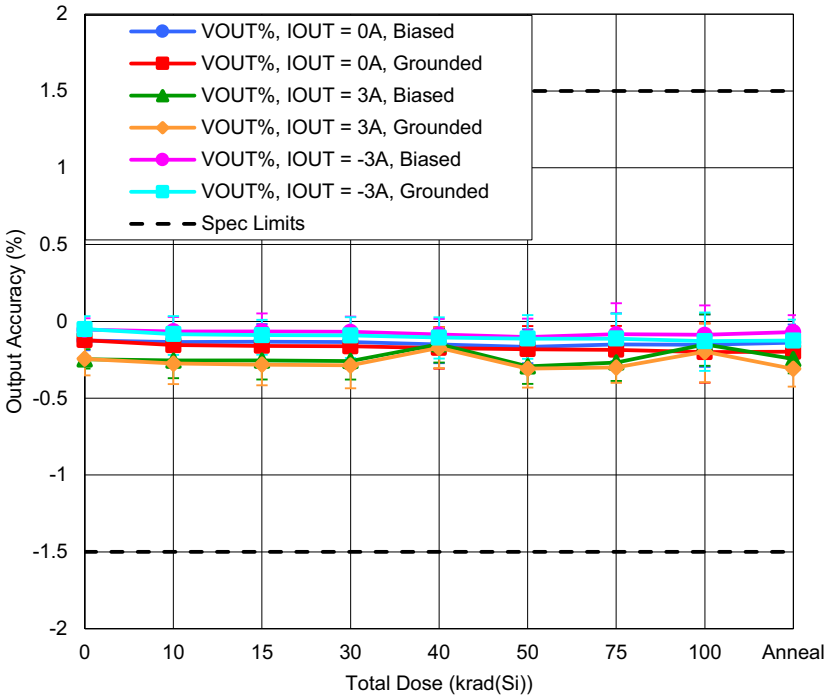


Figure 21. ISL75055SLHMF Output Accuracy (VOUT%) with V_{IN} = 5.5V, V_{CC} = 2.7V, V_{OUT} = 0.5V, and I_{OUT} = 0A, 3A or -3A as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a minimum of -1.5% and a maximum of 1.5%.

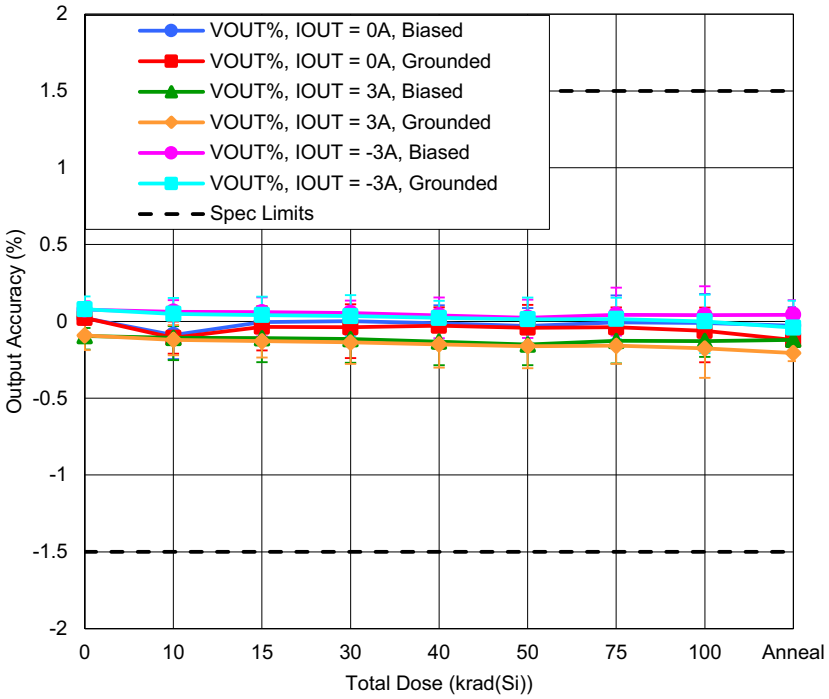


Figure 22. ISL75055SLHMF Output Accuracy (VOUT%) with V_{IN} = 0.75V, V_{CC} = 5.5V, V_{OUT} = 0.5V, and I_{OUT} = 0A, 3A or -3A as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a minimum of -1.5% and a maximum of 1.5%.

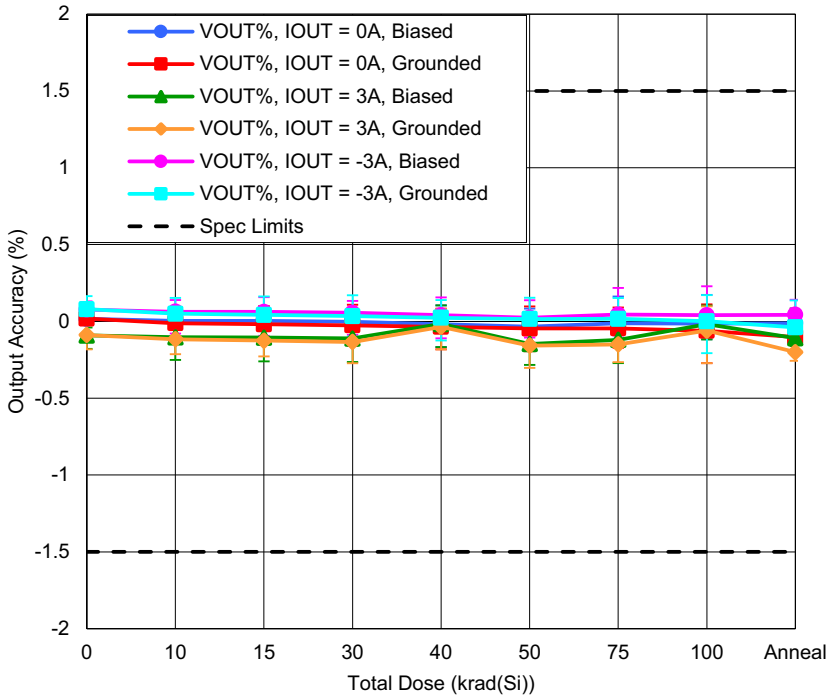


Figure 23. ISL75055SLHMF Output Accuracy (VOUT%) with V_{IN} = 0.75V, V_{CC} = 2.7V, V_{OUT} = 0.5V, and I_{OUT} = 0A, 3A or -3A as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a minimum of -1.5% and a maximum of 1.5%.

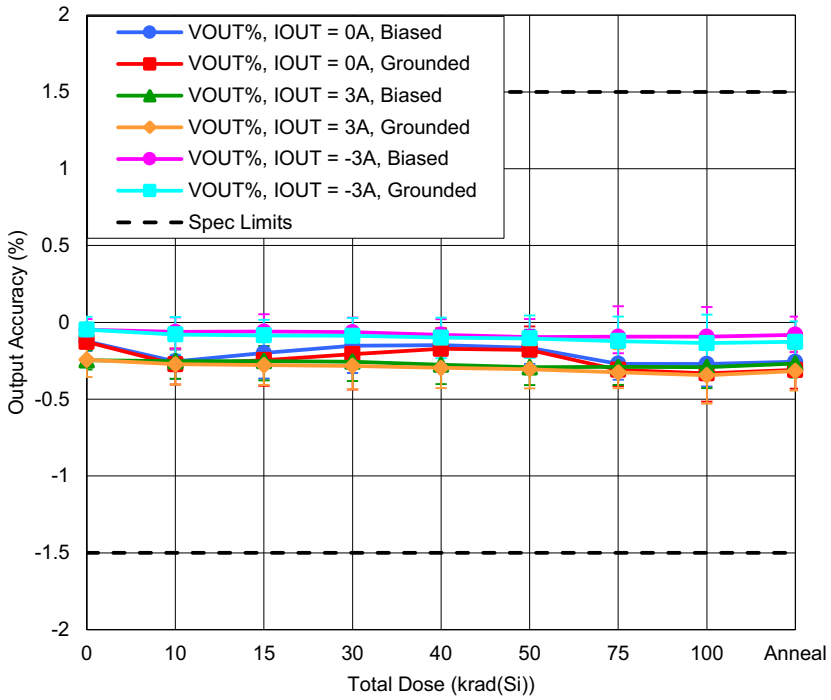


Figure 24. ISL75055SLHMF Output Accuracy (VOUT%) with V_{IN} = 1.5V, V_{CC} = 2.7V, V_{OUT} = 1.2V, and I_{OUT} = 0A, 3A or -3A as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a minimum of -1.5% and a maximum of 1.5%.

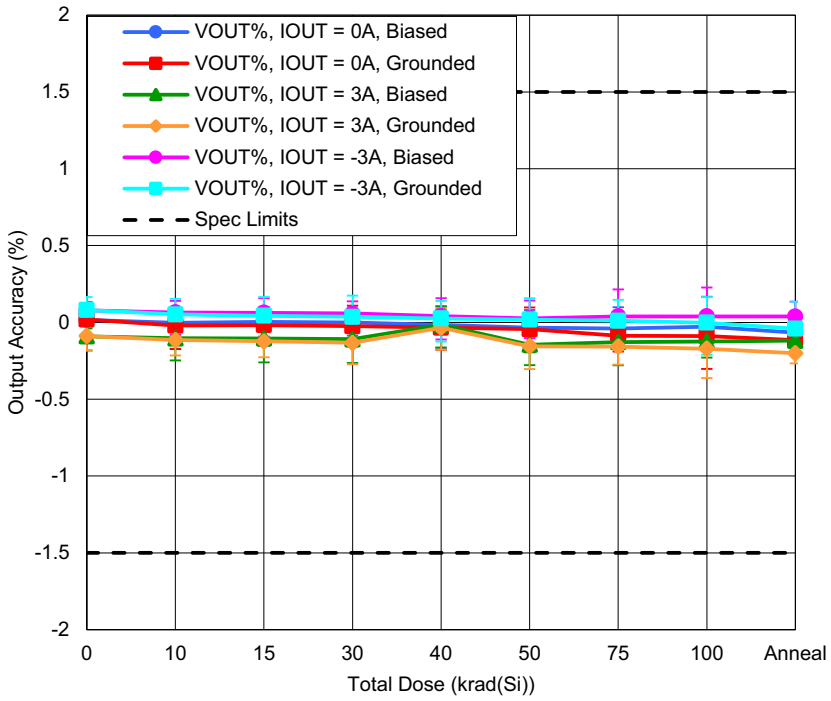


Figure 25. ISL75055SLHMF Output Accuracy (VOUT%) with V_{IN} = 0.75V, V_{CC} = 2.7V, V_{OUT} = 0.5V, and I_{OUT} = 0A, 3A or -3A as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a minimum of -1.5% and a maximum of 1.5%.

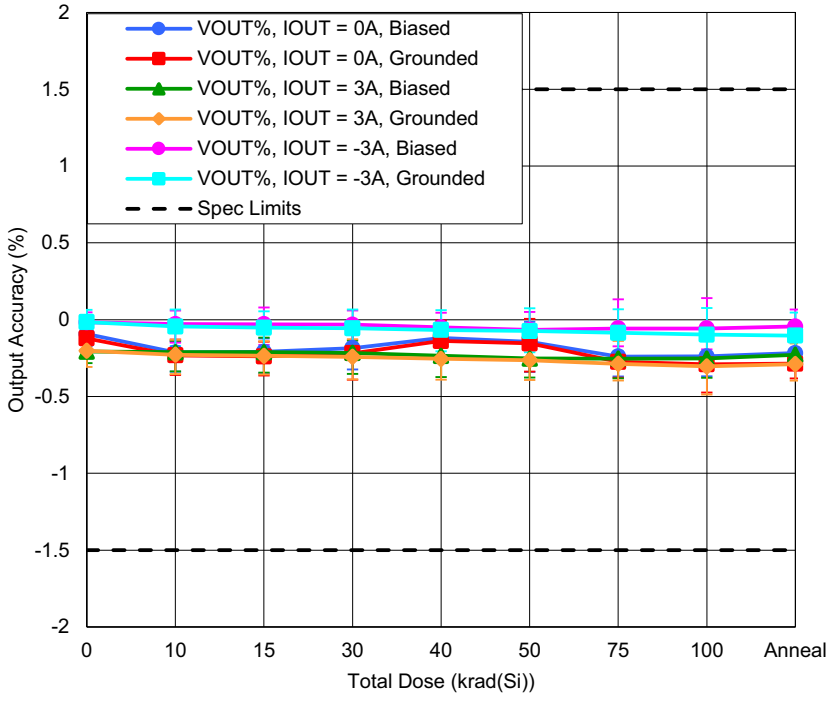


Figure 26. ISL75055SLHMF Output Accuracy (VOUT%) with V_{IN} = 2.1V, V_{CC} = 3.3V, V_{OUT} = 1.8V, and I_{OUT} = 0A, 3A or -3A as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a minimum of -1.5% and a maximum of 1.5%.

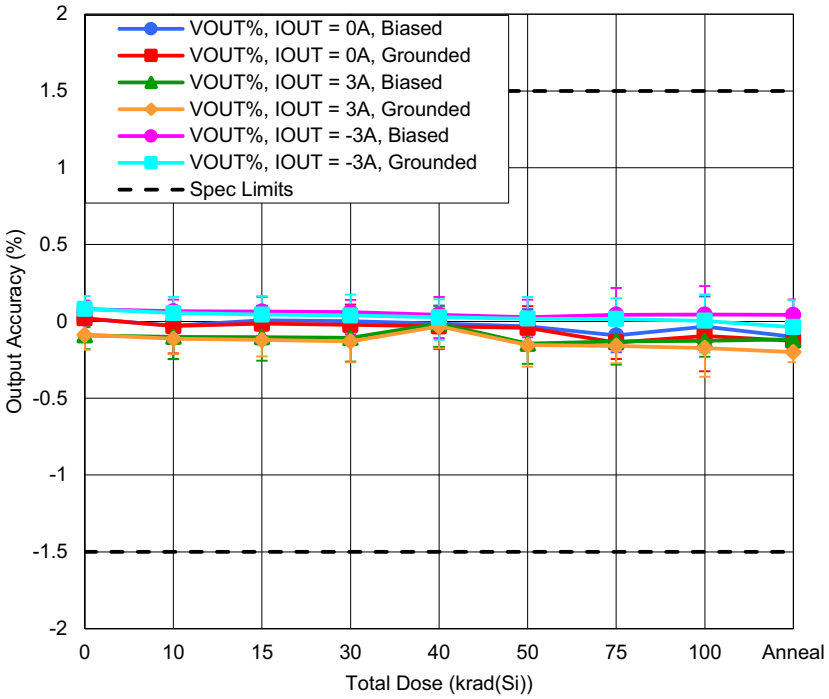


Figure 27. ISL75055SLHMF Output Accuracy (VOUT%) with V_{IN} = 5.5V, V_{CC} = 5.5V, V_{OUT} = 1.8V, and I_{OUT} = 0A, 3A or -3A as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a minimum of -1.5% and a maximum of 1.5%.

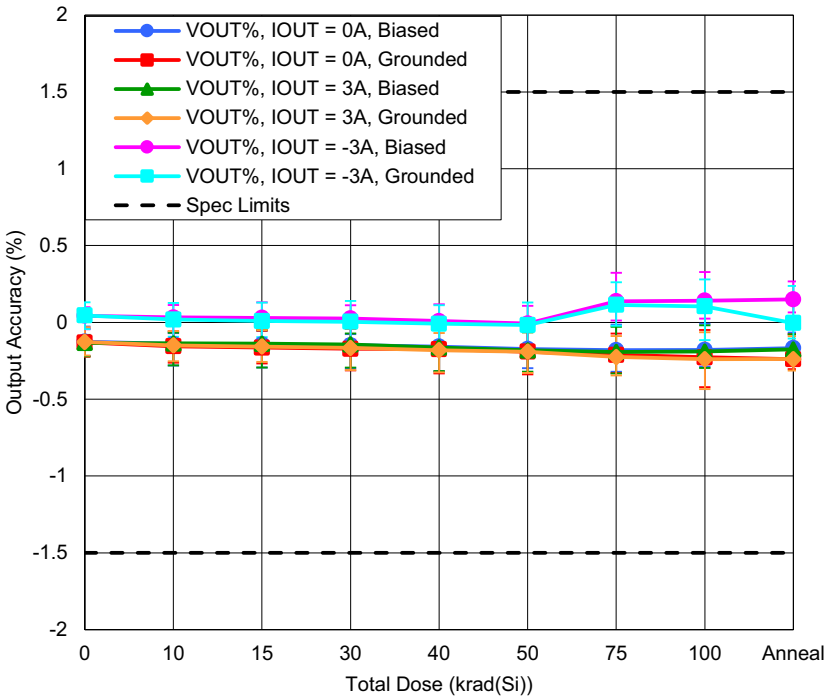


Figure 28. ISL75055SLHMF Output Accuracy (VOUT%) with V_{IN} = 3.6V, V_{CC} = 4.8V, V_{OUT} = 3.3V, and I_{OUT} = 0A, 3A or -3A as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a minimum of -1.5% and a maximum of 1.5%.

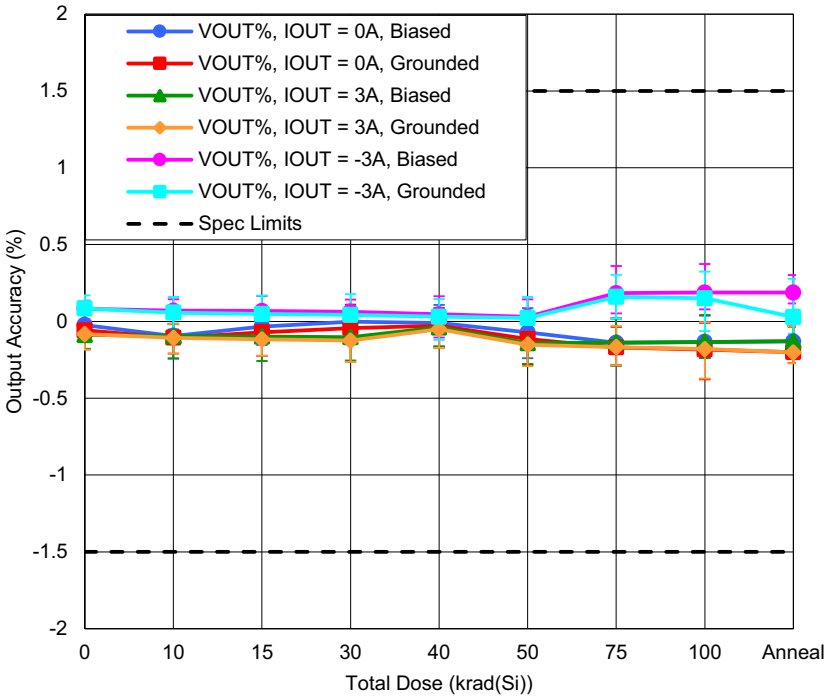


Figure 29. ISL75055SLHMF Output Accuracy (VOUT%) with V_{IN} = 5.5V, V_{CC} = 5.5V, V_{OUT} = 3.3V, and I_{OUT} = 0A, 3A or -3A as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a minimum of -1.5% and a maximum of 1.5%.

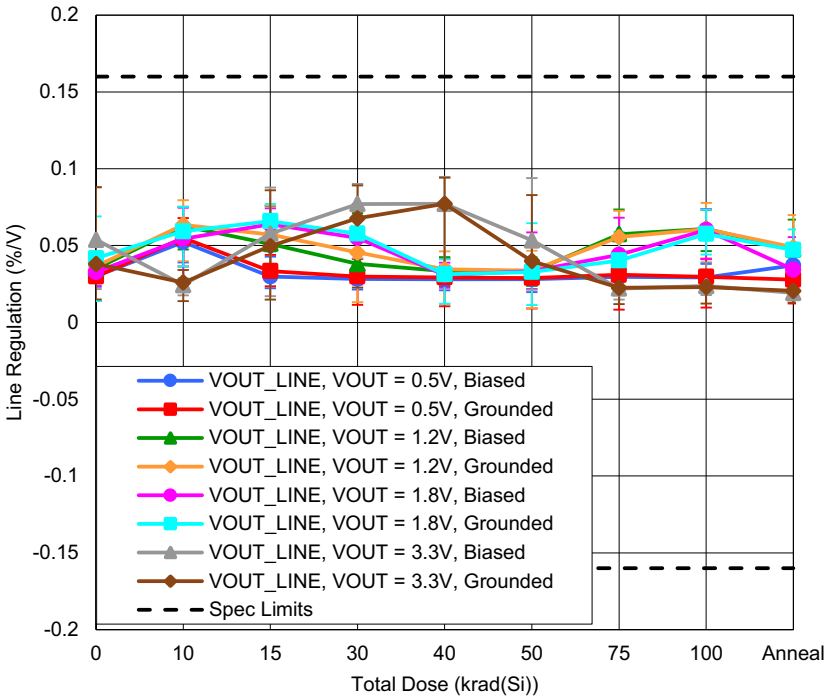


Figure 30. ISL75055SLHMF Line Regulation ($VOUT_{LINE}$) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -0.16%/V and a maximum of 0.16%/V.

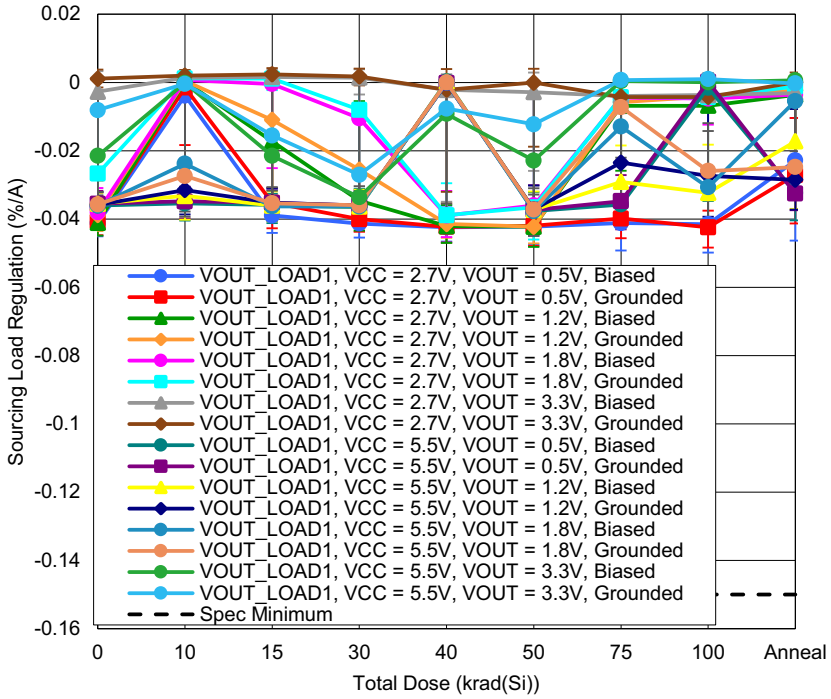


Figure 31. ISL75055SLHMF Sourcing Load Regulation (V_{OUT_LOAD1}) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a minimum of -0.15%/A.

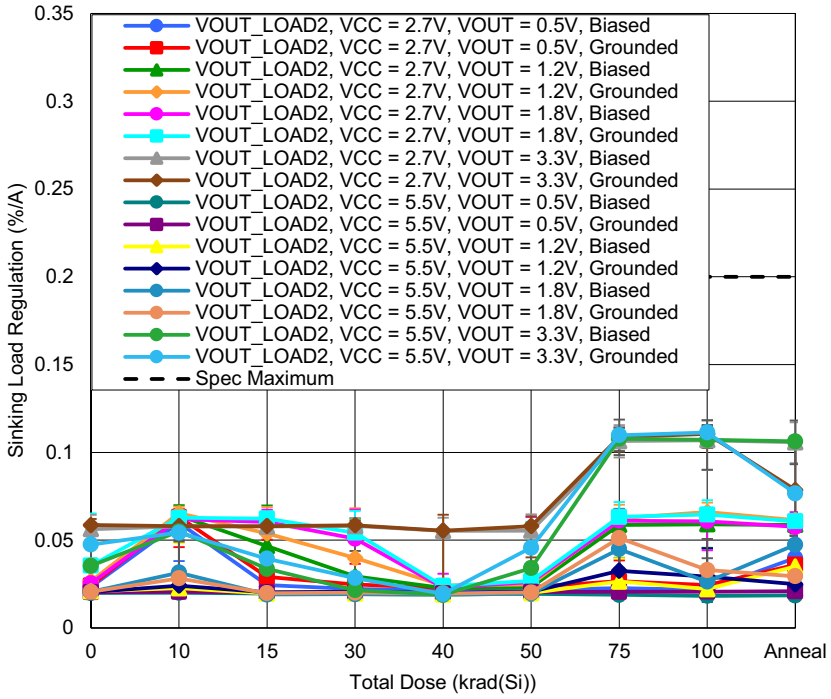


Figure 32. ISL75055SLHMF Sinking Load Regulation (V_{OUT_LOAD2}) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 0.20%/A.

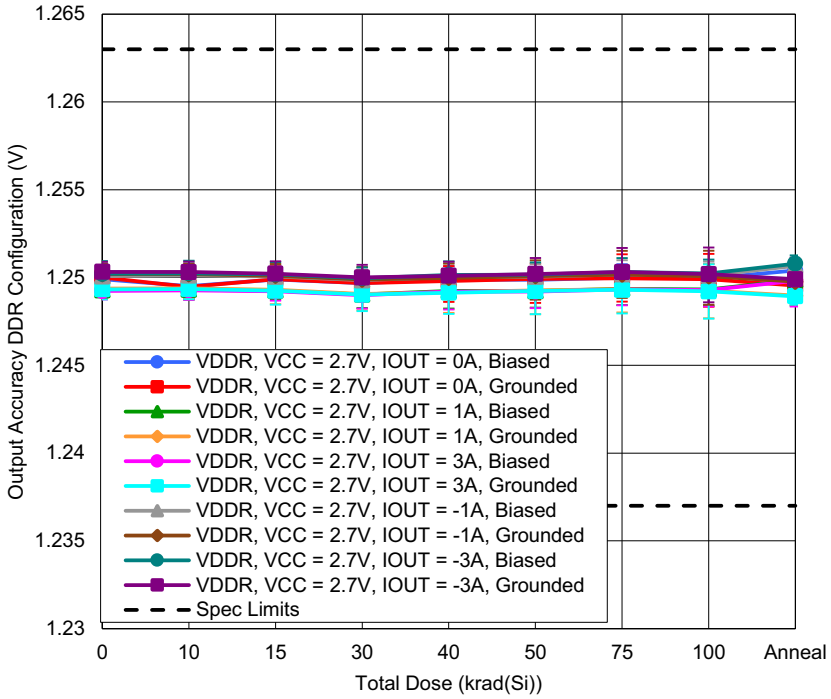


Figure 33. ISL75055SLHMF Output Accuracy DDR Configuration (V_DDR) with V_{IN} = BUF-IN = 2.5V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1.237V and a maximum of 1.263V.

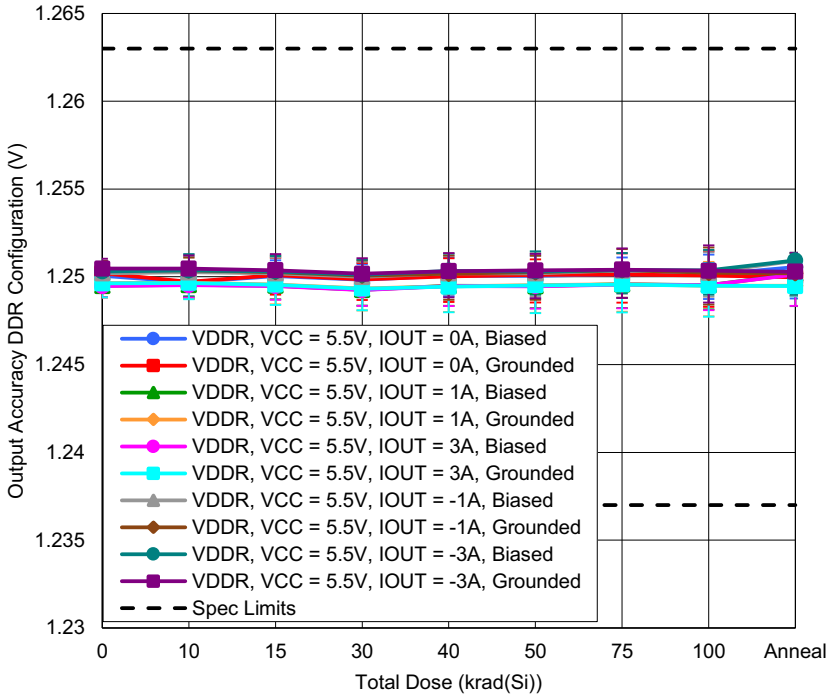


Figure 34. ISL75055SLHMF Output Accuracy DDR Configuration (V_DDR) with V_{IN} = BUF-IN = 2.5V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1.237V and a maximum of 1.263V.

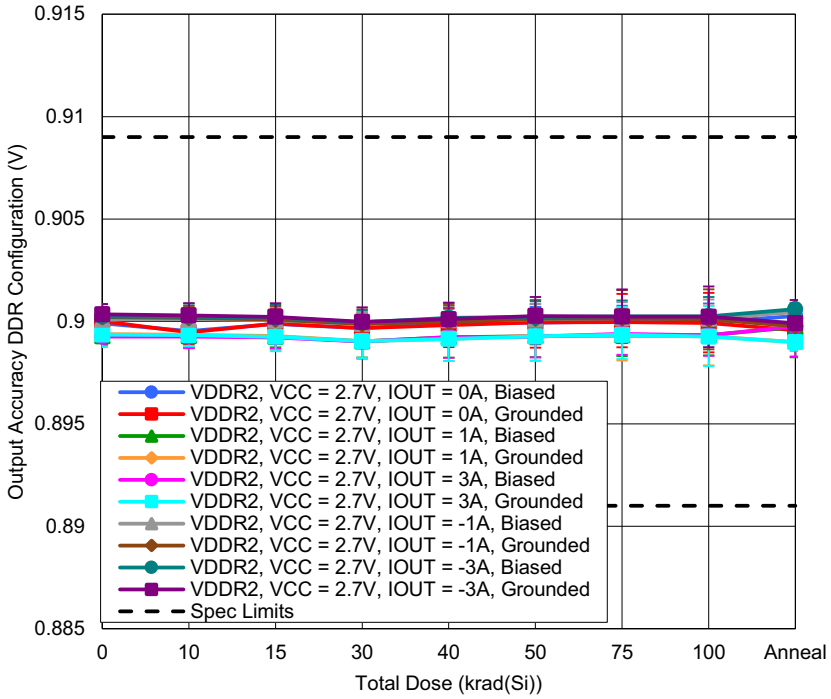


Figure 35. ISL75055SLHMF Output Accuracy DDR Configuration (V_DDR2) with V_{IN} = BUF-IN = 1.8V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.891V and a maximum of 0.909V.

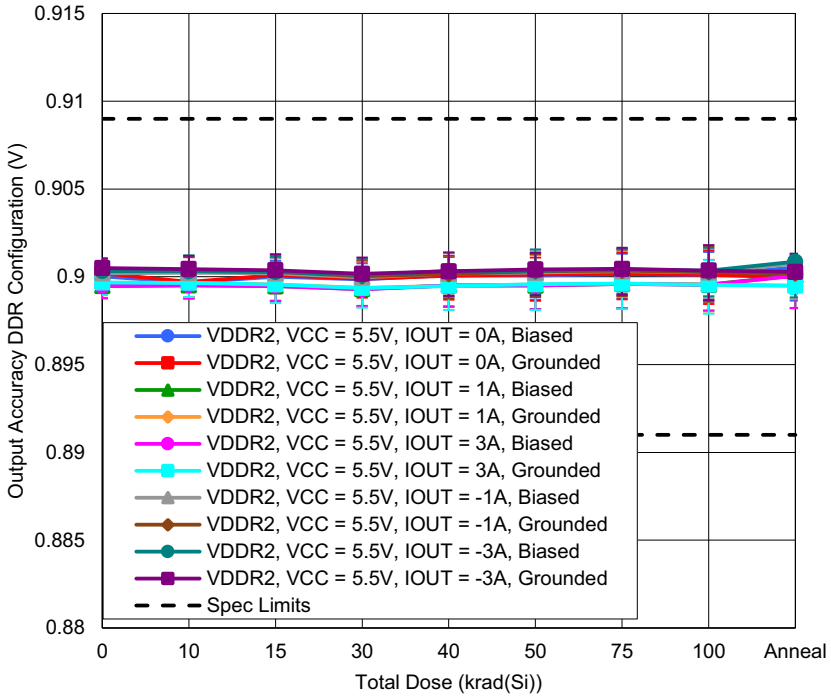


Figure 36. ISL75055SLHMF Output Accuracy DDR Configuration (V_DDR2) with V_{IN} = BUF-IN = 1.8V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.891V and a maximum of 0.909V.

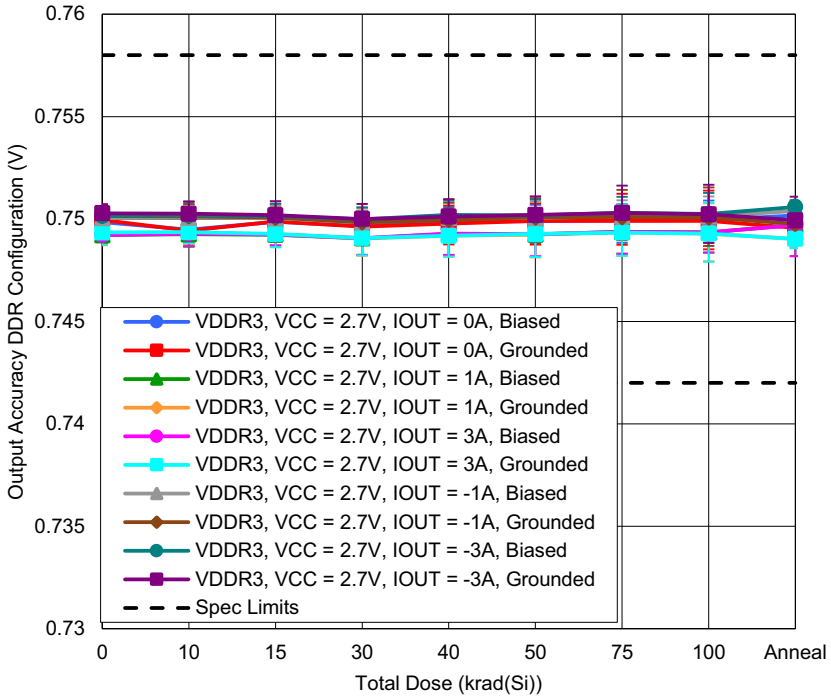


Figure 37. ISL75055SLHMF Output Accuracy DDR Configuration (V_DDR3) with V_{IN} = BUF-IN = 1.5V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.742V and a maximum of 0.758V.

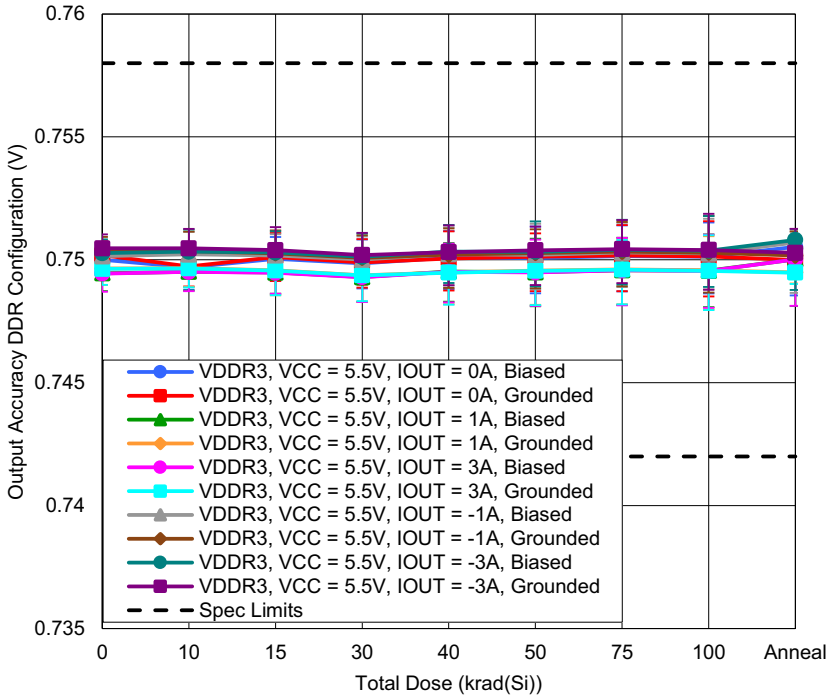


Figure 38. ISL75055SLHMF Output Accuracy DDR Configuration (V_DDR3) with V_{IN} = BUF-IN = 1.5V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.742V and a maximum of 0.758V.

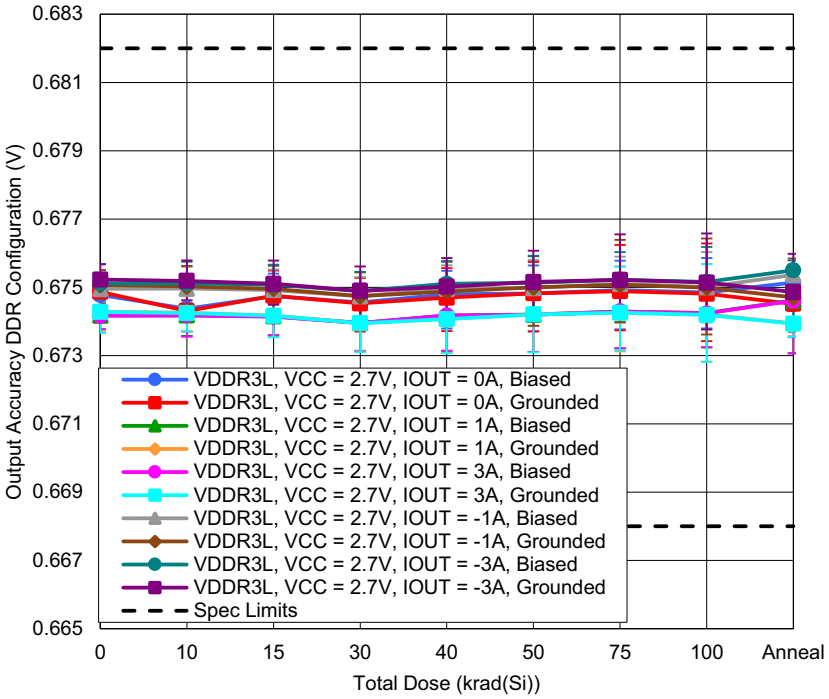


Figure 39. ISL75055SLHMF Output Accuracy DDR Configuration (V_DDR3L) with V_{IN} = BUF-IN = 1.35V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.668V and a maximum of 0.682V.

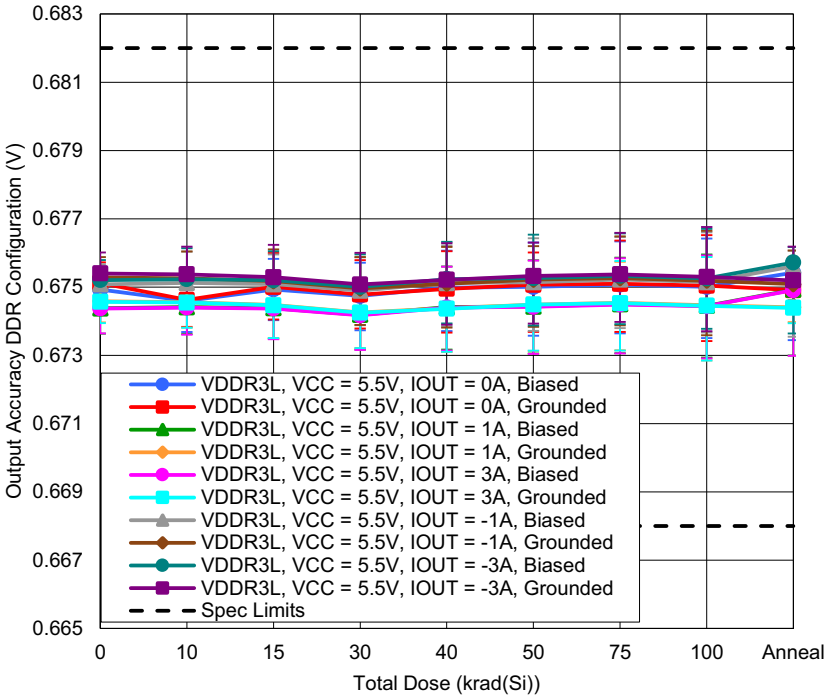


Figure 40. ISL75055SLHMF Output Accuracy DDR Configuration (V_DDR3L) with V_{IN} = BUF-IN = 1.35V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.668V and a maximum of 0.682V.

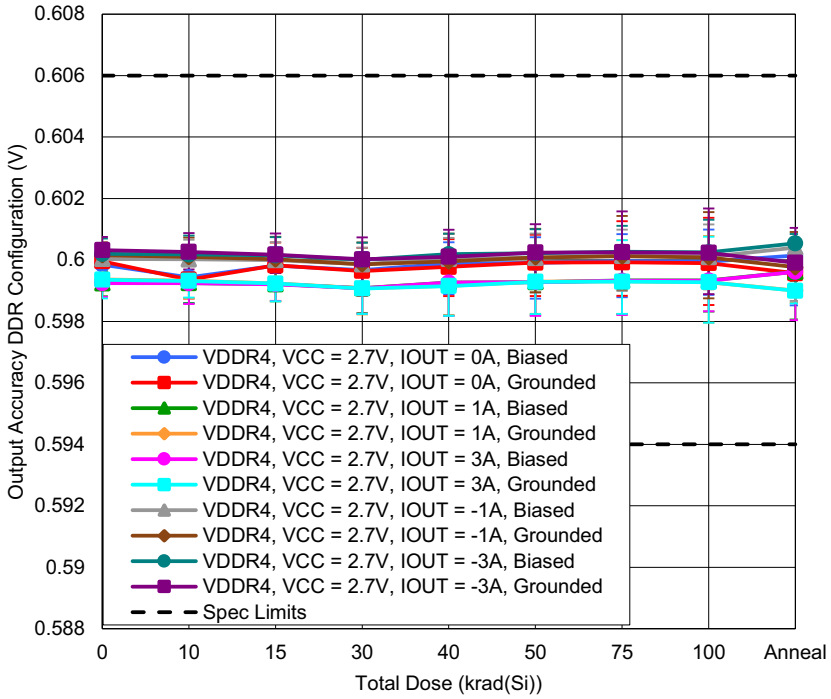


Figure 41. ISL75055SLHMF Output Accuracy DDR Configuration (V_DDR4) with V_{IN} = BUF-IN = 1.2V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.594V and a maximum of 0.606V.

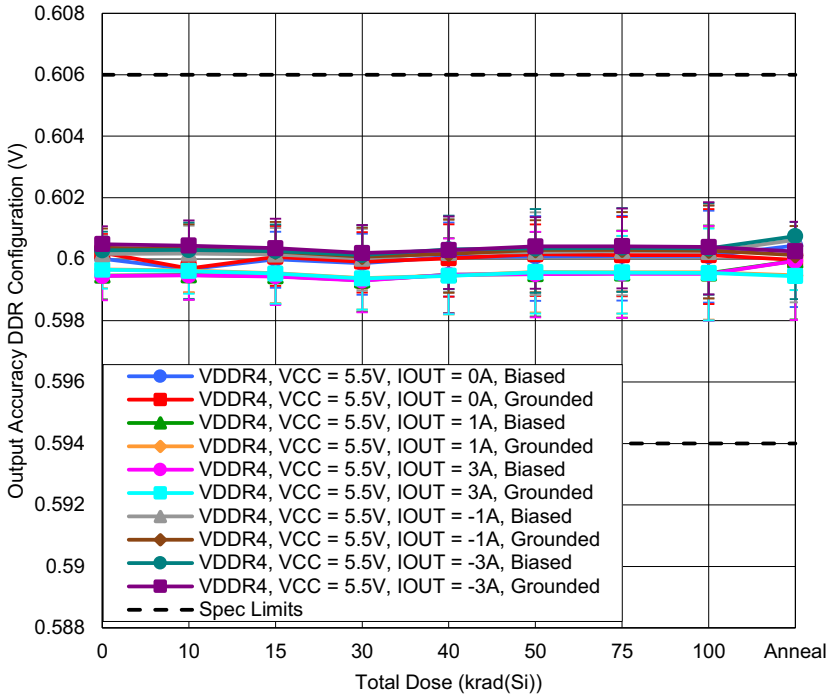


Figure 42. ISL75055SLHMF Output Accuracy DDR Configuration (V_DDR4) with V_{IN} = BUF-IN = 1.2V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.594V and a maximum of 0.606V.

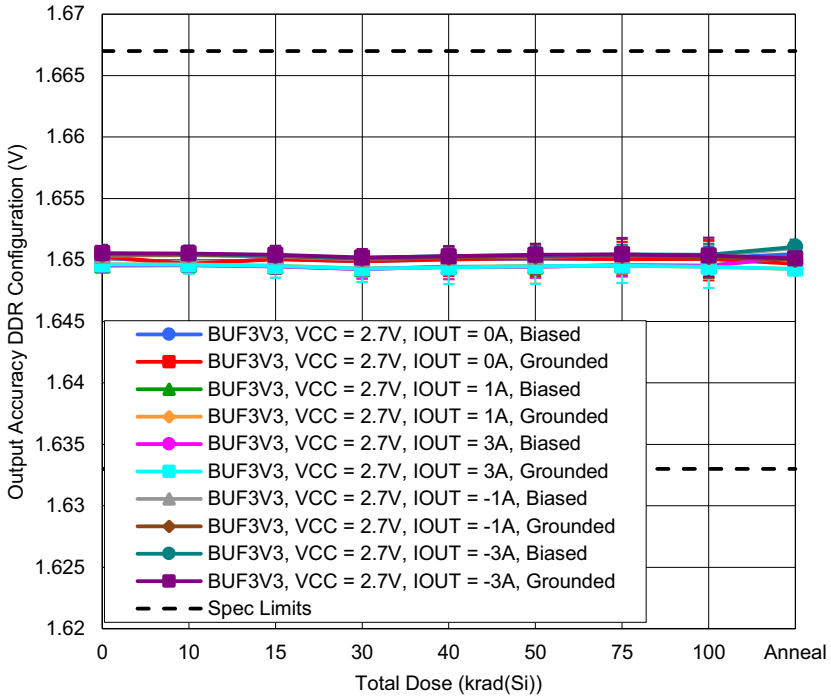


Figure 43. ISL75055SLHMF Output Accuracy DDR Configuration (BUF3V3) with V_{IN} = BUF-IN = 3.3V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1.633V and a maximum of 1.667V.

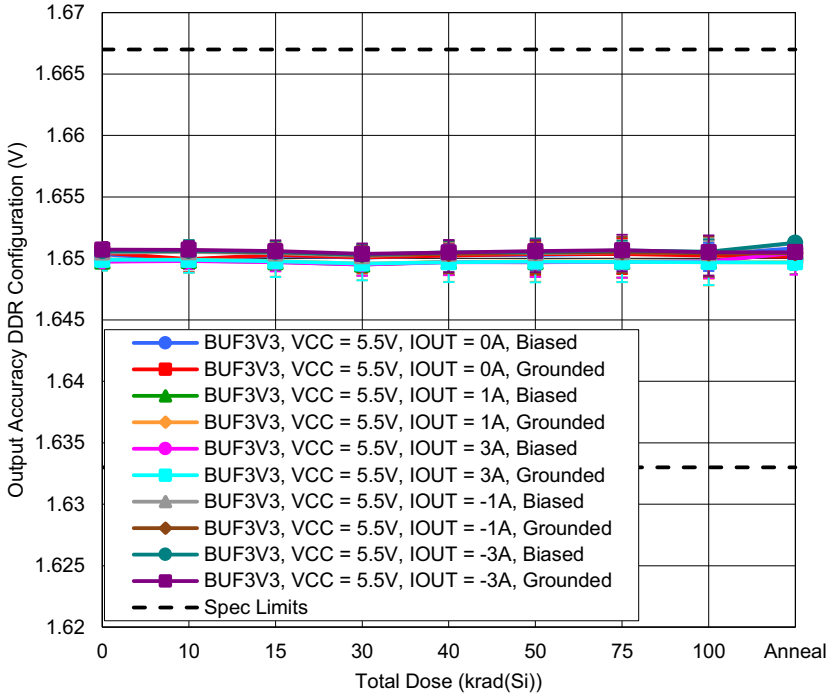


Figure 44. ISL75055SLHMF Output Accuracy DDR Configuration (BUF3V3) with V_{IN} = BUF-IN = 3.3V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1.633V and a maximum of 1.667V.

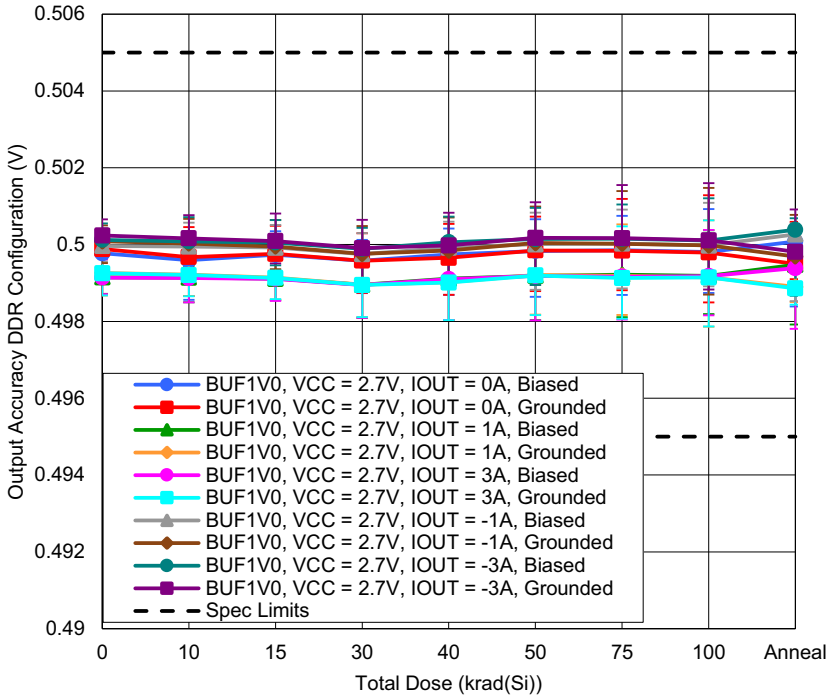


Figure 45. ISL75055SLHMF Output Accuracy DDR Configuration (BUF1V0) with V_{IN} = BUF-IN = 1.0V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.495V and a maximum of 0.505V.

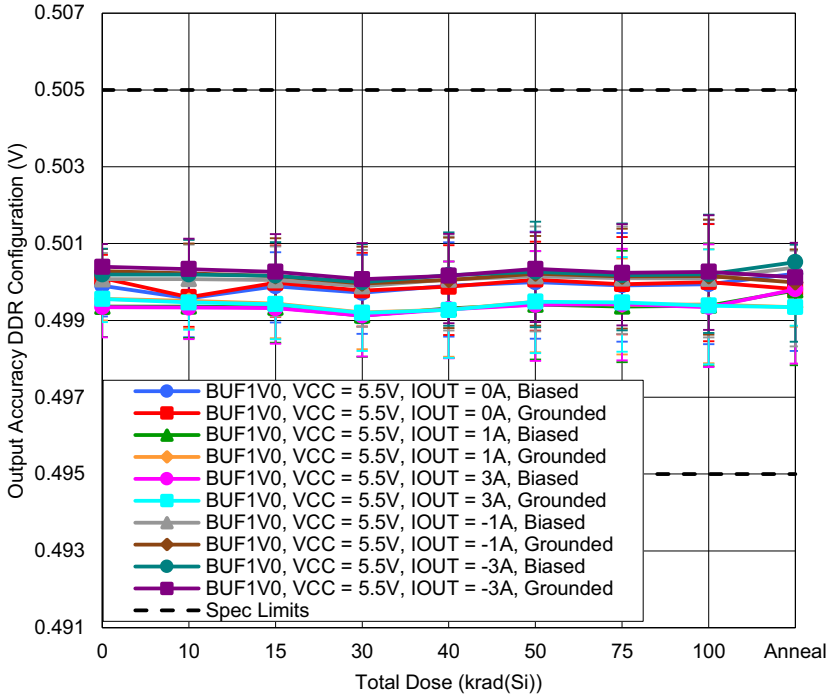


Figure 46. ISL75055SLHMF Output Accuracy DDR Configuration (BUF1V0) with V_{IN} = BUF-IN = 1.0V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.495V and a maximum of 0.505V.

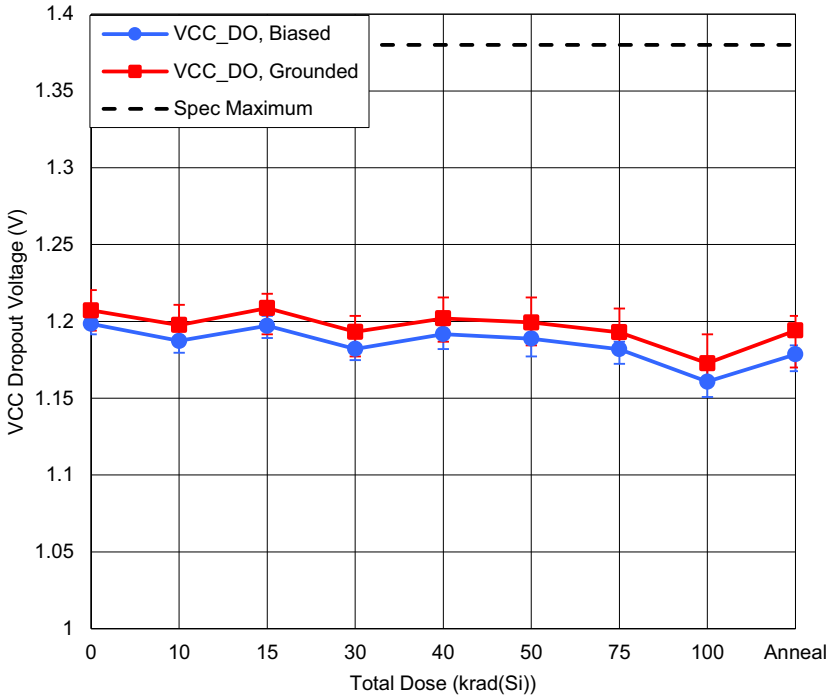


Figure 47. ISL75055SLHMF V_{CC} Dropout Voltage (VCC_DO) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 1.38V.

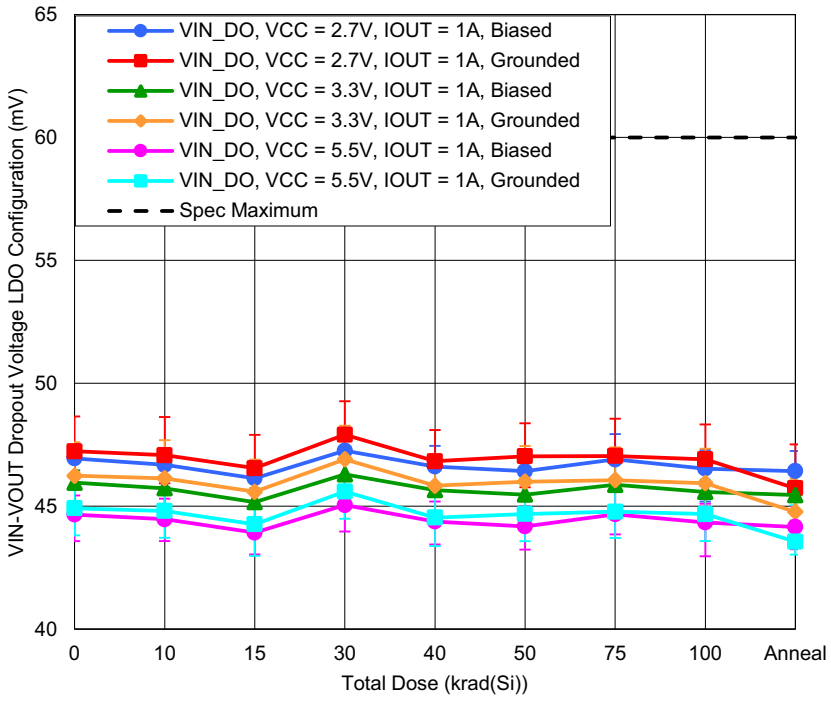


Figure 48. ISL75055SLHMF V_{IN}-V_{OUT} Dropout Voltage LDO Configuration (VIN_DO) with I_{OUT} = 1A as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 60mV.

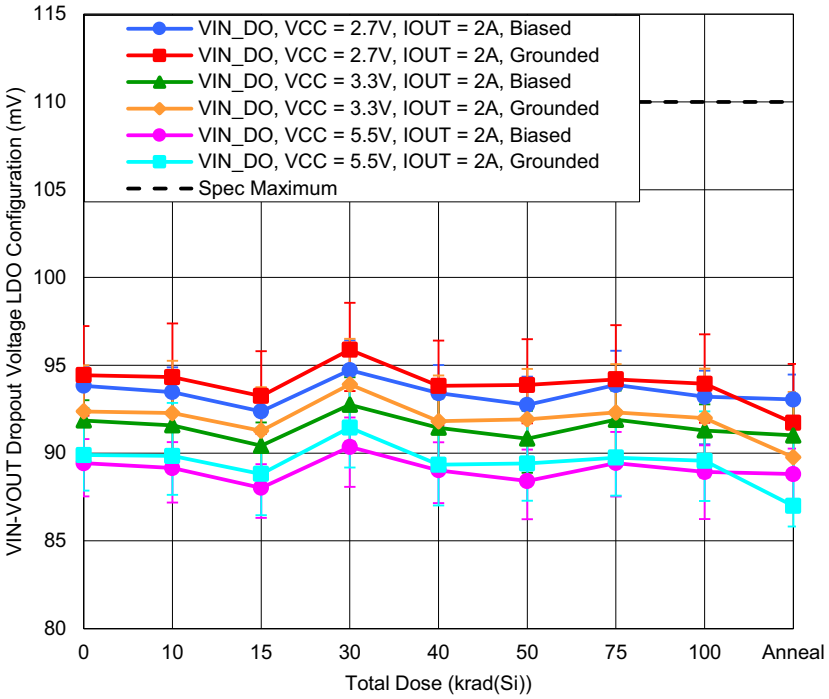


Figure 49. ISL75055SLHMF V_{IN}-V_{OUT} Dropout Voltage LDO Configuration (VIN_DO) with I_{OUT} = 2A as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 110mV.

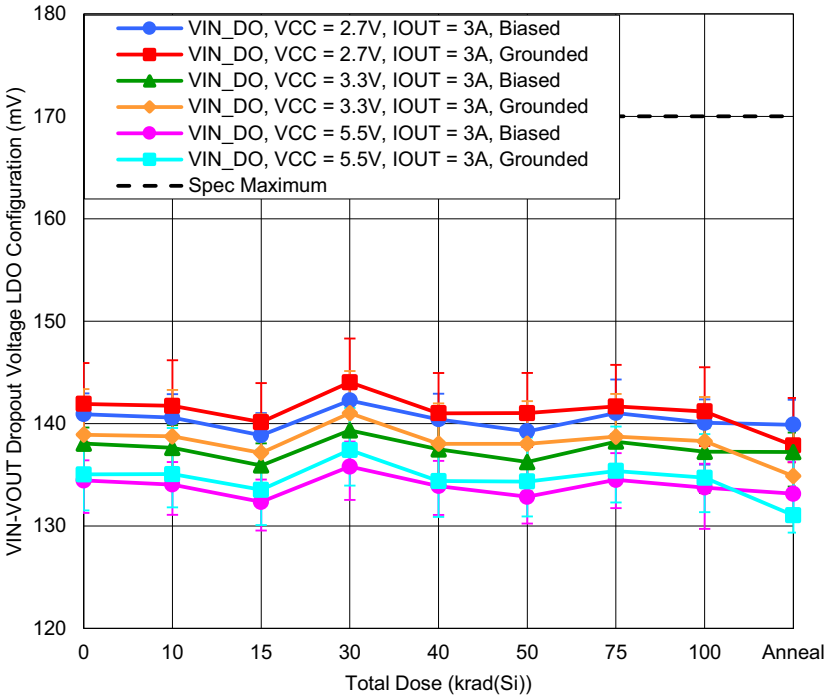


Figure 50. ISL75055SLHMF V_{IN}-V_{OUT} Dropout Voltage LDO Configuration (VIN_DO) with IOUT = 3A as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 170mV.

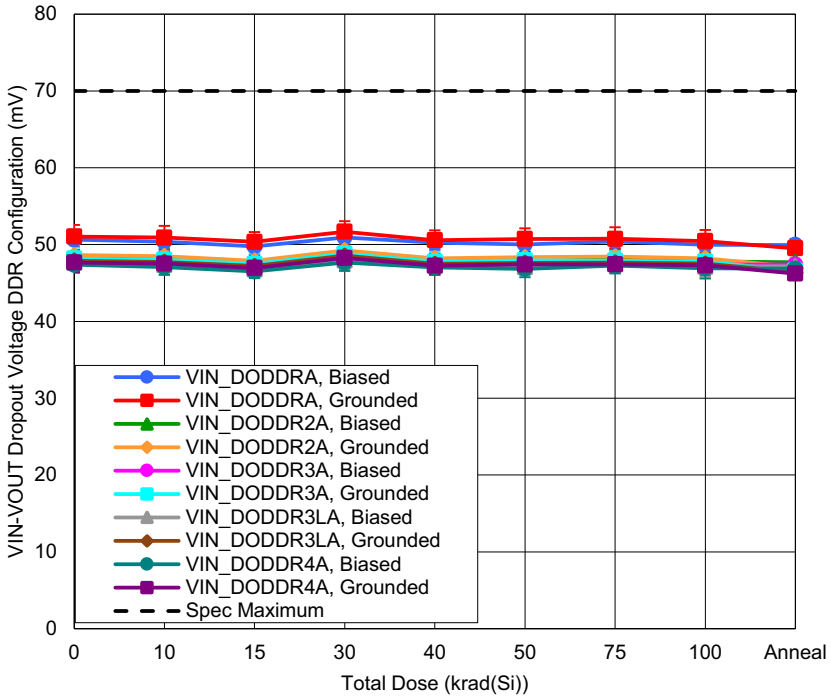


Figure 51. ISL75055SLHMF V_{IN}-V_{OUT} Dropout Voltage DDR Configuration (VIN_{DODDRA}, $VIN_{DODDR2A}$, $VIN_{DODDR3A}$, $VIN_{DODDR3LA}$, $VIN_{DODDR4A}$) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 70mV.

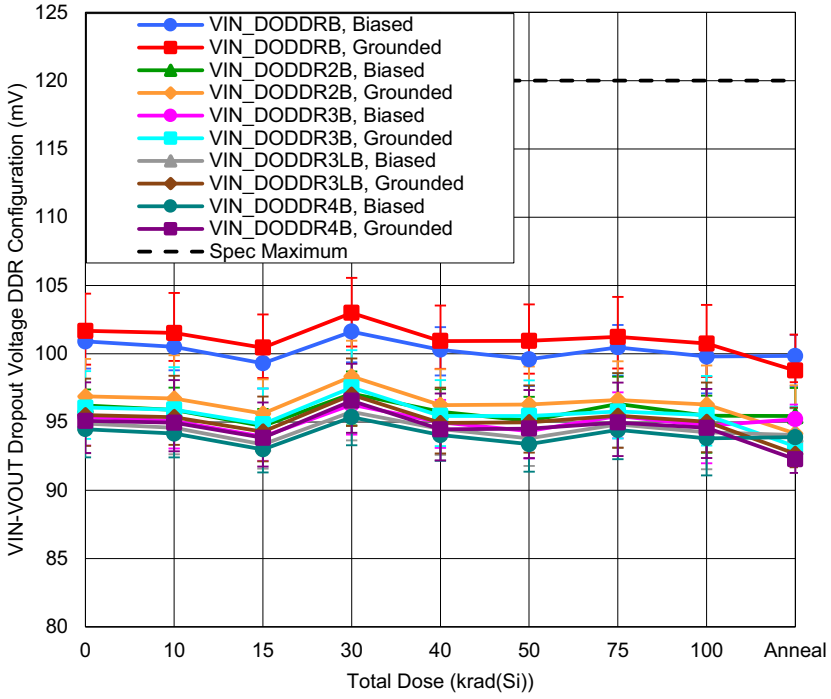


Figure 52. ISL75055SLHMF V_{IN}-V_{OUT} Dropout Voltage DDR Configuration (VIN_{DODDRB}, $VIN_{DODDR2B}$, $VIN_{DODDR3B}$, $VIN_{DODDR3LB}$, $VIN_{DODDR4B}$) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 120mV.

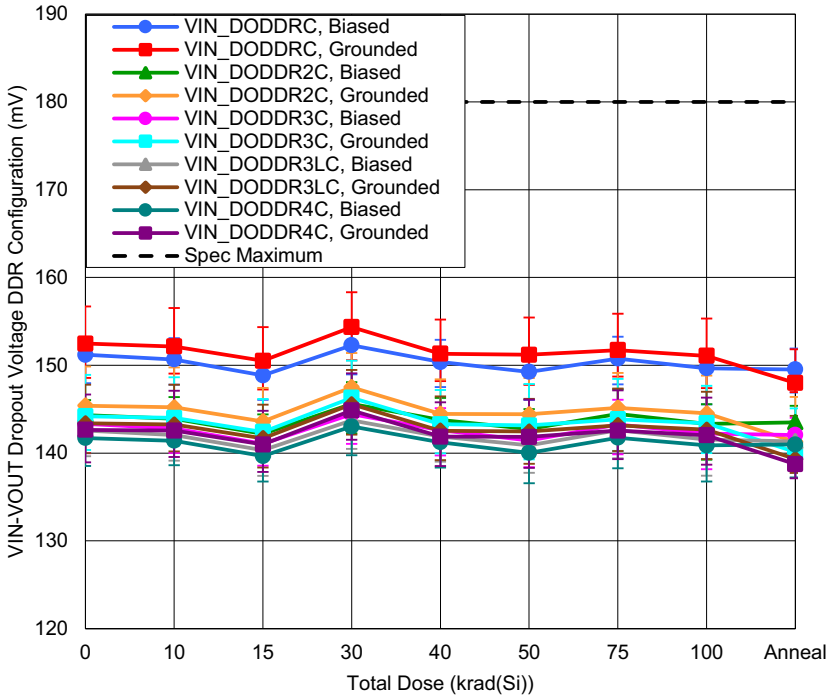


Figure 53. ISL75055SLHMF V_{IN}-V_{OUT} Dropout Voltage DDR Configuration (VIN_{DODDRC}, $VIN_{DODDR2C}$, $VIN_{DODDR3C}$, $VIN_{DODDR3LC}$, $VIN_{DODDR4C}$) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 180mV.

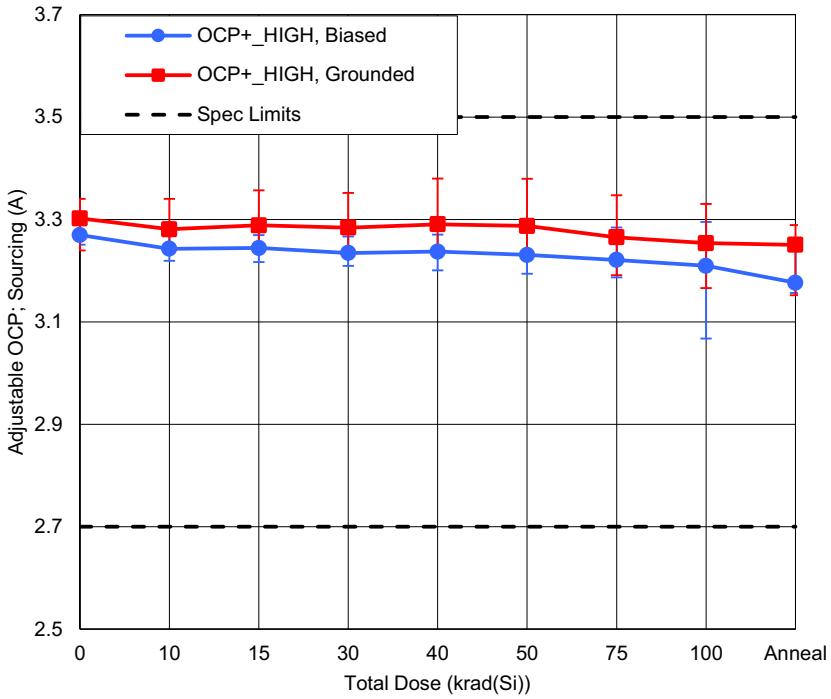


Figure 54. ISL75055SLHMF Adjustable OCP; Sourcing ($OCP+_{HIGH}$) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 2.7A and a maximum of 3.5A.

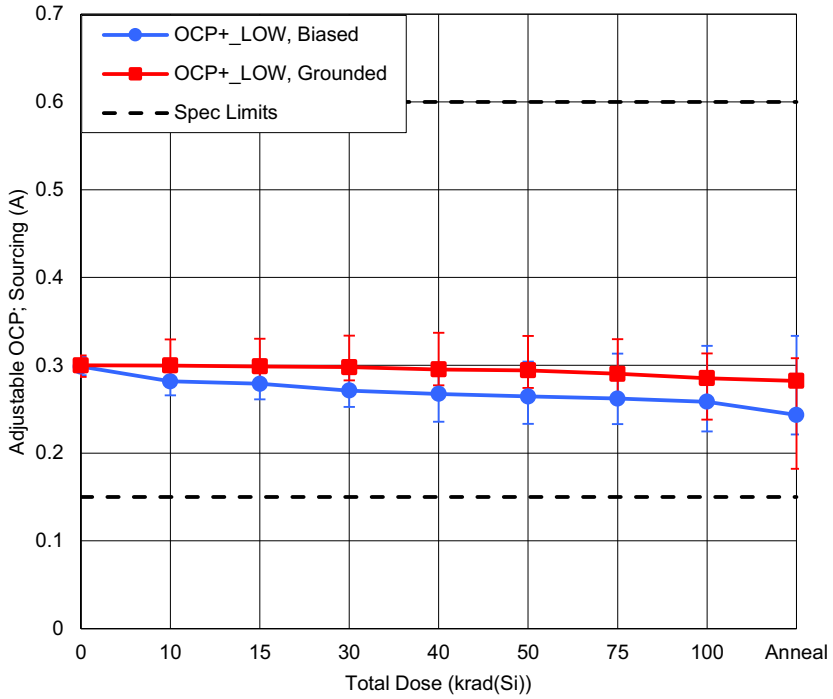


Figure 55. ISL75055SLHMF Adjustable OCP; Sourcing ($OCP+_{LOW}$) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.15A and a maximum of 0.6A.

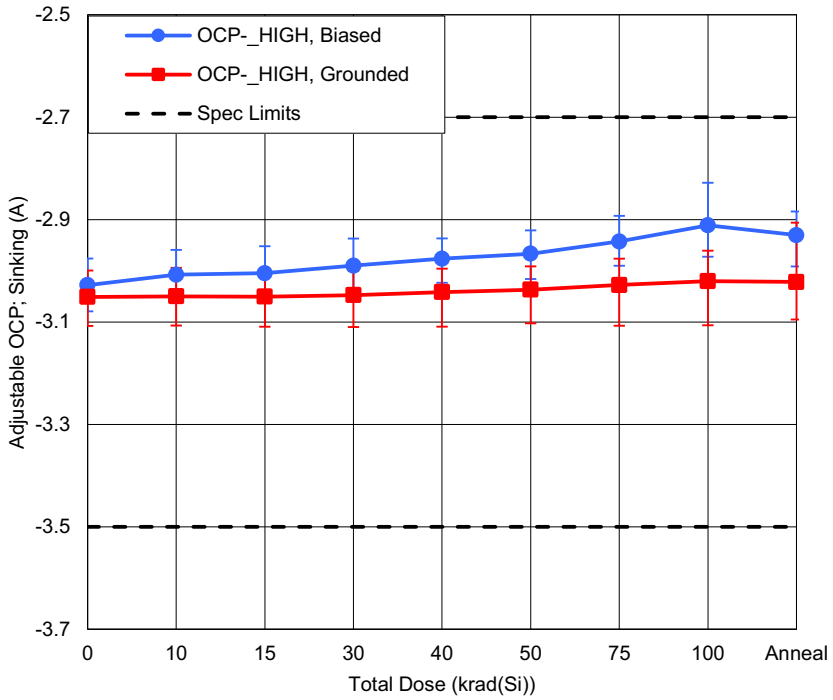


Figure 56. ISL75055SLHMF Adjustable OCP; Sinking ($OCP-_{HIGH}$) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -3.5A and a maximum of -2.7A.

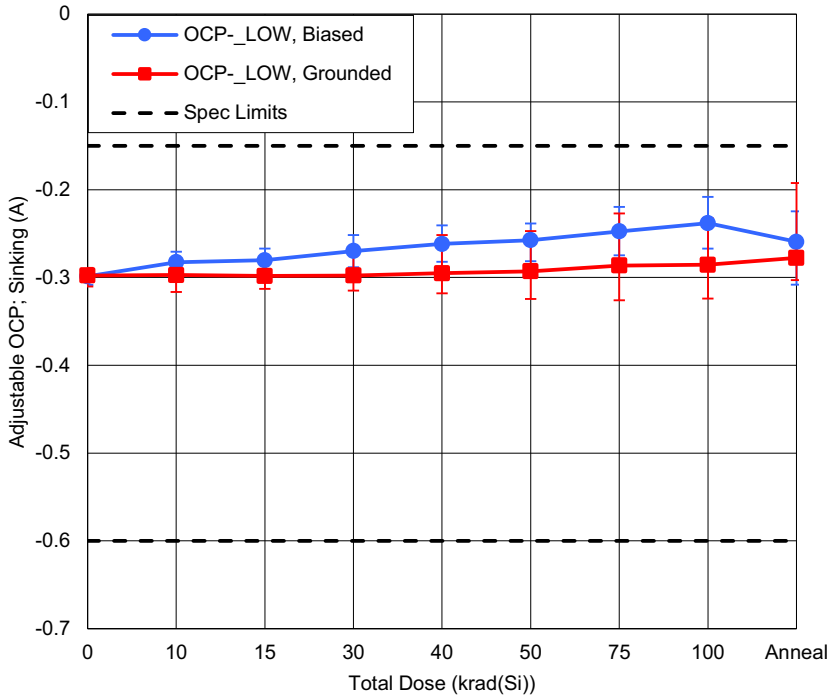


Figure 57. ISL75055SLHMF Adjustable OCP-, Sinking ($OCP-_{LOW}$) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -0.6A and a maximum of -0.15A.

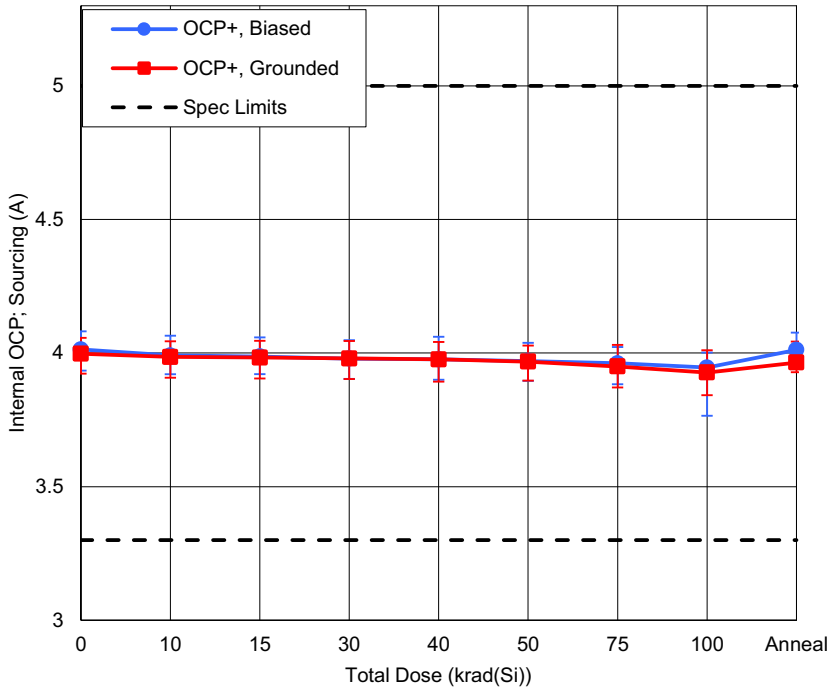


Figure 58. ISL75055SLHMF Internal OCP; Sourcing (OCP+) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 3.3A and a maximum of 5A.

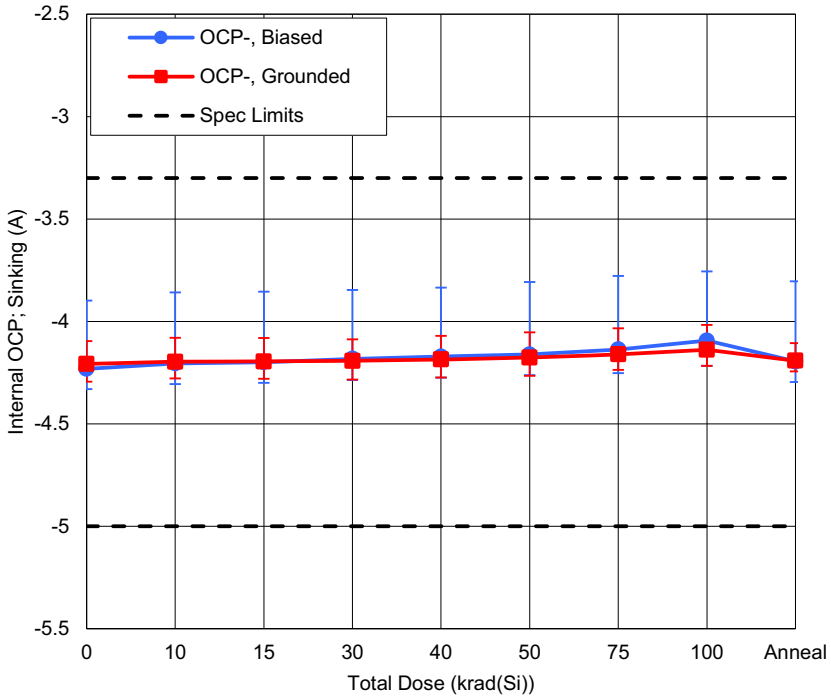


Figure 59. ISL75055SLHMF Internal OCP; Sinking (OCP-) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -5A and a maximum of -3.3A.

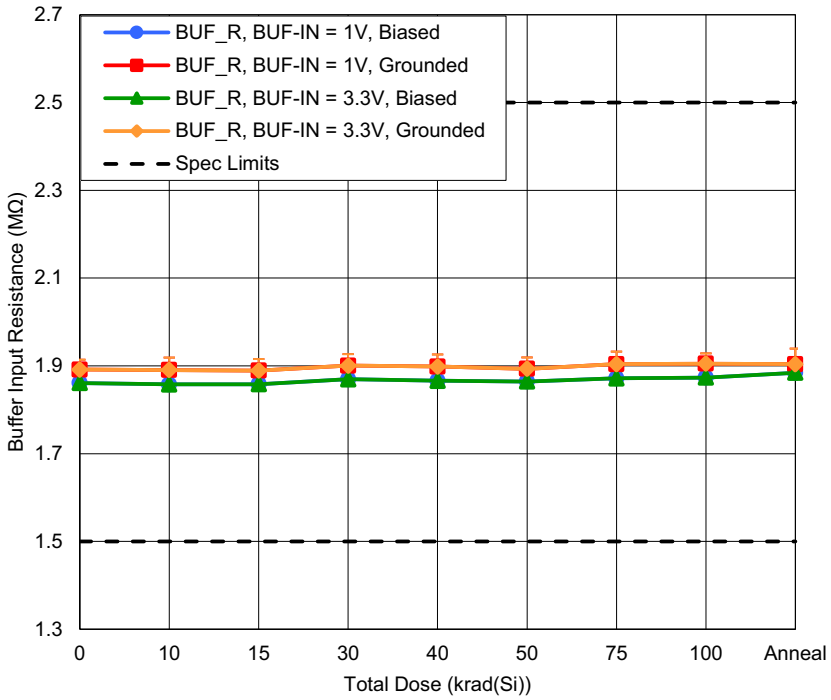


Figure 60. ISL75055SLHMF Buffer Input Resistance (BUF_R) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1.5MΩ and a maximum of 2.5MΩ.

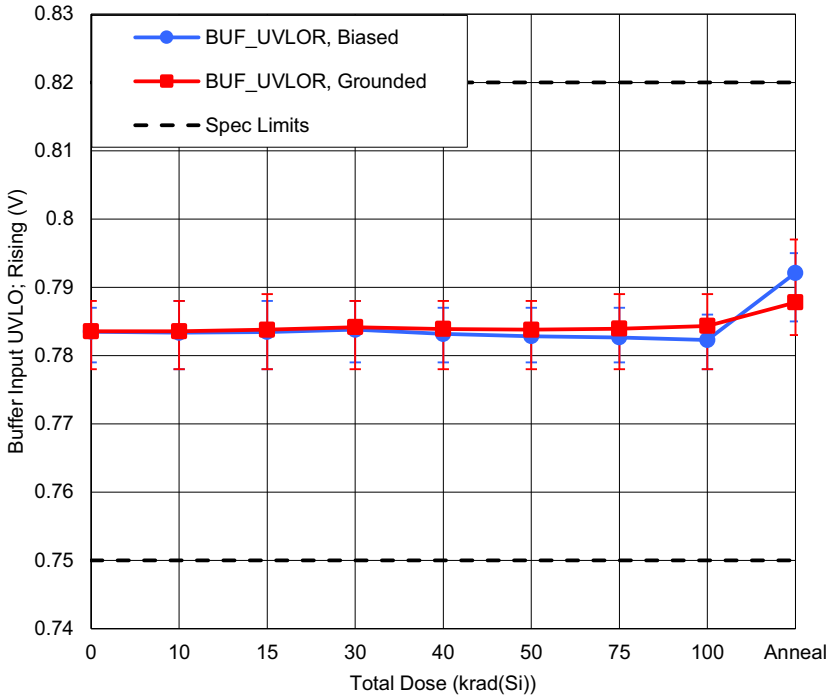


Figure 61. ISL75055SLHMF Buffer Input UVLO; Rising (BUF_{UVLOR}) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.75V and a maximum of 0.82V.

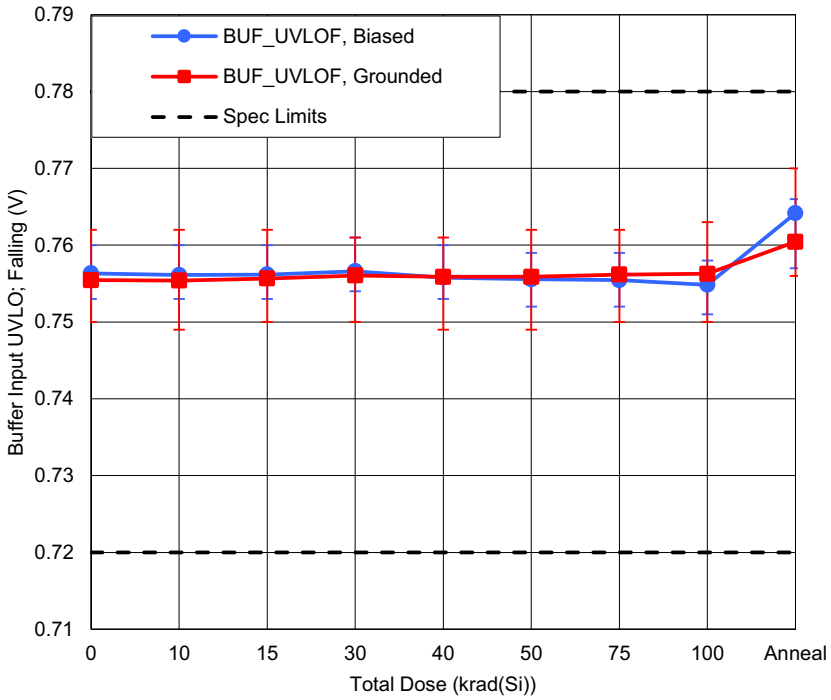


Figure 62. ISL75055SLHMF Buffer Input UVLO; Falling (BUF_{UVLOF}) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.72V and a maximum of 0.78V.

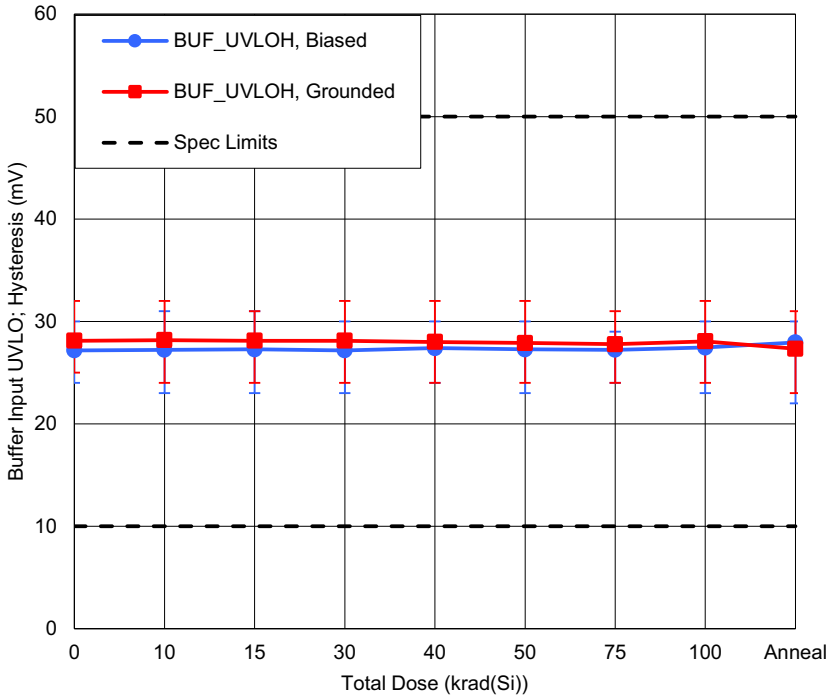


Figure 63. ISL75055SLHMF Buffer Input UVLO; Hysteresis (BUF_{UVLOH}) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 10mV and a maximum of 50mV.

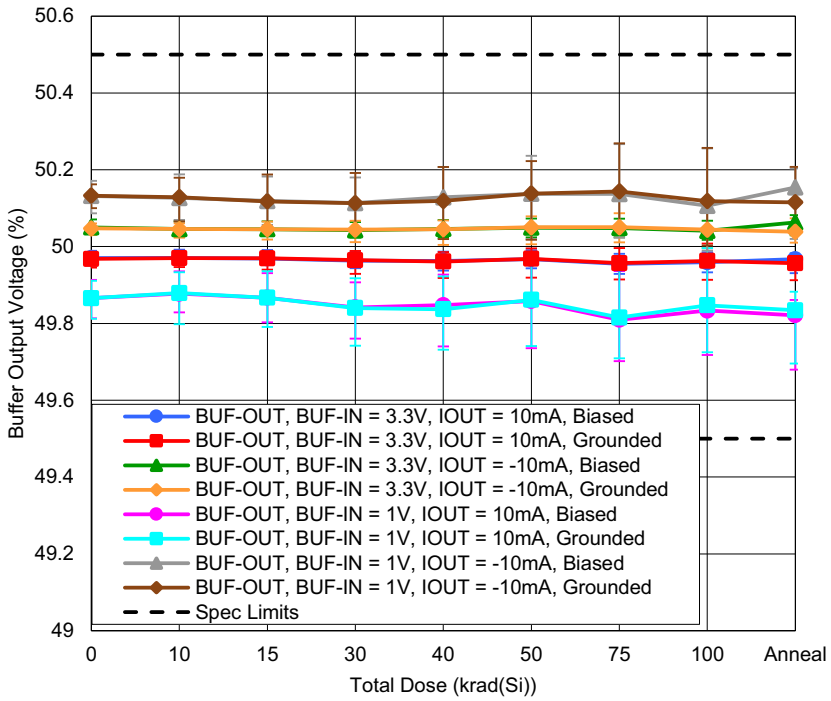


Figure 64. ISL75055SLHMF Buffer Output Voltage (BUF-OUT) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 49.5% and a maximum of 50.5%.

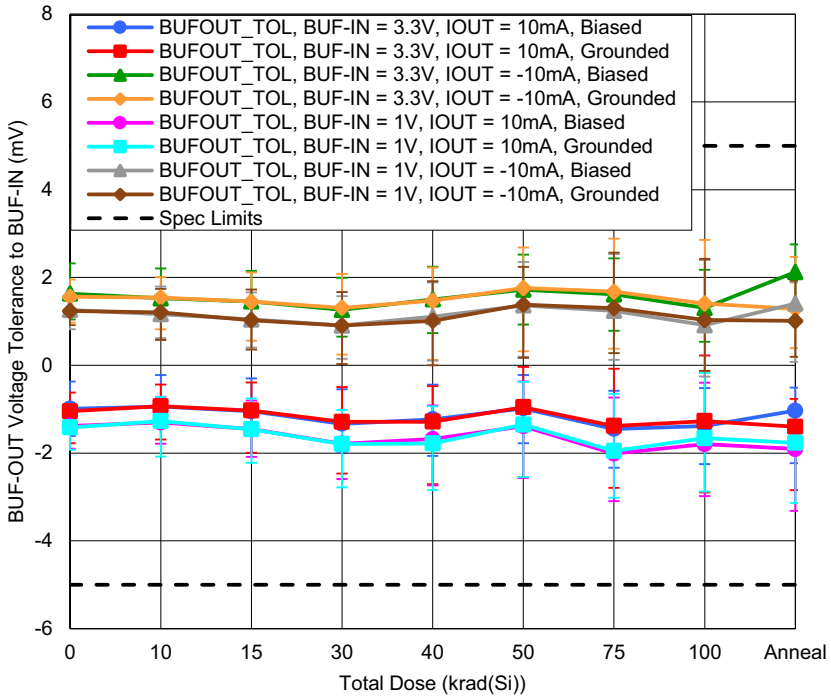


Figure 65. ISL75055SLHMF BUF-OUT Voltage Tolerance to BUF-IN ($BUFOUT_{TOL}$) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -5mV and a maximum of 5mV.

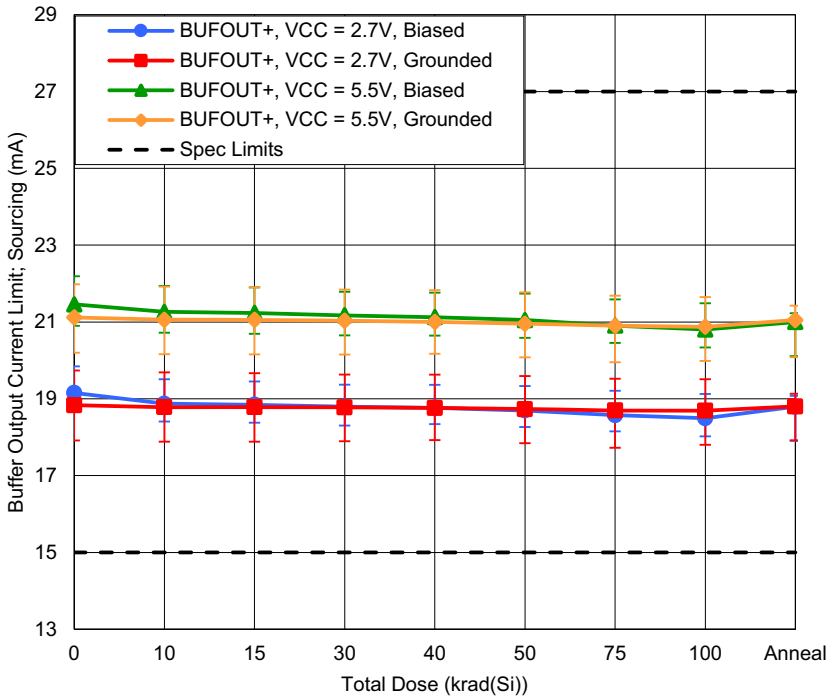


Figure 66. ISL75055SLHMF Buffer Output Current Limit; Sourcing (BUF_{OUT+}) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 15mA and a maximum of 27mA.

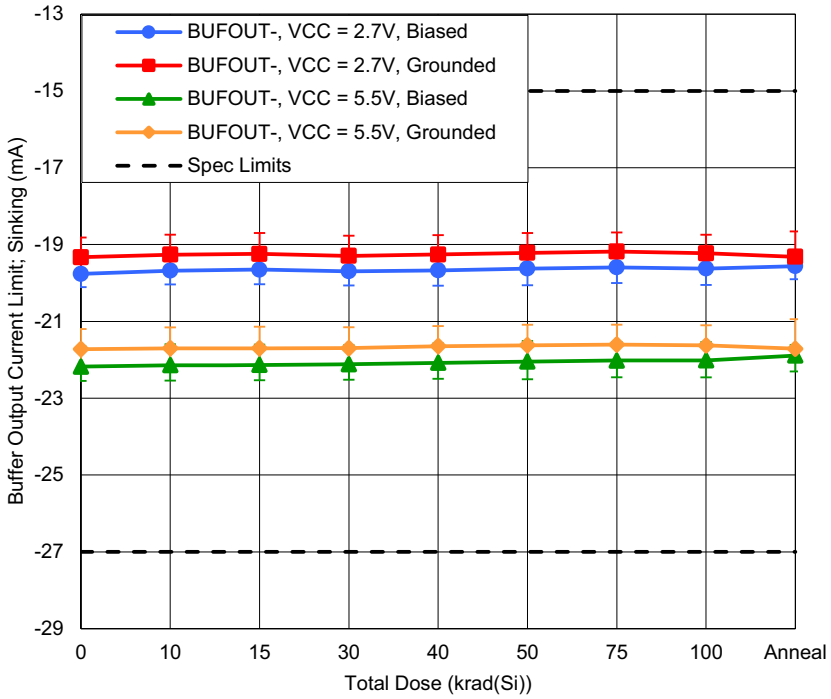


Figure 67. ISL75055SLHMF Buffer Output Current Limit; Sinking (BUF_{OUT-}) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -27mA and a maximum of -15mA.

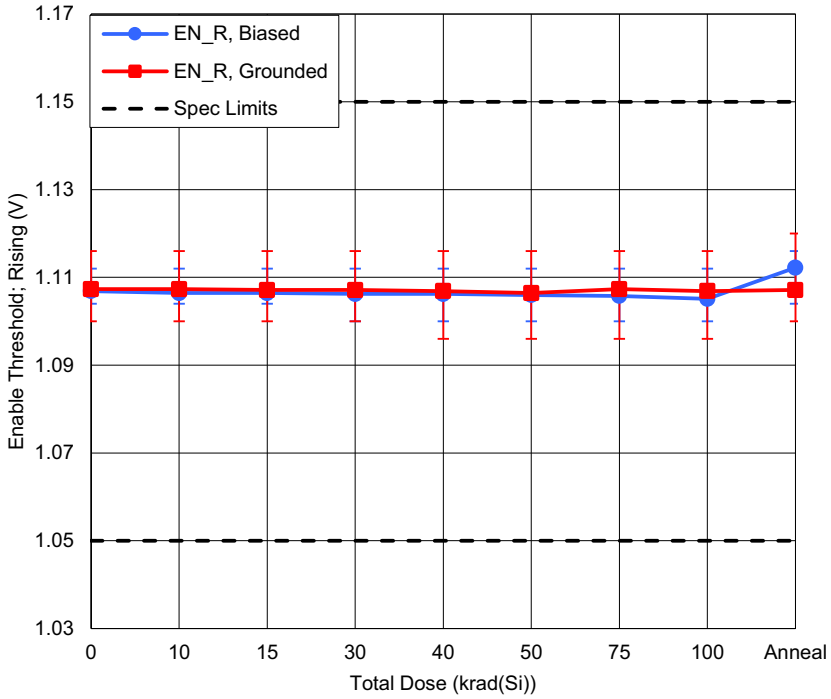


Figure 68. ISL75055SLHMF Enable Threshold; Rising (EN_R) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1.05V and a maximum of 1.15V.

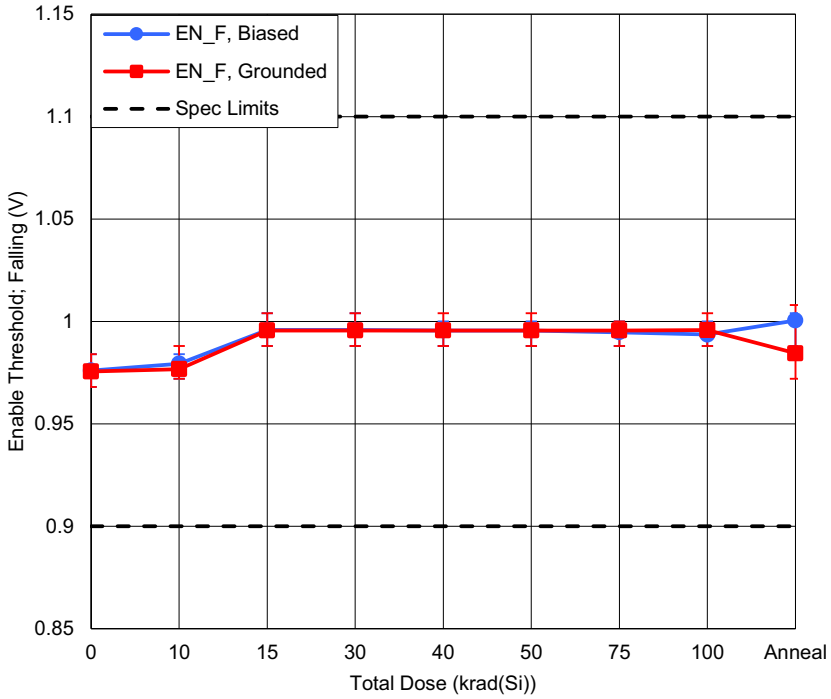


Figure 69. ISL75055SLHMF Enable Threshold; Falling (EN_F) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.9V and a maximum of 1.1V.

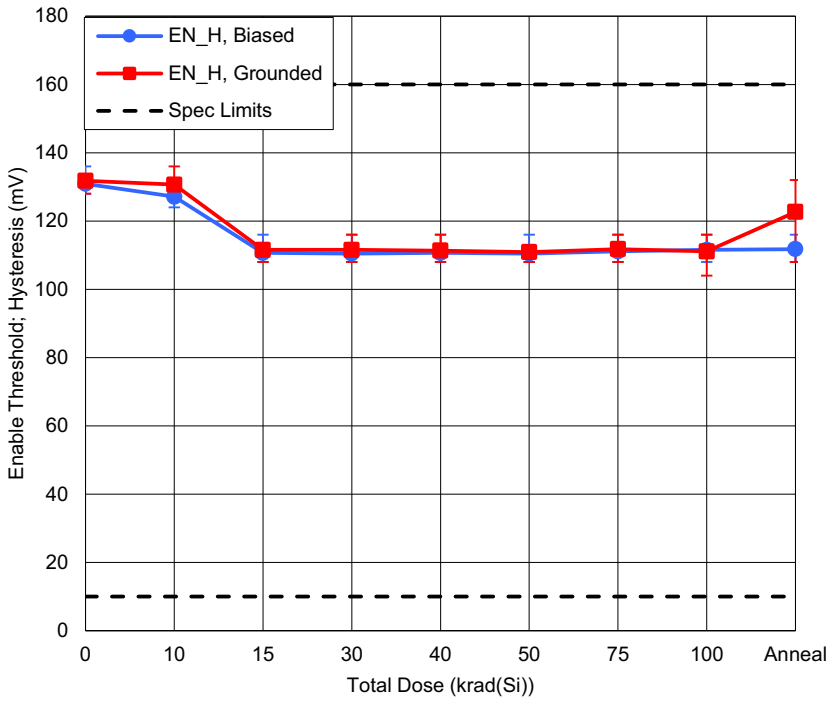


Figure 70. ISL75055SLHMF Enable Threshold; Hysteresis (EN_H) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 10mV and a maximum of 160mV.

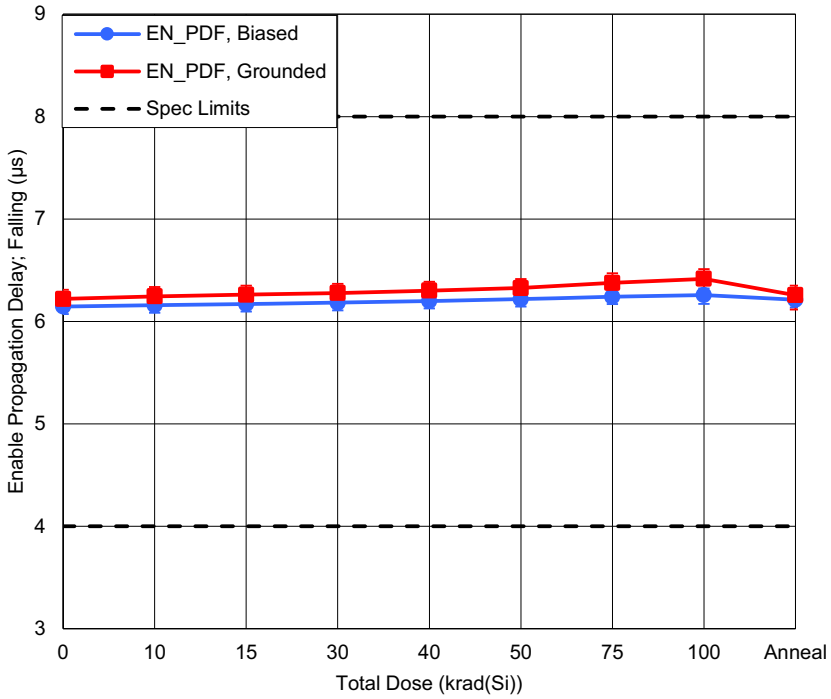


Figure 71. ISL75055SLHMF Enable Propagation Delay; Falling (EN_PDF) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 4µs and a maximum of 8µs.

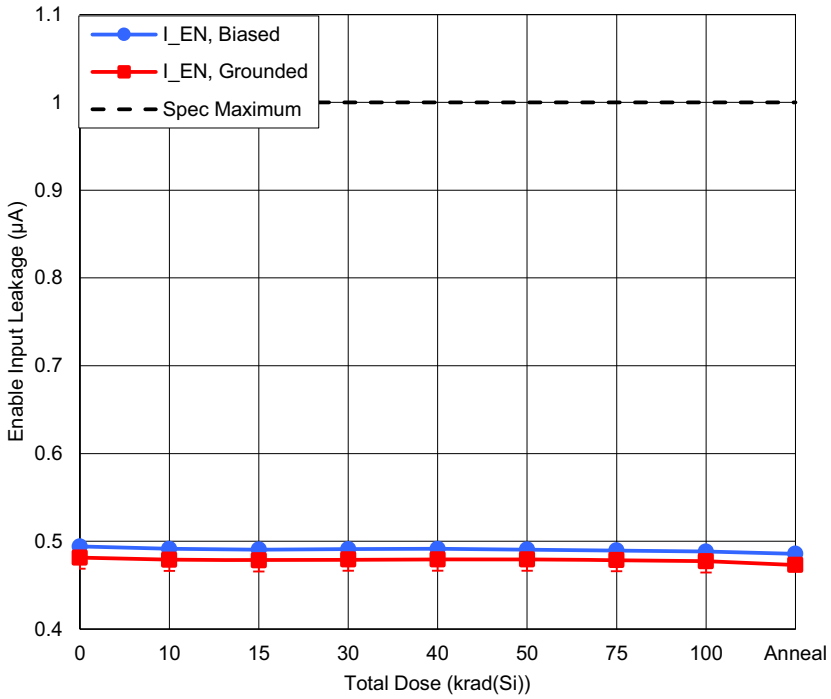


Figure 72. ISL75055SLHMF Enable Input Leakage (I_EN) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 1µA.

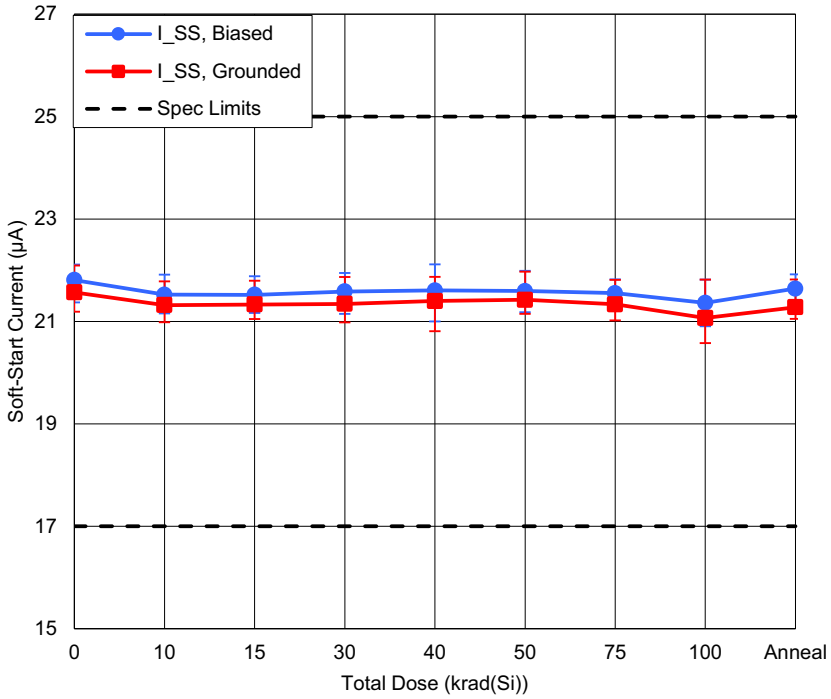


Figure 73. ISL75055SLHMF Soft-Start Current (I_SS) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 17µA and a maximum of 25µA.

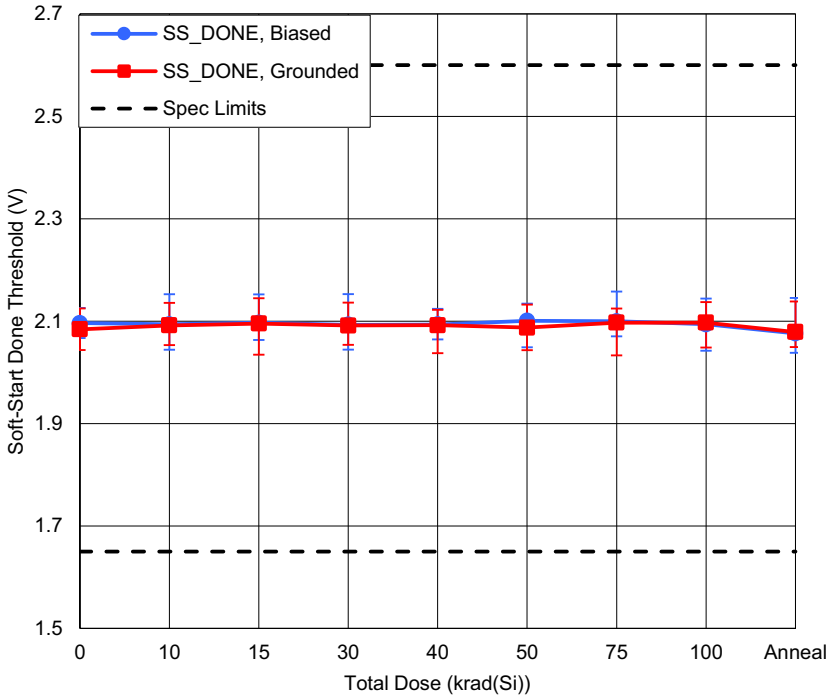


Figure 74. ISL75055SLHMF Soft-Start Done Threshold (SS_Done) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1.65V and a maximum of 2.6V.

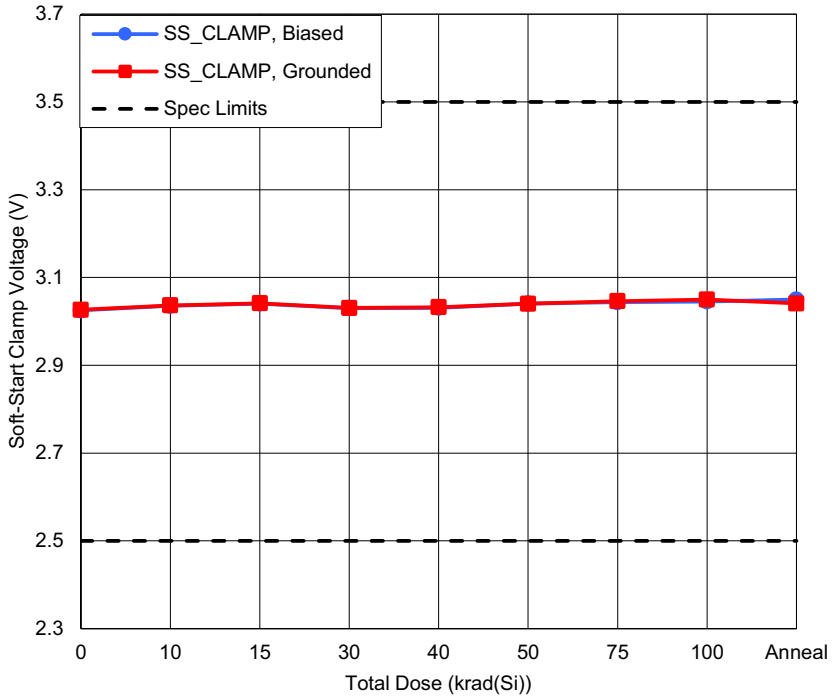


Figure 75. ISL75055SLHMF Soft-Start Clamp Voltage (SS_Clamp) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 2.5V and a maximum of 3.5V.

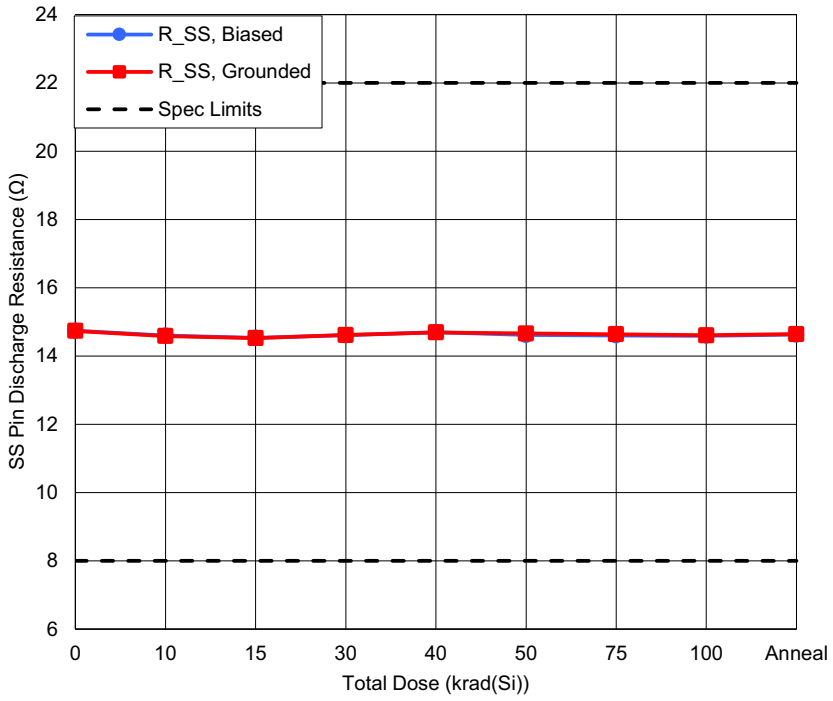


Figure 76. ISL75055SLHMF SS Pin Discharge Resistance (R_SS) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 8Ω and a maximum of 22Ω.

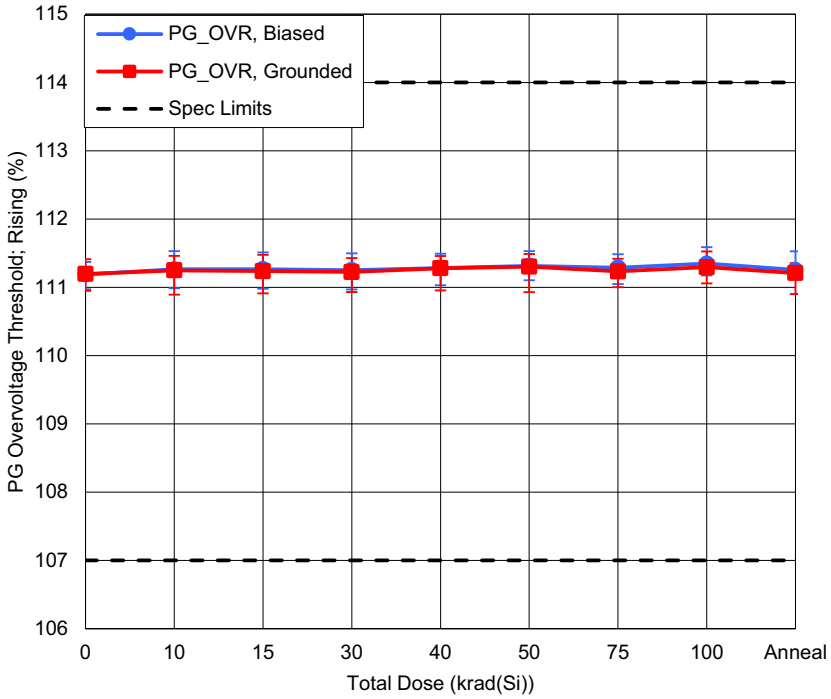


Figure 77. ISL75055SLHMF PG Overvoltage Threshold; Rising (PG_OVR) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 107% and a maximum of 114%.

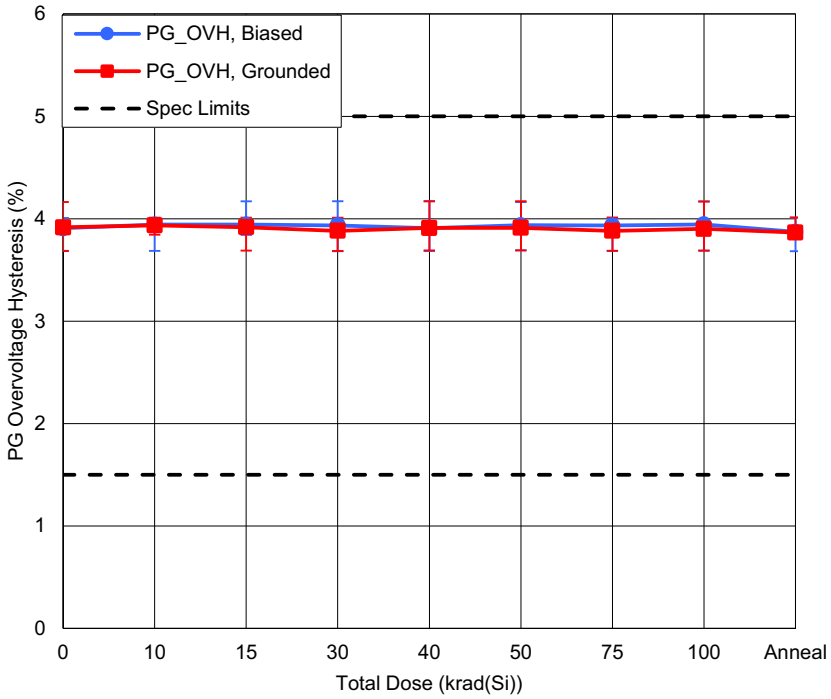


Figure 78. ISL75055SLHMF PG Overvoltage Hysteresis (PG_OVH) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1.5% and a maximum of 5%.

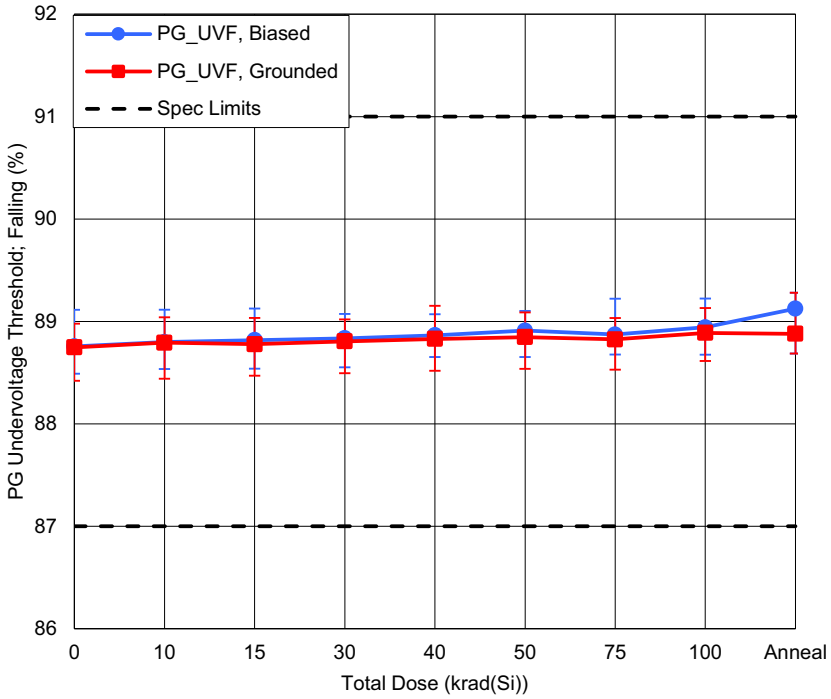


Figure 79. ISL75055SLHMF PG Undervoltage Threshold; Falling (PG_UVF) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 87% and a maximum of 91%.

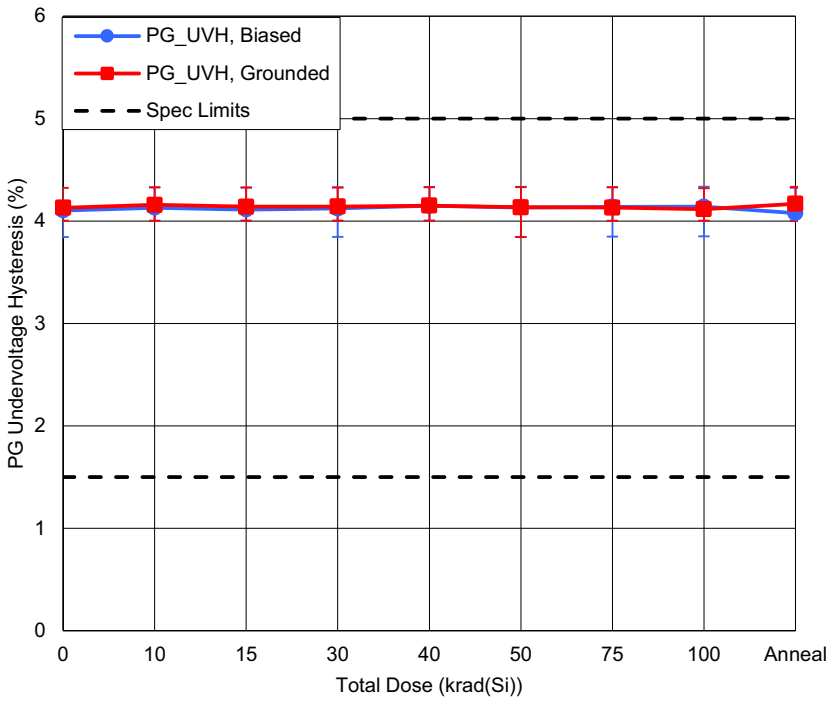


Figure 80. ISL75055SLHMF PG Undervoltage Hysteresis (PG_UVH) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1.5% and a maximum of 5%.

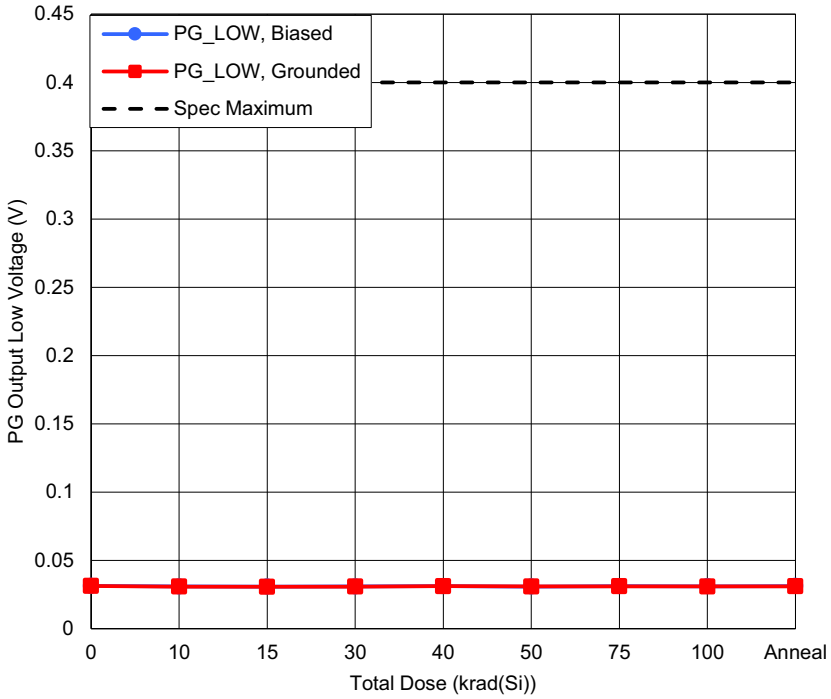


Figure 81. ISL75055SLHMF PG Output Low Voltage (PG_LOW) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 0.4V.

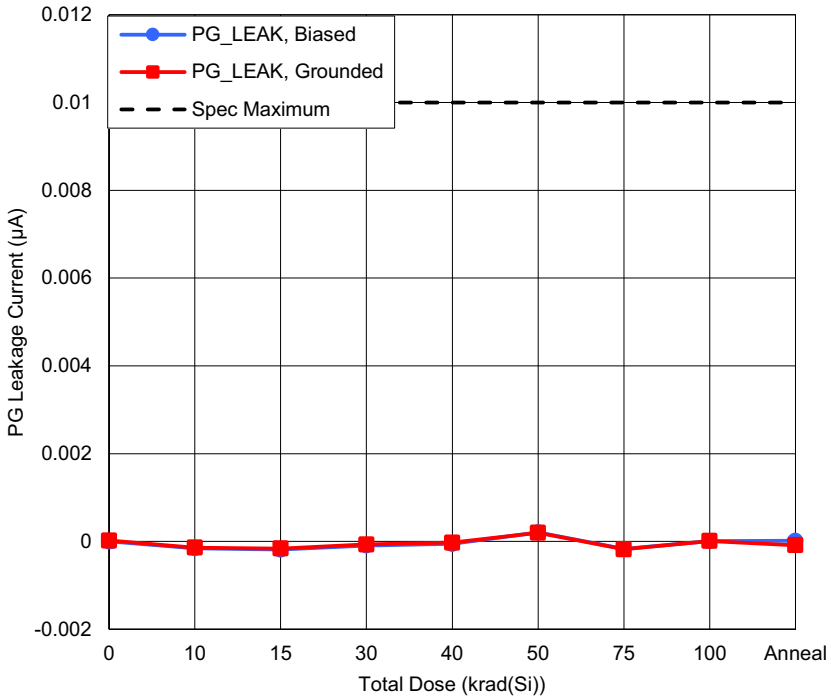


Figure 82. ISL75055SLHMF PG Leakage Current (PG_LEAK) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 0.01µA.

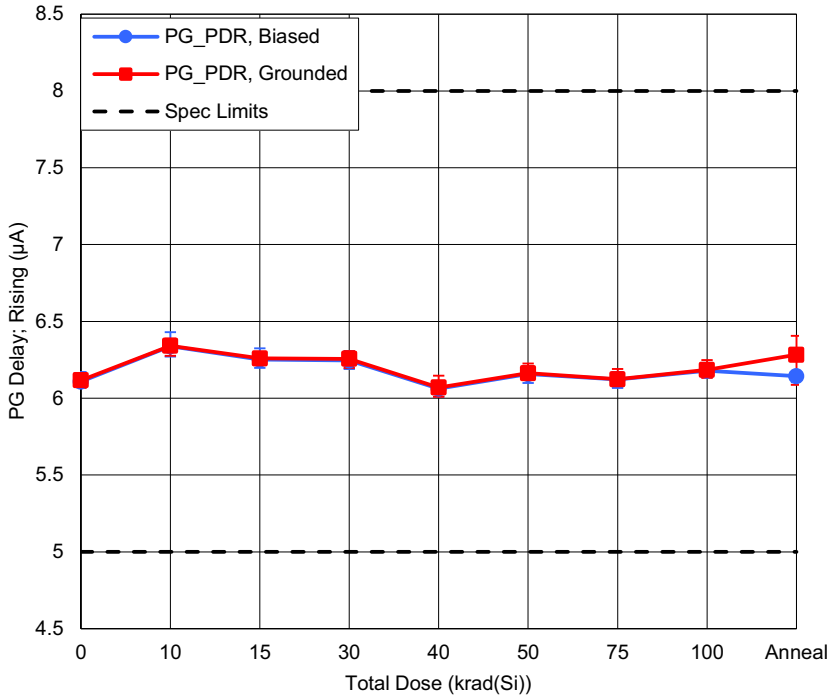


Figure 83. ISL75055SLHMF PG Delay; Rising (PG_PDR) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 5µs and a maximum of 8µs.

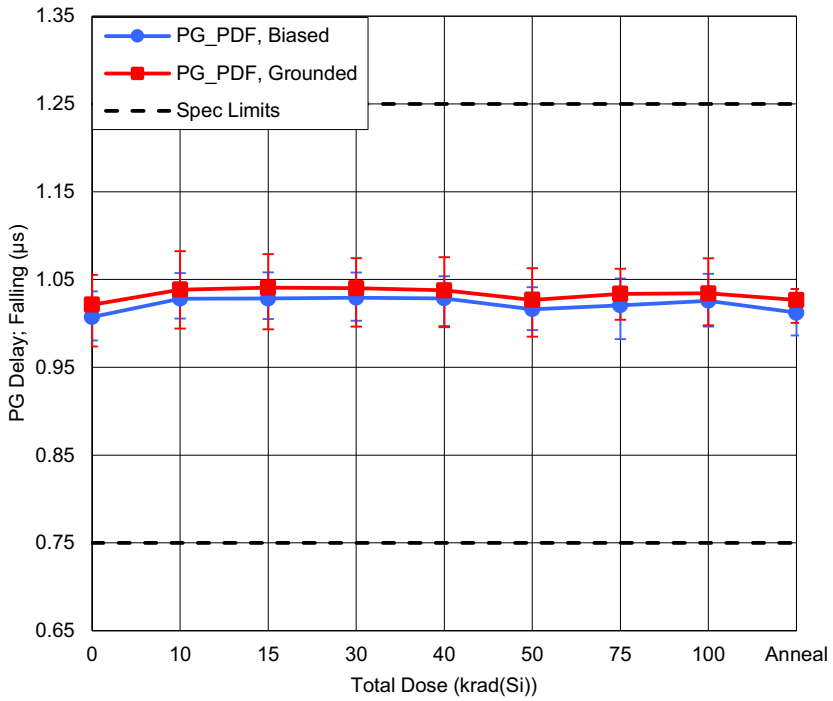


Figure 84. ISL75055SLHMF PG Delay; Falling (PG_PDF) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.75µs and a maximum of 1.25µs.

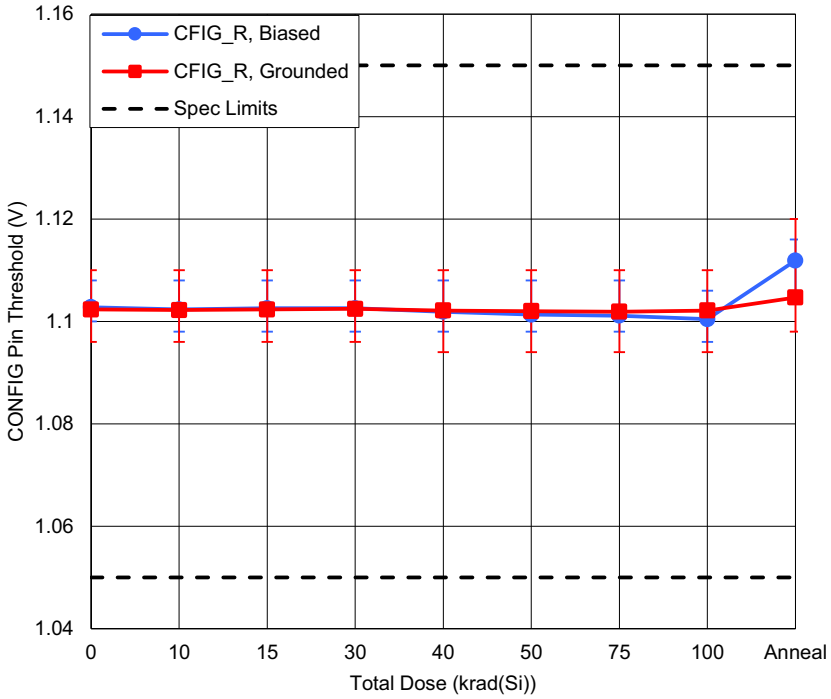


Figure 85. ISL75055SLHMF CONFIG Pin Threshold (CFIG_R) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1.05V and a maximum of 1.15V.

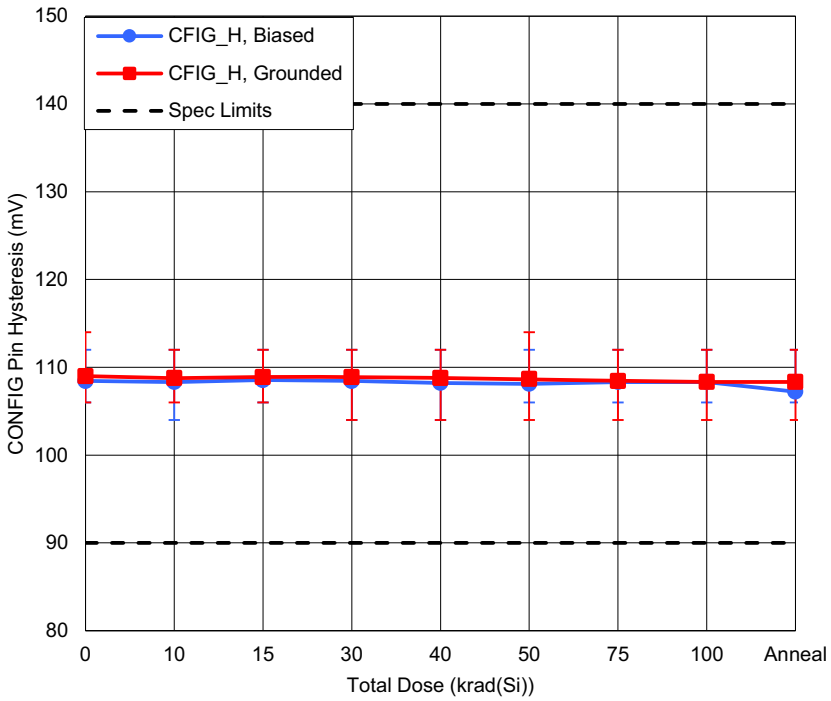


Figure 86. ISL75055SLHMF CONFIG Pin Hysteresis (CFIG_H) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 90mV and a maximum of 140mV.

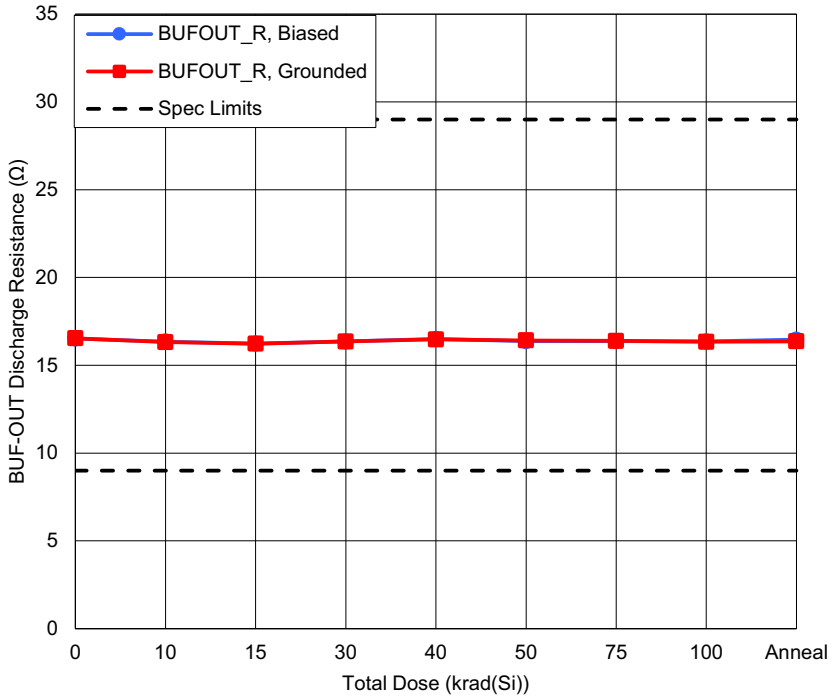


Figure 87. ISL75055SLHMF BUF-OUT Discharge Resistance (BUF-OUT_R) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 9Ω and a maximum of 29Ω.

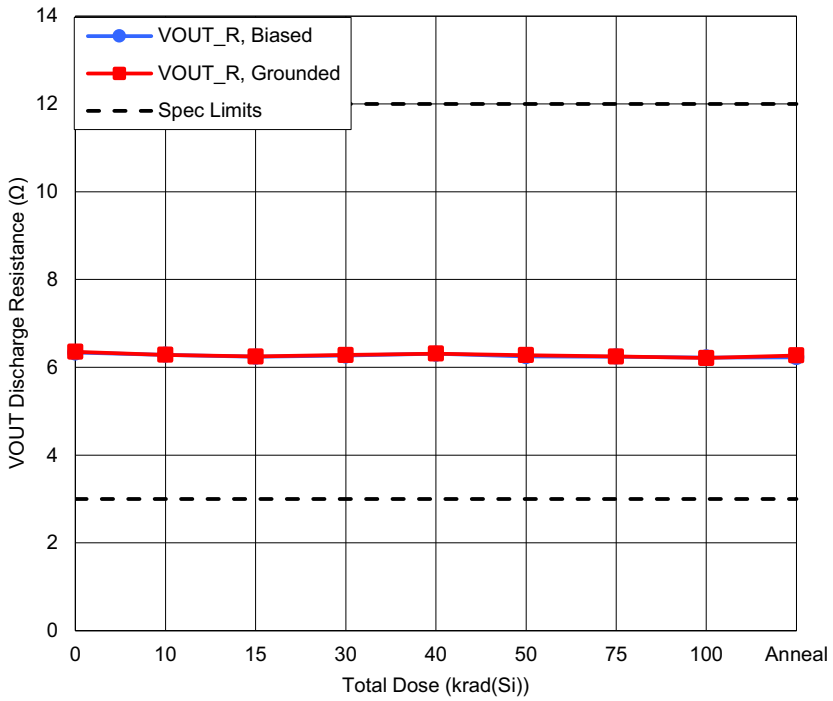


Figure 88. ISL75055SLHMF V_{OUT} Discharge Resistance (VOUT_R) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 3Ω and a maximum of 12Ω.

3. Discussion and Conclusion

This document reports the results of the LDR TID test of the ISL75055SLHMF radiation-hardened 5V, 3A source and sink LDO. The irradiation of biased and grounded samples to 100krad(Si) at a LDR of 0.01rad(Si)/s was followed by a 168-hour anneal at 100ºC under bias. All datasheet parameters passed at all downpoints. No evidence of bias dependence was observed.

4. Revision History

Revision	Date	Description
1.00	Jun 10, 2026	Initial release.

A. Appendix

Table 3 lists the datasheet parameters that are considered indicative of part performance. These parameters are plotted in Figure 3 to Figure 88. All limits are taken from the *ISL75055SLH Datasheet*, which may also have more details about the test conditions.

Table 3. ISL75055SLHMF Datasheet Total Dose Parameters (T_A = 25ºC)

Figure	Parameter	Symbol	Test Conditions	Low Limit	High Limit	Unit
3	V_{CC} Internal UVLO Rising Threshold	VCC_{UVLO_R}	V_{IN} = 3.3V, V_{OUT} = 0.5V, I_{OUT} = 0A	2.54	2.69	V
4	V_{CC} Internal UVLO Falling Threshold	VCC_{UVLO_F}	V_{IN} = 3.3V, V_{OUT} = 0.5V, I_{OUT} = 0A	2.44	2.6	V
5	V_{CC} UVLO Hysteresis	VCC_{UVLO_H}	-	90	140	mV
6	V_{CC} Enabled Supply Current	I_{VCC}	V_{CC} = 2.7V, V_{IN} = 0.75V, I_{OUT} = 0A; V_{CC} = 5.5V, V_{IN} = 5.5V, -3A < I_{OUT} < 3A; EA+ = VREF_INT; BUF - IN = 1V	2.7	7	mA
7	V_{CC} Disabled Supply Current	I_{VCC_SHDN1}	EN = 0V, V_{CC} = 5.5V, BUF-IN = 0V, EA+ = VREF_INT	120	300	µA
8	V_{CC} Disabled Supply Current	I_{VCC_SHDN2}	EN = 0V, V_{CC} = 5.5V, BUF-IN = 1V, EA+ = VREF_INT	310	1000	µA
9	V_{IN} UVLO Rising	VIN_{UVLO_R}	V_{CC} = 2.7V, BUF-IN = 1V, I_{OUT} = 0A	450	490	mV
10	V_{IN} UVLO Falling	VIN_{UVLO_F}	V_{CC} = 2.7V, BUF-IN = 1V, I_{OUT} = 0A	400	450	mV
11	V_{IN} UVLO Hysteresis	VIN_{UVLO_H}	-	10	70	mV
12	VREF_INT Voltage	V_{REF}	V_{IN} = 3.3V, EA+ = VREF_INT	492.5	507.5	mV
13	Error Amplifier V_{OS}	EA_VOS	V_{CC} = 3.3V, V_{IN} = 0.8V, I_{OUT} = 0A	-2.2	2.2	mV
14			V_{CC} = 2.7V, V_{IN} = 0.8V, I_{OUT} = 0A, 3A, -3A	-2.2	2.2	mV
15			V_{CC} = 5.5V, V_{IN} = 0.8V, I_{OUT} = 0A, 3A, -3A	-2.2	2.2	mV
16			V_{CC} = 2.7V, V_{IN} = 5.5V, I_{OUT} = 0A, 3A, -3A	-2.2	2.2	mV
17			V_{CC} = 5.5V, V_{IN} = 5.5V, I_{OUT} = 0A, 3A, -3A	-2.2	2.2	mV
18	Regulator Dead-Band	DBand	Change in Error Amp VOS from I_{OUT} = -1mA to I_{OUT} = 1mA	300	900	µV
19	EA+; EA- Input Bias Current	I_EA+; I_EA-	EA+ = EA- = 0.5V, V_{CC} = 3.3V, V_{IN} = 3.3V	-	0.35	µA
20	Output Accuracy	VOUT%	V_{IN} = 0.75V, V_{CC} = 2.7V, V_{OUT} = 0.5V, I_{OUT} = 0A, 3A, -3A	-1.5	1.5	%
21			V_{IN} = 5.5V, V_{CC} = 2.7V, V_{OUT} = 0.5V, I_{OUT} = 0A, 3A, -3A	-1.5	1.5	%
22			V_{IN} = 0.75V, V_{CC} = 5.5V, V_{OUT} = 0.5V, I_{OUT} = 0A, 3A, -3A	-1.5	1.5	%
23			V_{IN} = 0.75V, V_{CC} = 2.7V, V_{OUT} = 0.5V, I_{OUT} = 0A, 3A, -3A	-1.5	1.5	%
24			V_{IN} = 1.5V, V_{CC} = 2.7V, V_{OUT} = 1.2V, I_{OUT} = 0A, 3A, -3A	-1.5	1.5	%
25			V_{IN} = 0.75V, V_{CC} = 2.7V, V_{OUT} = 0.5V, I_{OUT} = 0A, 3A, -3A	-1.5	1.5	%
26			V_{IN} = 2.1V, V_{CC} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 0A, 3A, -3A	-1.5	1.5	%
27			V_{IN} = 5.5V, V_{CC} = 5.5V, V_{OUT} = 1.8V, I_{OUT} = 0A, 3A, -3A	-1.5	1.5	%
28			V_{IN} = 3.6V, V_{CC} = 4.8V, V_{OUT} = 3.3V, I_{OUT} = 0A, 3A, -3A	-1.5	1.5	%
29			V_{IN} = 5.5V, V_{CC} = 5.5V, V_{OUT} = 3.3V, I_{OUT} = 0A, 3A, -3A	-1.5	1.5	%
30	Line Regulation	$VOUT_{LINE}$	0.75V < VIN < 5.5V, EA+ = VREF_INT VOUT = 0.5V, 1.2V, 1.8V, 3.3V	-0.16	0.16	%/V

Table 3. ISL75055SLHMF Datasheet Total Dose Parameters (T_A = 25ºC) (Cont.)

Figure	Parameter	Symbol	Test Conditions	Low Limit	High Limit	Unit
31	Sourcing Load Regulation	V_{OUT_LOAD1}	V_{IN} = 0.75V and 5.5V, EA+ = VREF_INT V_{OUT} = 0.5V, 1.2V, 1.8V, 3.3V	-0.15	-	%/A
32	Sinking Load Regulation	V_{OUT_LOAD2}	V_{IN} = 0.75V and 5.5V, EA+ = VREF_INT V_{OUT} = 0.5V, 1.2V, 1.8V, 3.3V	-	0.20	%/A
33	Output Accuracy DDR Configuration	V_DDR	V_{IN} = BUF-IN = 2.5V, V_{CC} = 2.7V	1.237	1.263	V
34			V_{IN} = BUF-IN = 2.5V, V_{CC} = 5.5V	1.237	1.263	V
35		V_DDR2	V_{IN} = BUF-IN = 1.8V, V_{CC} = 2.7V	0.891	0.909	V
36			V_{IN} = BUF-IN = 1.8V, V_{CC} = 5.5V	0.891	0.909	V
37		V_DDR3	V_{IN} = BUF-IN = 1.5V, V_{CC} = 2.7V	0.742	0.758	V
38			V_{IN} = BUF-IN = 1.5V, V_{CC} = 5.5V	0.742	0.758	V
39		V_DDR3L	V_{IN} = BUF-IN = 1.35V, V_{CC} = 2.7V	0.668	0.682	V
40			V_{IN} = BUF-IN = 1.35V, V_{CC} = 5.5V	0.668	0.682	V
41		V_DDR4	V_{IN} = BUF-IN = 1.2V, V_{CC} = 2.7V	0.594	0.606	V
42			V_{IN} = BUF-IN = 1.2V, V_{CC} = 5.5V	0.594	0.606	V
43		BUF3V3	V_{IN} = BUF-IN = 3.3V, V_{CC} = 2.7V	1.633	1.667	V
44			V_{IN} = BUF-IN = 3.3V, V_{CC} = 5.5V	1.633	1.667	V
45		BUF1V0	V_{IN} = BUF-IN = 1.0V, V_{CC} = 2.7V	0.495	0.505	V
46			V_{IN} = BUF-IN = 1.0V, V_{CC} = 5.5V	0.495	0.505	V
47	V_{CC} Dropout Voltage	VCC_DO	I_{OUT} = 3A, V_{OUT} = 3.3V, V_{IN} = 3.6V	-	1.38	V
48	V_{IN}-V_{OUT} Dropout Voltage LDO Configuration	VIN_DO	I_{OUT} = 1A	-	60	mV
49			I_{OUT} = 2A	-	110	mV
50			I_{OUT} = 3A	-	170	mV
51	V_{IN}-V_{OUT} Dropout Voltage DDR Configuration	VIN_{DODDRA}	V_{CC} = 2.7V, BUF-IN = 2.5V, V_{IN} = 1.25V, I_{OUT} = 1A	-	70	mV
		$VIN_{DODDR2A}$	V_{CC} = 2.7V, BUF-IN = 1.8V, V_{IN} = 0.9V, I_{OUT} = 1A	-	70	mV
		$VIN_{DODDR3A}$	V_{CC} = 2.7V, BUF-IN = 1.5V, V_{IN} = 0.75V, I_{OUT} = 1A	-	70	mV
		$VIN_{DODDR3LA}$	V_{CC} = 2.7V, BUF-IN = 1.35V, V_{IN} = 0.675V, I_{OUT} = 1A	-	70	mV
		$VIN_{DODDR4A}$	V_{CC} = 2.7V, BUF-IN = 1.2V, V_{IN} = 0.6V, I_{OUT} = 1A	-	70	mV
52		VIN_{DODDRB}	V_{CC} = 2.7V, BUF-IN = 2.5V, V_{IN} = 1.25V, I_{OUT} = 2A	-	120	mV
		$VIN_{DODDR2B}$	V_{CC} = 2.7V, BUF-IN = 1.8V, V_{IN} = 0.9V, I_{OUT} = 2A	-	120	mV
		$VIN_{DODDR3B}$	V_{CC} = 2.7V, BUF-IN = 1.5V, V_{IN} = 0.75V, I_{OUT} = 2A	-	120	mV
		$VIN_{DODDR3LB}$	V_{CC} = 2.7V, BUF-IN = 1.35V, V_{IN} = 0.675V, I_{OUT} = 2A	-	120	mV
		$VIN_{DODDR4B}$	V_{CC} = 2.7V, BUF-IN = 1.2V, V_{IN} = 0.6V, I_{OUT} = 2A	-	120	mV
53		VIN_{DODDRC}	V_{CC} = 2.7V, BUF-IN = 2.5V, V_{IN} = 1.25V, I_{OUT} = 3A	-	180	mV
		$VIN_{DODDR2C}$	V_{CC} = 2.7V, BUF-IN = 1.8V, V_{IN} = 0.9V, I_{OUT} = 3A	-	180	mV
		$VIN_{DODDR3C}$	V_{CC} = 2.7V, BUF-IN = 1.5V, V_{IN} = 0.75V, I_{OUT} = 3A	-	180	mV
		$VIN_{DODDR3LC}$	V_{CC} = 2.7V, BUF-IN = 1.35V, V_{IN} = 0.675V, I_{OUT} = 3A	-	180	mV
		$VIN_{DODDR4C}$	V_{CC} = 2.7V, BUF-IN = 1.2V, V_{IN} = 0.6V, I_{OUT} = 3A	-	180	mV
54	Adjustable OCP; Sourcing	$OCP+_{HIGH}$	V_{OUT} = 0V, V_{IN} = 2V, V_{CC} = 2.7V, $R_{OCP-SRC}$ = 3kΩ	2.7	3.5	A
55		$OCP+_{LOW}$	V_{OUT} = 0V, V_{IN} = 2V, V_{CC} = 2.7V, $R_{OCP-SRC}$ = 30kΩ	0.15	0.6	A
56	Adjustable OCP; Sinking	$OCP-_{HIGH}$	V_{OUT} = 1V, V_{IN} = 2V, V_{CC} = 2.7V, $R_{OCP-SRC}$ = 3kΩ	-3.5	-2.7	A
57	Adjustable OCP; Sinking	$OCP-_{LOW}$	V_{OUT} = 1V, V_{IN} = 2V, V_{CC} = 2.7V, $R_{OCP-SRC}$ = 30kΩ	-0.6	-0.15	A
58	Internal OCP; Sourcing	OCP+	V_{OUT} = 0V, V_{IN} = 2V, V_{CC} = 2.7V, $R_{OCP-SRC}$ = 0Ω	3.3	5	A
59	Internal OCP; Sinking	OCP-	V_{OUT} = 1V, V_{IN} = 2V, V_{CC} = 2.7V, $R_{OCP-SRC}$ = 0Ω	-5	-3.3	A

Table 3. ISL75055SLHMF Datasheet Total Dose Parameters (T_A = 25ºC) (Cont.)

Figure	Parameter	Symbol	Test Conditions	Low Limit	High Limit	Unit
60	Buffer Input Resistance	BUF_R	BUF-IN = 1V	1.5	2.5	MΩ
61	Buffer Input UVLO; Rising	BUF_{UVLOR}	V_{CC} = 2.7V, V_{IN} = 3.3V, CONFIG = V_{CC}	0.75	0.82	V
62	Buffer Input UVLO; Falling	BUF_{UVLOF}	V_{CC} = 2.7V, V_{IN} = 3.3V, CONFIG = V_{CC}	0.72	0.78	V
63	Buffer Input UVLO; Hysteresis	BUF_{UVLOH}	-	10	50	mV
64	Buffer Output Voltage	BUF-OUT	As a percentage of BUF-IN; 1.0V < BUF-IN < 3.3V; -10mA < IBUF-OUT < 10mA	49.5	50.5	%
65	BUF-OUT Tolerance to BUF-IN	$BUFOUT_{TOL}$	1.0V < BUF-IN < 3.3V; -10mA < IBUF-OUT < 10mA	-5	5	mV
66	Buffer Output Current Limit; Sourcing	BUF_{OUT+}	BUF-OUT = 0V, V_{IN} = V_{CC} = 2.7V, BUF-IN = 1.2V, V_{IN} = V_{CC} = 5.5V, BUF-IN = 3.3V	15	27	mA
67	Buffer Output Current Limit; Sinking	BUF_{OUT-}	BUF-OUT = V_{CC}, V_{IN} = V_{CC} = 2.7V, BUF-IN = 1.2V, V_{IN} = V_{CC} = 5.5V, BUF-IN = 3.3V	-27	-15	mA
68	Enable Threshold; Rising	EN_R	VREF_INT rising (200mV) V_{IN} = V_{CC} = 3.3V	1.05	1.15	V
69	Enable Threshold; Falling	EN_F	VREF_INT falling (200mV) V_{IN} = V_{CC} = 3.3V	0.9	1.1	V
70	Enable Threshold; Hysteresis	EN_H	-	10	160	mV
71	Enable Propagation Delay; Falling	EN_PDF	EN = 0V to 5V, EN rising edge to VREF_INT = 450mV, V_{IN} = V_{CC} = 3.3V, C_{VREF_INT} = 100nF	4	8	µs
72	Enable Input Leakage	I_EN	EN = 5.5V	-	1	µA
73	Soft-Start Current	I_SS	SS = 0V, V_{IN} = V_{CC} = 3.3V	17	25	µA
74	Soft-Start Done Threshold	SS_Done	V_{IN} = V_{CC} = 3.3V, PG = 2V	1.65	2.6	V
75	Soft-Start Clamp Voltage	SS_Clamp	V_{IN} = V_{CC} = 3.3V	2.5	3.5	V
76	SS Pin Discharge Resistance	R_SS	SS = 1V, EN = 0V, V_{IN} = V_{CC} = 3.3V	8	22	Ω
77	PG Overvoltage Threshold; Rising	PG_OVR	V_{IN} = V_{CC} = 3.3V, EA- as a % of EA+, EA+ = 0.5V	107	114	%
78	PG Overvoltage Hysteresis	PG_OVH	V_{IN} = V_{CC} = 3.3V, EA- as a % of EA+, EA+ = 0.5V	1.5	5	%
79	PG Undervoltage Threshold; Falling	PG_UVF	V_{IN} = V_{CC} = 3.3V, EA- as a % of EA+, EA+ = 0.5V	87	91	%
80	PG Undervoltage Hysteresis	PG_UVH	V_{IN} = V_{CC} = 3.3V, EA- as a % of EA+, EA+ = 0.5V	1.5	5	%
81	PG Output Low Voltage	PG_LOW	I_PG = 1mA, V_{IN} = V_{CC} = 2.7V, EN = 0V	-	0.4	V
82	PG Leakage Current	PG_LEAK	V_{IN} = V_{CC} = 5.5V, PG = 5.5V, V_{OUT} in regulation	-	0.01	µA
83	PG Delay; Rising	PG_PDR	V_{IN} = V_{CC} = 2.7V, EA- rising edge (0.5V) to PG Rising (89% of V_{CC})	5	8	µs
84	PG Delay; Falling	PG_PDF	V_{IN} = V_{CC} = 2.7V, EA- falling edge (0.4V) to PG Falling (89% of V_{CC})	0.75	1.25	µs
85	CONFIG Pin Threshold	CFIG_R	V_{IN} = V_{CC} = 2.7V, EN = 0V, Rising Threshold when V_{OUT} falls to 0.8V	1.05	1.15	V
86	CONFIG Pin Hysteresis	CFIG_H	-	90	140	mV
87	BUF-OUT Discharge Resistance	BUF-OUT_R	BUF-IN = 0.5V, V_{IN} = V_{CC} = CONFIG = 2.7V, BUF-OUT sinking current = 10mA	9	29	Ω
88	V_{OUT} Discharge Resistance	VOUT_R	EN = 0V, V_{IN} = V_{CC} = CONFIG = 2.7V, V_{OUT} sinking current = 20mA	3	12	Ω

Related Literature

For a full list of related documents, visit our website:

- ISL75055SLHMF device page
- MIL-STD-883 test method 1019

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.