ISL75055SLH

Single Event Effects (SEE) Testing of the ISL75055SLH 3A Source and Sink LDO

Introduction

The intense proton and heavy-ion environment encountered in space applications can cause a variety of Single Event Effects (SEE) in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Latch-Up (SEL), Single Event Gate Rupture (SEGR), and Single Event Burnout (SEB). SEE can lead to system-level performance issues, including disruption, degradation, and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. This report discusses the results of the SEE testing performed on the ISL75055SLH product. The device is offered with radiation assurance screening to 75krad(Si) at 10mrad(Si)/s.

SEE Summary

SEE testing was performed with normal incidence gold for an LET of 86.3MeV·cm^2/mg at the surface of the device. The LET in the active silicon layer ranged from 88.4MeV·cm^2/mg to 90.3MeV·cm^2/mg. The range to Bragg peak was 51µm.

Additional testing was performed with normal incidence silver for an LET of 45.8MeV·cm^2/mg at the surface of the device. The LET in the active silicon layer ranged from 47.9MeV·cm^2/mg to 49.8MeV·cm^2/mg. The range to the Bragg peak was 67.6µm.

The ISL75055SLH proved to be free of Destructive Single Event Effects (DSEE) under the following maximum parameter set at a die temperature of 125°C: V_{CC} = 6.2V and V_{IN} = 6.2V at 86.3MeV·cm^2/mg and V_{CC} = 6.9V and V_{IN} = 6.2V at 45.8MeV·cm^2/mg.

The ISL75055SLH was tested for SETs in both an LDO and DDR terminator configuration. The ISL75055SLH was monitored for SET events during which VOUT deviated by 2% of its operating value, BUF-OUT deviated by 2% of its operating value, and the differential between V_{OUT} and BUF-OUT exceeded ±40mV. The ISL75055SLH was also monitored for PG SETs during which PG pulled low without a loss of V_{OUT} regulation and SEFIs during which PG pulled low and there was a loss of V_{OUT} regulation. However, the ISL75055SLH did not exhibit any of these SEEs at an LET of 86MeV·cm^2/mg.

The results of this report apply to both the ISL75055SLHMF (ceramic) and the ISL75055SLHNEZ (plastic), as the parts were depackaged for testing such that the bare silicon was exposed to the heavy-ion beam.

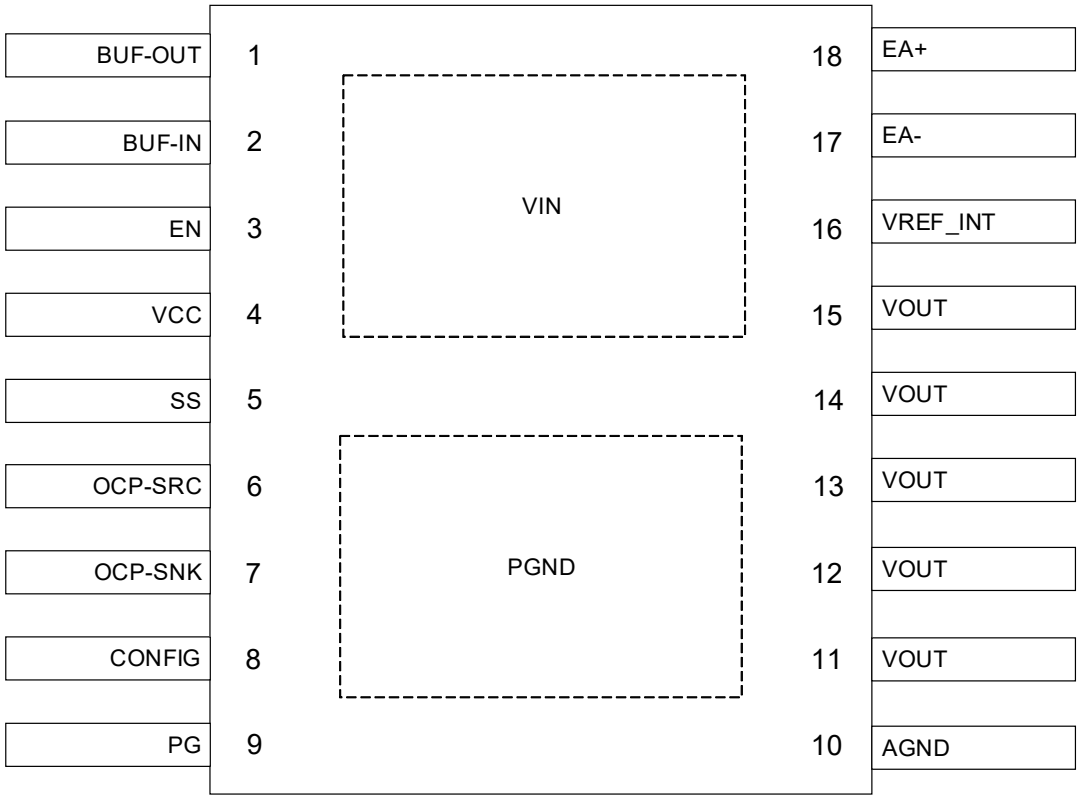
Product Description

The ISL75055SLH is a radiation-hardened 0.75V to 5.5V input, 3A sourcing and sinking low-dropout linear regulator designed for powering the VTT termination rail of DDR memory modules. A buffered reference amplifier provides an accurate VREF supply for the DDR. Individual adjustable overcurrent protection (OCP) for sourcing and sinking allows the current limit of the LDO to be configured down to 300mA applications.

The ISL75055SLH features external error amplifier inputs to set VDDQ/2 as the reference voltage in DDR applications. It also features an internal 0.5V reference for standard LDO applications.

Separate VCC bias and LDO VIN pins, combined with a very low dropout, allow minimal internal losses while maintaining highly accurate output regulation.

The ISL75055SLHMF is offered in an 18 Ld CDFP, and the ISL75055SLHNEZ is offered in a 48 Ld plastic eTQFP. Both versions operate across the full-range military temperature range of -55°C to +125°C



Note: Pin 1 has a protrusion in the package lead. See Package Outline Drawing.

Figure 1. ISL75055SLHMF Pin Assignments

Table 1. ISL75055SLHMF Pin Descriptions

Pin Number	Pin Name	Description
1	BUF-OUT	Buffered reference outputs voltage 50% of BUF-IN for DDR applications. This pin can source or sink up to 10mA. Place a minimum 100nF, maximum 2.2µF capacitor on this pin to AGND for filtering. A minimum of 1µF is recommended for SEE mitigation Buffered reference output is independent of EN input and active when BUF-IN is above 0.78V.
2	BUF-IN	Buffered reference input voltage VDDQ for DDR applications. An internal voltage driver outputs 50% of the input signal (VDDQ/2) on BUF-OUT pin. When VIN directly supplies BUF-IN, a 1kΩ/1µF filter is recommended at the input of BUF-IN for SEE mitigation.
3	EN	Enable pin for the LDO output
4	VCC	Analog bias pin with 2.7V to 5.5V input range. Place a 1µF capacitor on this pin to AGND for filtering.
5	SS	Soft-start pin. Place a capacitor on this pin for soft-start power up. A 20µA current source charges capacitor for ramping the reference of the error amplifier for a controlled start-up.
6	OCP-SRC	Sourcing Overcurrent Protection setting pin. A resistor on this pin to GND sets the Sourcing OCP level from 300mA to 3A. Short this pin to AGND for 4A OCP level.
7	OCP-SNK	Sinking Overcurrent Protection setting pin. A resistor on this pin to GND sets the Sinking OCP level from 300mA to 3A. Short this pin to AGND for 4.1A OCP level.
8	CONFIG	LDO V_{OUT} and BUF-OUT discharge control pin. When low, discharge function disabled. When high, discharge function enabled. Internal switch discharges V_{OUT} when EN = low. Internal switch discharges BUF-OUT when BUF-IN is below input UVLO threshold.
9	PG	Open-drain Power-Good indicator pin. Place a resistor form PG to VCC. When V_{OUT} is in OV/UV, PG pin pulls low.

Table 1. ISL75055SLHMF Pin Descriptions (Cont.)

Pin Number	Pin Name	Description
10	AGND	Analog ground pin. The lid of the part is internally connected to this pin.
11-15	VOUT	LDO output pin. Place a minimum of 2x 150pF tantalum capacitors near this pin to PGND for stability.
16	VREF_INT	Internal 500mV reference. Place a 0.1µF ceramic capacitor on this pin to AGND.
17	EA-	Inverting input to the error amplifier.
18	EA+	Non-inverting input to the error amplifier. Connect to VREF_INT for the 500mV internal reference or connect to BUF-OUT for DDR applications.
EPADU	VIN	LDO input voltage. A single 150µF tantalum capacitor and 2x10µF ceramic capacitor is recommended close to VIN and PGND connections. This is the upper EPAD on the backside of package. Connect EPADU to the PCB on multiple layers with thermal vias underneath the EPADU to maximize thermal performance.
EPADL	PGND	LDO power ground connection. Connect common to AGND pin. The lid of the part is internally connected to this pin. This is the lower EPAD on the backside of package Connect EPADL to the PCB on multiple layers with thermal vias underneath the EPADL to maximizes thermal performance.

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1. SEE Testing

1.1 Objective

The testing was intended to find the limit of the LDO input voltage (V_{IN}) and the analog bias voltage (V_{CC}) set by the onset of DSEE at a LET of 86.3MeV·cm^2/mg (normal incidence gold) and 45.8MeV·cm^2/mg (normal incidence silver). Additional testing was intended to identify and quantify SETs and SEFIs occurring in the output voltage, buffered output voltage, or on the PG pin of the ISL75055SLH.

1.2 Facility

SEE testing was done at the Texas A&M University (TAMU) Radiation Effects Facility of the Cyclotron Institute in College Station, Texas. This facility is coupled to a K500 superconducting cyclotron that can supply a wide range of ion species and flux. The SEE testing in this report was performed in April 2025.

2. Results

2.1 DSEE Results

DSEE testing was performed to determine the maximum LDO input voltage (V_{IN}) and analog bias voltage (V_{CC}) free from DSEEs at a die temperature of 125°C. The test board was laid out such that two parts could be irradiated simultaneously. During each run, the devices were exposed to heavy ions to a fluence of 1E7ions/cm^2.

To stress the entire device during DSEE testing, the device was configured such that V_{REF} was supplied to BUF-IN through a voltage divider and BUF-OUT fed into EA+. In this configuration, both the LDO and DDR terminator circuitry are exercised. Figure 2 shows the schematic for DSEE testing.

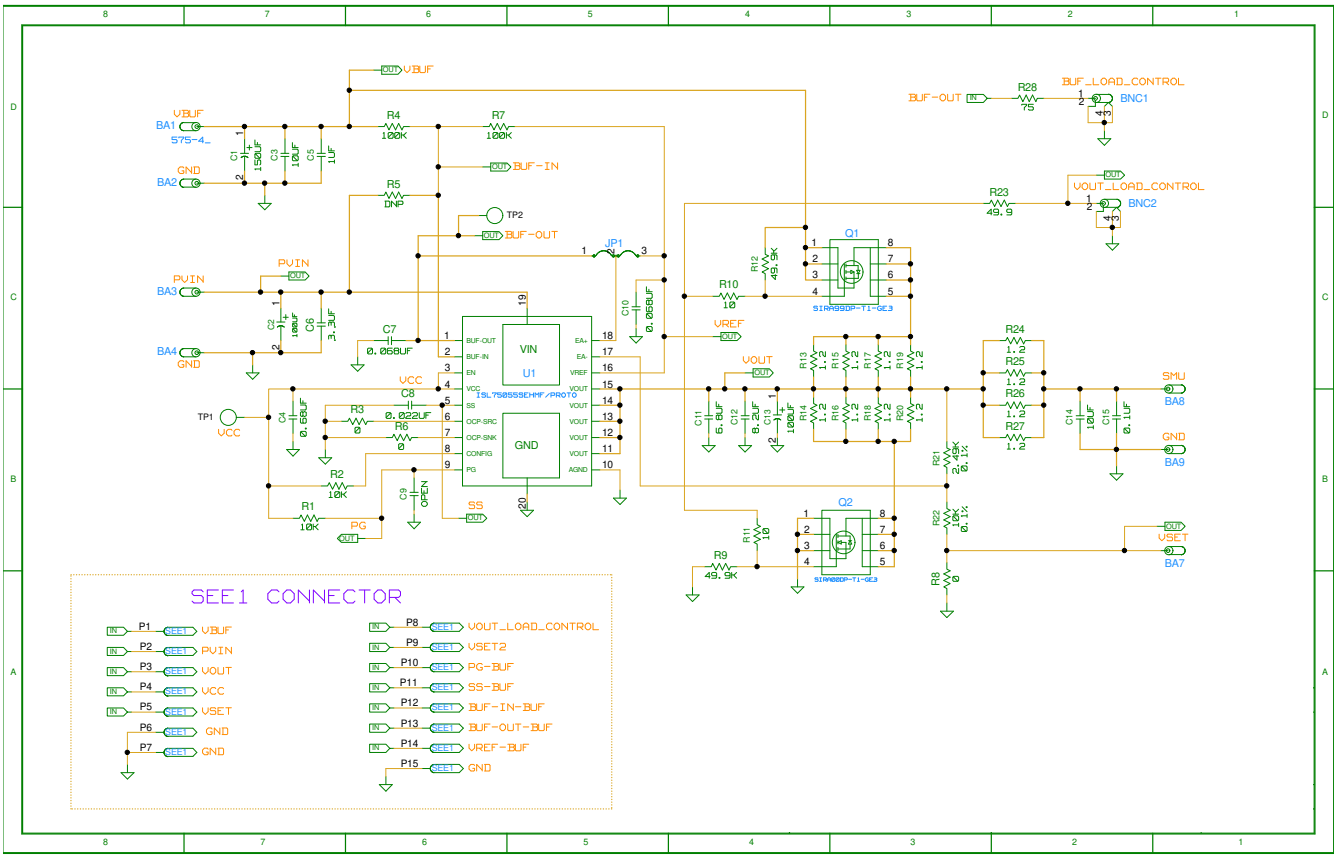

Figure 2. ISL75055SLH DSEE Schematic

For V_{CC} DSEE testing, V_{IN} was set to 2V, and V_{OUT} was set to 1V. I_{OUT} was switched between sourcing 3.3A and sinking 3.3A at 100Hz with a 50% duty cycle. The voltage on BUF-IN was 1.25V, and the voltage on BUF-OUT was 0.625V. There was no load on the buffer. EN was tied to V_{CC}, and PG was pulled up to V_{CC} through a 10kΩ resistor. V_{CC} was initially set to 5.5V and increased in steps of 5% derating following each run. Testing concluded when V_{CC} reached 6.9V or the device exhibited a DSEE. A device was considered to have exhibited a DSEE if the output voltage at no load deviated by ±1% or the current on V_{CC} at no load deviated by ±10%.

V_{IN} DSEE testing was conducted in two sections: one with EN grounded and one with EN high.

V_{IN} DSEE testing was performed with EN grounded to apply the maximum stress to the pass transistor, as blocking mode is the worst-case condition for testing MOSFETs. For this testing, V_{OUT} was tied to ground, and there was no load. V_{CC} was tied to ground. V_{IN} was initially set to 5.5V and was increased in steps of 5% derating. Testing concluded when V_{IN} reached 6.9V or the device exhibited a DSEE. A device was considered to have exhibited a DSEE if the current on V_{IN} deviated by ±50%.

For V_{IN} DSEE testing with EN high, the device under test sourced 3.3A. V_{CC} was set to 6.2V. V_{IN} was initially set to 5.5V, and V_{OUT} was initially set to 4V. V_{IN} was increased in steps of 5% derating. V_{OUT} was simultaneously increased to maintain a 1.5V differential between V_{IN} and V_{OUT}. To increase V_{OUT} without making a board modification between runs, V_{OUT} was set using an external power supply connected to EA-. BUF-IN was increased following each run from a starting voltage of 1.33V to a maximum voltage of 1.8V. Testing concluded when V_{IN} reached the maximum voltage attained during V_{IN} DSEE testing with EN = 0V or the device exhibited a DSEE. A device was considered to have exhibited a DSEE if the output voltage at no load deviated by ±2%, the current on V_{CC} deviated by ±5%, or the current on V_{IN} deviated by ±15%.

2.1.1 LET = 86.3MeV·cm²/mg

The results of V_{CC} DSEE testing at 86.3MeV·cm²/mg are displayed in Table 2. All four devices exhibited DSEEs when operated with V_{CC} = 6.5V; therefore, the device should be operated with a maximum value of V_{CC} = 6.2V to be robust against DSEE at 86.3MeV·cm²/mg.

Table 2. ISL75055SLH VCC DSEE Test Results at 86.3MeV·cm²/mg

VCC/PG/EN (V)	DUT #	Result	I_{VCC} at I_{OUT} = 0A (±10%)			V_{OUT} (±1%)		
			Pre (mA)	Post (mA)	Δ (%)	Pre (V)	Post (V)	Δ (%)
5.5	1	Pass	4.433	4.467	0.77	1.106	1.011	-0.49
	2	Pass	4.584	4.619	0.76	1.042	1.043	0.10
	3	Pass	4.280	4.209	-1.66	0.976	0.977	0.10
	4	Pass	4.276	4.202	-1.73	0.948	0.948	0.00
5.8	1	Pass	4.566	4.646	1.75	1.012	1.011	-0.10
	2	Pass	4.719	4.765	0.97	1.043	1.041	-0.19
	3	Pass	4.300	4.318	0.42	0.977	0.975	-0.20
	4	Pass	4.319	4.656	7.80	0.949	0.949	0.00
6.2	1	Pass	4.96	5.033	1.47	1.011	1.011	0.00
	2	Pass	5.082	4.65	-8.50	1.041	1.041	0.00
	3	Pass	4.695	4.678	-0.36	0.975	0.972	-0.31
	4	Pass	4.993	4.952	-0.82	0.950	0.947	-0.32
6.5	1	Fail	5.534	8.683	56.9	1.011	1.014	0.29
	2	Fail	5.136	9.88	92.4	1.041	1.040	-0.10
	3	Fail	5.125	5.868	14.5	0.973	0.973	0.00
	4	Fail	5.466	21.72	297.4	0.974	0.948	0.11

The results of V_{IN} DSEE testing with EN grounded for the ISL75055SLH are displayed in Table 3. All four devices exhibited DSEEs when operated with V_{IN} = 6.5V, the device should be operated with a maximum value of V_{IN} = 6.2V to be robust against DSEE with the EN = 0V at 86.3MeV·cm^2/mg.

Table 3. ISL75055SLH VIN DSEE with EN = 0V Test Results at 86.3MeV·cm^2/mg

V_{IN} (V)	V_{OUT} (V)	DUT #	Result	I_{VIN} (±50%)		
				Pre (µA)	Post (µA)	Δ (%)
5.5	GND	5	Pass	55	52	-5.45
		6	Pass	46	48	4.35
		7	Pass	70	71	1.43
		8	Pass	59	62	5.08
5.8	GND	5	Pass	64	67	4.68
		6	Pass	69	62	-10.14
		7	Pass	73	74	1.37
		8	Pass	65	65	0.00
6.2	GND	5	Pass	66	61	-7.58
		6	Pass	73	73	0.00
		7	Pass	74	74	0.00
		8	Pass	73	74	1.37
6.5	GND	5	Fail	60	212,000	353,233
		6	Fail	74	63,000	85,035
		7	Fail	76	61,000	80,163
		8	Fail	74	51,000	68,819

The results of V_{IN} DSEE testing with EN high at 86.3MeV·cm^2/mg are displayed in Table 4. All four devices passed with V_{IN} = 6.2V; therefore, the device should be operated with a maximum value of V_{IN} = 6.2V to be robust against DSEE with the part enabled at 86.3MeV·cm^2/mg and 125°C.

Table 4. ISL75055SLH VIN DSEE with EN High Test Results at 86.3MeV·cm^2/mg

V_{IN} (V)	BUF-IN (V)	V_{OUT} (V)	DUT #	Result	I_{VCC} at I_{OUT} = 0A (±5%)			I_{VIN} at I_{OUT} = 0A (±15%)			V_{OUT} (±2%)		
					Pre (mA)	Post (mA)	Δ (%)	Pre (µA)	Post (µA)	Δ (%)	Pre (V)	Post (V)	Δ (%)
5.5	1.33	4	9	Pass	4.848	4.942	1.94	43	38.5	-10.47	4.018	4.010	-0.20
			10	Pass	4.923	4.918	-0.10	14	13.2	-5.71	4.049	4.0138	-0.87
			11	Pass	4.822	4.798	-0.50	26	26	0.00	4.019	4.014	-0.12
			12	Pass	4.838	4.866	0.58	25	28	12.00	4.037	4.035	-0.05
5.8	1.43	4.3	9	Pass	4.939	4.-12	1.48	101	96	-4.95	4.397	4.404	0.16
			10	Pass	4.898	4.95	1.06	85	78	-8.24	4.413	4.408	-0.11
			11	Pass	4.799	4.802	0.06	92	89	-3.26	4.422	4.384	-0.86
			12	Pass	4.841	4.882	0.85	84	78	-7.14	4.434	4.433	-0.02
6.2	1.57	4.7	9	Pass	4.913	4.077	3.34	144	147	2.08	5.045	5.111	1.31
			10	Pass	4.956	5.047	1.84	121	125	3.31	5.049	5.11	1.21
			11	Pass	4.859	4.888	0.60	144	148	2.78	5.104	5.089	-0.29
			12	Pass	4.934	5.019	1.72	139	147	5.76	5.161	5.169	0.16

DSEE testing indicates that the ISL75055SLH should be operated with a maximum of V_{IN} = 6.2V and V_{CC} = 6.2V regardless of whether EN is high or low at 125°C and 86.3MeV·cm^2/mg.

2.1.2 LET = 45.8MeV·cm^2/mg

The results of V_{CC} DSEE testing at 45.8MeV·cm^2/mg are displayed in Table 5. None of the four devices exhibited DSEEs when operated with V_{CC} = 6.9V; therefore, the device should be operated with a maximum value of V_{CC} = 6.9V to be robust against DSEE at 45.8MeV·cm^2/mg.

Table 5. ISL75055SLH V_{CC} DSEE Test Results at 45.8MeV·cm^2/mg

VCC/PG/EN (V)	DUT #	Result	I_{VCC} at I_{OUT} = 0A (±10%)			V_{OUT} (±1%)		
			Pre (mA)	Post (mA)	Δ (%)	Pre (V)	Post (V)	Δ (%)
6.2	21	Pass	5.392	5.398	0.11	0.999	0.998	-0.10
	22	Pass	5.273	5.279	0.11	0.972	0.969	-0.31
	23	Pass	4.620	4.983	7.86	1.041	1.041	0.00
	24	Pass	4.687	4.693	0.13	1.067	1.068	0.09
6.5	21	Pass	5.536	5.433	-1.86	0.998	0.998	0.00
	22	Pass	5.096	5.109	0.26	0.969	0.970	0.10
	23	Pass	5.511	5.477	-0.62	1.041	1.041	0.00
	24	Pass	5.153	5.113	-0.78	1.068	1.067	-0.09
6.9	21	Pass	6.729	6.582	-2.18	0.997	0.997	0.00
	22	Pass	6.410	6.106	-4.74	0.970	0.971	0.10
	23	Pass	6.633	6.601	-0.48	1.041	1.041	0.00
	24	Pass	6.232	6.159	-1.17	1.067	1.067	0.00

The results of V_{IN} DSEE testing with EN grounded for the ISL75055SLH are displayed in Table 6. All four devices exhibited DSEEs when operated with V_{IN} = 6.5V; therefore, the device should be operated with a maximum value of V_{IN} = 6.2V to be robust against DSEE with the EN = 0V at 45.8MeV·cm^2/mg.

Table 6. ISL75055SLH V_{IN} DSEE with EN = 0V Test Results at 45.8MeV·cm^2/mg

V_{IN} (V)	V_{OUT} (V)	DUT #	Result	I_{VIN} (±50%)		
				Pre (µA)	Post (µA)	Δ (%)
6.2	GND	25	Pass	13.42	13.21	-1.56
		26	Pass	46.7	58.4	25.05
		27	Pass	31.19	16.39	-47.45
		28	Pass	55.5	64.4	16.03
6.5	GND	25	Fail	19.66	33,000	167,753
		26	Fail	64.4	33,400	51,763
		27	Fail	18.3	79,000	431,593
		28	Fail	70.3	55,000	78,136

Since the V_{IN} DSEE performance of the DUT with EN = 0V did not improve with lower LET, V_{IN} DSEE testing with the DUT enabled was not performed at 45.8MeV·cm^2/mg since it already passed with V_{IN} = 6.2V at 86.3MeV·cm^2/mg.

DSEE testing indicates that the ISL75055SLH should be operated with a maximum of V_{IN} = 6.2V and V_{CC} = 6.9V regardless of whether EN is high or low at 125°C and 45.8MeV·cm^2/mg.

2.2 SET Results

The ISL75055SLH was tested for SETs in both an LDO and DDR terminator configuration at 25°C and an LET of 86.3MeV·cm^2/mg. Each run was to a fluence of 1E7ions/cm^2.

2.2.1 DDR Mode

For SET testing in a DDR configuration, the board was set up to irradiate one part at a time. BUF-IN was supplied directly by V_{IN}, and a 1kΩ and 0.680µF filter was applied at the input of BUF-IN. A 0.680µF bypass capacitor was applied to BUF-OUT, and BUF-OUT fed into EA+. The devices were tested under six different test conditions as given in Table 7. For each test condition, the load on the buffer was switched between -10mA and 10mA at 100Hz and a 50% duty cycle. EN was tied to V_{CC}. PG was pulled up to V_{CC} though a 10kΩ resistor.

Table 7. ISL75055SLH DDR SET Test Conditions

Test Condition	Number of Devices Tested	Total Fluence (ions/cm^2)	VCC (V)	V_{IN} (V)	BUF-IN (V)	V_{OUT} (V)	BUF-OUT (V)	I_{OUT} (A)
#1	4	4E7	2.7	1.2	1.2	0.6	0.6	3
#2	4	4E7	5.5	1.2	1.2	0.6	0.6	3
#3	4	4E7	2.7	1.2	1.2	0.6	0.6	-3
#4	4	4E7	5.5	1.2	1.2	0.6	0.6	-3
#5	4	4E7	5.5	5.5	5.5	2.75	2.75	0.3
#6	4	4E7	5.5	5.5	5.5	2.75	2.75	-0.3

During irradiation, devices were monitored for V_{OUT} SETs, BUF-OUT SETs, Differential SETs, PG SETs, and SEFIs. A V_{OUT} SET was defined as an event during which V_{OUT} deviated beyond ±2% of its operating value. A BUF-OUT SET was defined as an event during which BUF-OUT deviated beyond ±2% of its operating value. A Differential SET was defined as an event during which the differential between V_{OUT} and BUF-OUT deviated beyond ±40mV, a condition forbidden by the JEDEC DDR specification. A PG SET was defined as an event during which PG pulled low but the device did not enter soft-start, and there was no loss of V_{OUT} regulation. A SEFI was defined as an event during which PG pulled low and there was a loss of V_{OUT} regulation.

V_{OUT} and BUF-OUT SETs were captured with a trigger set to capture events during which V_{OUT} or BUF-OUT, respectively, deviated beyond ±2% of its operating value. Differential SETs were captured with a trigger set to capture events during which the differential between V_{OUT} and BUF-OUT deviated beyond 40mV. The differential between VOUT and BUF-OUT was generated using a differential amplifier. PG SETs and SEFIs were captured with a trigger set to capture events during which PG fell below 1.35V.

The results of DDR SET testing for the ISL75055SLH are displayed in Table 8. The results are summarized in Table 9. No V_{OUT} SETs, BUF-OUT SETs, Differential SETs, PG SETs, or SEFIs were observed during testing.

Table 8. ISL75055SLH DDR SET Test Results at 86.3MeV·cm^2/mg

Test Condition	DUT #	Fluence (ions/cm^2)	# of V_{OUT} SETs	# of BUF-OUT SETs	# of Differential SETs	# of PG SETs	# of SEFIs
#1	21	1.0E7	0	0	0	0	0
	22	1.0E7	0	0	0	0	0
	23	1.0E7	0	0	0	0	0
	24	1.0E7	0	0	0	0	0
#2	21	1.0E7	0	0	0	0	0
	22	1.0E7	0	0	0	0	0
	23	1.0E7	0	0	0	0	0
	24	1.0E7	0	0	0	0	0

Table 8. ISL75055SLH DDR SET Test Results at 86.3MeV·cm^2/mg

Test Condition	DUT #	Fluence (ions/cm^2)	# of V_{OUT} SETs	# of BUF-OUT SETs	# of Differential SETs	# of PG SETs	# of SEFIs
#3	21	1.0E7	0	0	0	0	0
	22	1.0E7	0	0	0	0	0
	23	1.0E7	0	0	0	0	0
	24	1.0E7	0	0	0	0	0
#4	21	1.0E7	0	0	0	0	0
	22	1.0E7	0	0	0	0	0
	23	1.0E7	0	0	0	0	0
	24	1.0E7	0	0	0	0	0
#5	25	1.0E7	0	0	0	0	0
	26	1.0E7	0	0	0	0	0
	27	1.0E7	0	0	0	0	0
	28	1.0E7	0	0	0	0	0
#6	25	1.0E7	0	0	0	0	0
	26	1.0E7	0	0	0	0	0
	27	1.0E7	0	0	0	0	0
	28	1.0E7	0	0	0	0	0

Table 9. ISL75055SLH DDR SET Test Summary at 86.3MeV·cm^2/mg

Test Condition	# of DUTs	Total Fluence (ions/cm^2)	# of V_{OUT} SETs	# of BUF-OUT SETs	# of Differential SETs	# of PG SETs	# of SEFIs
#1	4	4.0E7	0	0	0	0	0
#2	4	4.0E7	0	0	0	0	0
#3	4	4.0E7	0	0	0	0	0
#4	4	4.0E7	0	0	0	0	0
#5	4	4.0E7	0	0	0	0	0
#6	4	4.0E7	0	0	0	0	0

2.2.2 LDO Mode

For SET testing in an LDO configuration, the board was set up to irradiate two parts at a time. A 0.068µF bypass capacitor was applied to V_{REF}, and V_{REF} fed into EA+. The devices were tested under eight different test conditions as given in Table 10. For each test condition, EN was tied to V_{CC}. PG was pulled up to V_{CC} though a 10kΩ resistor.

Table 10. ISL75055SLH LDO SET Test Conditions

Test Condition	Number of Devices Tested	Total Fluence (ions/cm^2)	VCC (V)	V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)
#1	4	4E7	2.7	1.5	1	3
#2	4	4E7	5.5	1.5	1	3
#3	4	4E7	2.7	1.5	1	-3
#4	4	4E7	5.5	1.5	1	-3
#5	4	4E7	2.7	5.5	1	0.3
#6	4	4E7	5.5	5.5	1	0.3
#7	4	4E7	2.7	5.5	1	-0.3
#8	4	4E7	5.5	5.5	1	-0.3

During irradiation, devices were monitored for V_{OUT} SETs, PG SETs, and SEFIs. A V_{OUT} SET was defined as an event during which V_{OUT} deviated beyond ±2% of its operating value. A PG SET was defined as an event during which PG pulled low but the device did not enter soft-start, and there was no loss of V_{OUT} regulation. A SEFI was defined as an event during which PG pulled low and there was a loss of V_{OUT} regulation.

V_{OUT} SETs were captured with a trigger set to capture events during which V_{OUT} deviated beyond ±2% of its operating value. PG SETs and SEFIs were captured with a trigger set to capture events during which PG fell below 1.5V.

The results of LDO SET testing for the ISL75055SLH are displayed in Table 11. The results are summarized in Table 12. No V_{OUT} SETs, PG SETs, or SEFIs were observed during testing.

Table 11. ISL75055SLH LDO SET Test Results at 86.3MeV·cm^2/mg

Test Condition	DUT #	Fluence (ions/cm^2)	# of V_{OUT} SETs	# of BUF-OUT SETs	# of Differential SETs	# of PG SETs	# of SEFIs
#1	13	1.0E7	0	0	0	0	0
	14	1.0E7	0	0	0	0	0
	15	1.0E7	0	0	0	0	0
	16	1.0E7	0	0	0	0	0
#2	13	1.0E7	0	0	0	0	0
	14	1.0E7	0	0	0	0	0
	15	1.0E7	0	0	0	0	0
	16	1.0E7	0	0	0	0	0
#3	13	1.0E7	0	0	0	0	0
	14	1.0E7	0	0	0	0	0
	15	1.0E7	0	0	0	0	0
	16	1.0E7	0	0	0	0	0

Table 11. ISL75055SLH LDO SET Test Results at 86.3MeV·cm^2/mg (Cont.)

Test Condition	DUT #	Fluence (ions/cm^2)	# of V_{OUT} SETs	# of BUF-OUT SETs	# of Differential SETs	# of PG SETs	# of SEFIs
#4	13	1.0E7	0	0	0	0	0
	14	1.0E7	0	0	0	0	0
	15	1.0E7	0	0	0	0	0
	16	1.0E7	0	0	0	0	0
#5	17	1.0E7	0	0	0	0	0
	18	1.0E7	0	0	0	0	0
	19	1.0E7	0	0	0	0	0
	20	1.0E7	0	0	0	0	0
#6	17	1.0E7	0	0	0	0	0
	18	1.0E7	0	0	0	0	0
	19	1.0E7	0	0	0	0	0
	20	1.0E7	0	0	0	0	0
#7	17	1.0E7	0	0	0	0	0
	18	1.0E7	0	0	0	0	0
	19	1.0E7	0	0	0	0	0
	20	1.0E7	0	0	0	0	0
#8	17	1.0E7	0	0	0	0	0
	18	1.0E7	0	0	0	0	0
	19	1.0E7	0	0	0	0	0
	20	1.0E7	0	0	0	0	0

Table 12. ISL75055SLH LDO SET Test Summary at 86.3MeV·cm^2/mg

Test Condition	# of DUTs	Total Fluence (ions/cm^2)	# of V_{OUT} SETs	# of PG SETs	# of SEFIs
#1	4	4.0E7	0	0	0
#2	4	4.0E7	0	0	0
#3	4	4.0E7	0	0	0
#4	4	4.0E7	0	0	0
#5	4	4.0E7	0	0	0
#6	4	4.0E7	0	0	0
#7	4	4.0E7	0	0	0
#8	4	4.0E7	0	0	0

3. Discussion and Conclusion

SEE testing was performed with normal incidence gold for an LET of 86.3MeV·cm^2/mg and normal incidence silver for an of 45.8MeV·cm^2/mg.

Testing indicated that the maximal parameter set to be robust against DSEE is: V_{IN} = 6.2V and V_{CC} = 6.2V at 86.3MeV·cm^2/mg and V_{IN} = 6.9V and V_{CC} = 6.2V at 45.8MeV·cm^2/mg.

The ISL75055SLH was tested for SETs in both an LDO and DDR terminator configuration. The ISL75055SLH was monitored for SETs during which V_{OUT} deviated by 2% of its operating value, BUF-OUT deviated by 2% of its operating value, and the differential between V_{OUT} and BUF-OUT exceeded ±40mV. The ISL75055SLH was also monitored for PG SETs during which PG pulled low without a loss of V_{OUT} regulation and SEFIs during which PG pulled low and there was a loss of V_{OUT} regulation.

However, the ISL75055SLH did not exhibit any of these SEEs at an LET of 86.3MeV·cm^2/mg. Therefore, the ISL75055SLH is an excellent choice for radiation-hardened 3A LDO and DDR terminator applications.

4. Revision History

Revision	Date	Description
1.00	Jun 8, 2026	Initial release.

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