ISL74420SLH

Single Event Effects (SEE) Testing of the ISL74420SLH Quad Clock Fanout IC

Introduction

The intense proton and heavy-ion environment encountered in space applications can cause a variety of Single Event Effects (SEE) in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Latch-Up (SEL), Single Event Gate Rupture (SEGR), and Single Event Burnout (SEB). SEE can lead to system-level performance issues including disruption, degradation, and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. This report discusses the results of the SEE testing performed on the ISL74420SLH product. The ISL74420SLH is offered with radiation assurance screening to 75krad(Si) at 10mrad(Si)/s.

SEE Summary

All SEE testing was performed with normal incidence gold for a LET of 86.3MeV·cm^2/mg at the surface of the device. The LET in the active silicon layer of the device ranged from 88.4MeV·cm^2/mg to 90.2MeV·cm^2/mg.

The ISL74420SLH proved to be free of Destructive Single Event Effects (DSEE) under the following maximum parameter set: PVIN = 20.7V, VCC = 5.5V, and VCCEXT = 6.5V.

The clock fanout IC was monitored for two types of SETs: missing pulses and frequency deviations. The device did not exhibit missing pulses.

There were frequency deviation SETs on CLKOUT0 and CLKOUT1 when the ISL74420SLH was operated in leader mode using the internal oscillator. However, these events lacked a well-defined signature.

The I^{2}C registers were continuously read out during testing to monitor for SEUs. No SEUs were observed.

A SEFI was defined as an event in which the READY pin pulled low. No SEFIs were observed.

The results of this report apply to both the ISL74420SLHMF (ceramic) and the ISL74420SLHMNZ (plastic) as the parts were unpackaged for testing such that the bare silicon was exposed to the heavy ion beam.

Product Description

The ISL74420SLH is a radiation hardened quad output clock fanout buffer with an optional internal oscillator. It provides synchronization clocks for any application and are particularly useful in multiphase power converters. Each of the four outputs can be set to a different frequency division and phase delay.

The division and delay options can be set through selection pins or over an I^{2}C interface.

In addition to the external CLKIN capability, an internal oscillator operates at 48MHz and is tunable ±10% with an external resistor.

The ISL74420SLH is offered in a 48 Lead Ceramic Quad Flat Pack (CQFP) or a 48 Lead Thin Quad Flat Package (TQFP) that are fully specified across the temperature range of -55°C to +125°C.

© 2025 Renesas Electronics

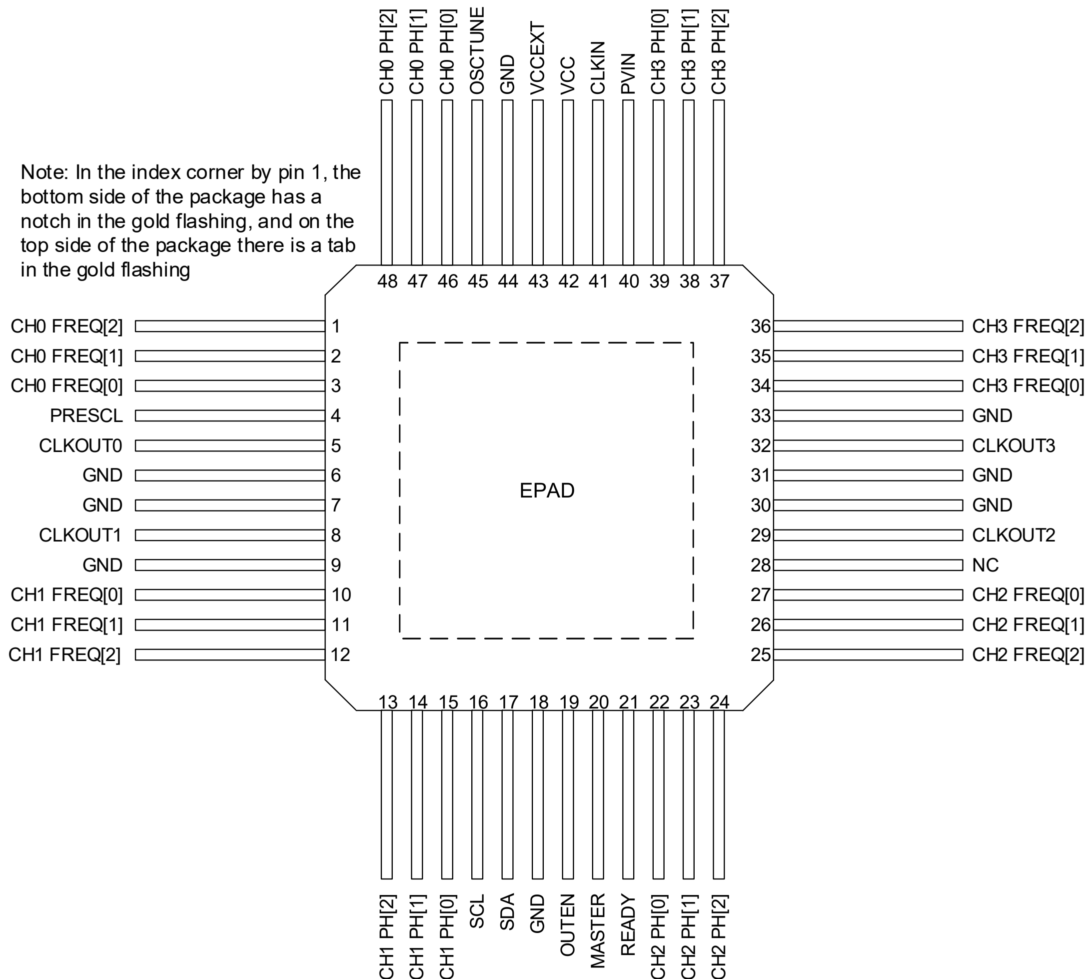

Figure 1. ISL74420SLH 48-Ld CQFP Pin Assignments

Table 1. ISL74420SLH Pin Descriptions

Pin Number	Pin Name	Description
1	CH0 FREQ[2]	3-level (tri-level) logic with 3-bit setting for frequency division selection on Channel 0.
2	CH0 FREQ[1]	
3	CH0 FREQ[0]	
4	PRESCL	3-level (tri-level) logic prescale selection for all channels.
5	CLKOUT0	Clock output pin for Channel 0.
6, 7, 9, 30, 31, 33, 44	GND	Connect these pins to the PCB ground.
8	CLKOUT1	Clock output pin for Channel 1
10	CH1 FREQ[0]	3-level (tri-level) logic with 3-bit setting for frequency division selection on Channel 1
11	CH1 FREQ[1]	
12	CH1 FREQ[2]	
13	CH1 PH[2]	3-level (tri-level) logic with 3-bit setting for phase delay selection for Channel 1.
14	CH1 PH[1]	
15	CH1 PH[0]	

Table 1. ISL74420SLH Pin Descriptions (Cont.)

Pin Number	Pin Name	Description
16	SCL	I^2C/SMBus clock input. SCL requires an external pull-up resistor for proper operation. Tie to VCC through a 4.7kΩ to 100kΩ resistor even if I^2C/SMBus is not going to be used.
17	SDA	I^2C/SMBus data input/output. SDA requires an external pull-up resistor for proper operation. Tie to VCC through a 4.7kΩ to 100kΩ resistor even if I^2C/SMBus is not going to be used.
18	GND	Connect this pin to the PCB ground.
19	OUTEN	Logic level input to enable the CLKOUTx pins.
20	MASTER	Logic level input to select if the part should use its internal oscillator when no external clock is present. A logic high enables Leader Mode and uses the internal 48MHz oscillator if no CLK-IN signal is present. A logic low enables Follower Mode and the internal oscillator is disabled, relying only on the CLK-IN input.
21	READY	Open-drain output to indicate if the part is ready to enable the CLKOUTx pins
22	CH2 PH[0]	3-level (tri-level) logic with 3-bit setting for phase delay selection for Channel 2.
23	CH2 PH[1]	
24	CH2 PH[2]	
25	CH2 FREQ[2]	3-level (tri-level) logic with 3-bit setting for frequency division selection on Channel 2.
26	CH2 FREQ[1]	
27	CH2 FREQ[0]	
28	NC	No internal connection. Renesas recommends connecting this pin to GND.
29	CLKOUT2	Clock output pin or Channel 2.
32	CLKOUT3	Clock output pin or Channel 3.
34	CH3 FREQ[0]	3-level (tri-level) logic with 3-bit setting for frequency division selection on Channel 3.
35	CH3 FREQ[1]	
36	CH3 FREQ[2]	
37	CH3 PH[2]	3-level (tri-level) logic with 3-bit setting for phase delay selection for Channel 3.
38	CH3 PH[1]	
39	CH3 PH[0]	
40	PVIN	The power supply input to the IC. This supplies power to the internal linear regulator. Locally bypass PVIN to GND with a 0.1µF or larger capacitor.
41	CLKIN	External clock input. Tie this pin to the ISL74420SLH GND with a short trace if not using CLKIN.
42	VCC	Output of the 3.3V internal linear regulator. The regulator can by bypassed by providing a 3.0V to 3.6V supply to both PVIN and VCC. Locally bypass VCC to GND with a 1µF capacitor.
43	VCCEXT	The power supply input for all of the CLKOUTx pins. This can be connected to VCC or supplied externally to level shift them to a different voltage. If supplied externally, locally bypass VCCEXT to GND with a 1µF or larger capacitor.
45	OSCTUNE	Connect a resistor between this pin and GND to adjust the internal oscillator.
46	CH0 PH[0]	3-level (tri-level) logic with 3-bit setting for phase delay selection for Channel 0.
47	CH0 PH[1]	
48	CH0 PH[2]	
-	EPAD	Connect to the PCB ground. The EPAD is connected internally within the package to pin 30 (GND).
-	LID	The LID is connected internally within the package to pin 30 (GND).

Contents

1. SEE Testing 5

1.1 Objective 5

1.2 Facility 5

2. Results 5

2.1 DSEE Results 5

2.1.1 PVIN DSEE Results 5

2.1.2 VCC DSEE Results 6

2.1.3 VCCEXT DSEE Results 7

2.2 SET Results 7

3. Discussion and Conclusion 11

4. Revision History 11

1. SEE Testing

1.1 Objective

The testing was intended to find the limits of the power supply input to the IC (PVIN), the output of the internal linear regulator (VCC), and the power supply input for all the CLKOUTx pins (VCCEXT) set by the onset of Destructive Single Event Effects (DSEE) at a LET of 86.3MeV·cm^2/mg (normal incidence gold). Additional testing was intended to identify and quantify SETs and SEFIs occurring in the clock output of the ISL74420SLH and SEUs in the I^{2}C registers. The SET, SEU, and SEFI studies also consisted of irradiation with normal incidence gold (86.3MeV·cm^2/mg).

1.2 Facility

SEE testing was done at the Texas A&M University (TAMU) Radiation Effects Facility of the Cyclotron Institute in College Station, Texas. This facility is coupled to a K500 superconducting cyclotron that can supply a wide range of ion species and flux. The SEE testing in this report was performed on June 4, 2024.

2. Results

2.1 DSEE Results

DSEE testing consisted of three components: PVIN DSEE testing, VCC DSEE testing, and VCCEXT DSEE testing. For all three components, PRESCL and CLKIN were grounded. SCL and SDA were pulled up to VCC through a 4.7kΩ resistor provided by the I^{2}C dongle. OUTEN and MASTER were tied to VCC. OSCTUNE was tied to ground through a 12.7kΩ resistor setting the internal oscillator frequency to 48MHz. CLKOUT0 provided an undivided output of the internal oscillator, CLKOUT1 provided a 24MHz clock output, CLKOUT2 provided a 333.33kHz clock output, and CLKOUT3 provided a 100kHz clock output. The phases for all the clock outputs were set to 0°. The die temperature was +125°C.

2.1.1 PVIN DSEE Results

The purpose of the first component of DSEE testing was to find the maximum value of the power supply input voltage to the IC (PVIN) set by the onset of DSEEs at a die temperature of 125°C. For PVIN DSEE testing, VCC and VCCEXT were bypassed to ground through a 0.68µF capacitor. PVIN was initially set to 13.2V and incremented after each run up to a maximum voltage of 20.7V. Testing ended when the device underwent a DSEE or when PVIN reached 20.7V. The device was considered to have experienced a DSEE if the current on the PVIN pin changed by ±1%.

The results of PVIN DSEE testing are displayed in Table 2. None of the devices exhibited a DSEE during testing. Therefore, the device can be operated with a maximum PVIN value of 20.7V.

The devices were monitored for SEFIs during PVIN DSEE testing. No SEFIs were observed during PVIN DSEE testing.

Table 2. ISL74420SLH PVIN DSEE Test Results

PVIN (V)	DUT #	RUN #	Result	Fluence (ions/cm^2)	I_{PVIN} (±1%)		
					Pre (mA)	Post (mA)	Δ (%)
13.2	1	401	Pass	1E7	45.2	45.1	-0.221
	2	406	Pass	1E7	45.8	45.8	0.000
14.7	1	402	Pass	1E7	45.1	45.1	0.000
	2	407	Pass	1E7	45.7	45.7	0.000
16.5	1	403	Pass	1E7	45.0	45.0	0.000
	2	408	Pass	1E7	45.6	45.7	0.219

Table 2. ISL74420SLH PVIN DSEE Test Results (Cont.)

PVIN (V)	DUT #	RUN #	Result	Fluence (ions/cm^2)	I_{PVIN} (±1%)		
					Pre (mA)	Post (mA)	Δ (%)
18.4	1	404	Pass	1E7	44.9	44.7	-0.445
	2	409	Pass	1E7	45.6	45.6	0.000
	3	411	Pass	1E7	45.5	45.5	0.000
	4	413	Pass	1E7	44.8	44.9	0.223
20.7	1	405	Pass	1E7	44.7	44.8	0.224
	2	410	Pass	1E7	45.7	45.8	0.219
	3	412	Pass	1E7	45.3	45.3	0.000
	4	414	Pass	1E7	44.9	44.8	-0.223

2.1.2 VCC DSEE Results

The purpose of the second component of DSEE testing was to find the maximum value of the linear regulator output (VCC) set by the onset of DSEEs at a die temperature of 125°C. For VCC DSEE testing, the VCC supply was overdriven so that the internal regulator from PVIN was inactive, and the VCC current could be monitored directly. Additionally, PVIN was set to 13.2V, and VCCEXT was set to 3.3V. VCC was initially set to 4.0V and was incremented after each run to a maximum voltage of 5.5V. Testing ended when the device underwent a DSEE or when VCC reached 5.5V. The device was considered to have experienced a DSEE if the current on the PVIN pin or VCC pin changed by ±15%.

The results of VCC DSEE testing are displayed in Table 3. None of the DUTs exhibited DSEEs during testing. Therefore, the device should be operated with a maximum value of VCC = 5.5V to be robust against DSEE.

Table 3. ISL74420SLH VCC DSEE Test Results

VCC (V)	DUT #	RUN #	Result	I_{PVIN} (±15%)			I_{VCC} (±15%)		
				Pre (mA)	Post (mA)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)
4.0	5	415	Pass	52	51	-1.923	27.490	27.450	-0.146
4.5	5	416	Pass	49	47	-4.082	32.929	32.950	0.064
5.0	5	417	Pass	46	46	0.000	38.780	38.750	-0.077
	6	420	Pass	43	45	4.651	38.910	38.880	-0.077
	7	423	Pass	52	51	-1.923	38.92	38.91	-0.026
	8	426	Pass	46	46	0.000	38.88	38.84	-0.103
5.3	5	418	Pass	49	47	-4.082	42.4	42.4	0.000
	6	421	Pass	46	46	0.000	42.6	42.6	0.000
	7	424	Pass	49	44	-10.204	42.62	42.58	-0.094
	8	427	Pass	46	48	4.348	42.53	42.51	-0.047
5.5	5	419	Pass	47	47	0.000	44.98	44.95	-0.067
	6	422	Pass	46	46	0.000	45.18	45.12	-0.133
	7	425	Pass	46	46	0.000	45.21	45.25	0.088
	8	428	Pass	44	46	4.545	45.1	45.08	-0.044

2.1.3 VCCEXT DSEE Results

The purpose of the third component of DSEE testing was to find the maximum value of the power supply inputs to the CLKOUTx pins (VCCEXT) set by the onset of DSEEs at a die temperature of 125°C. For VCCEXT DSEE testing, PVIN was set to 13.2V, and VCC was bypassed to ground through a 0.68µF capacitor. VCCEXT was initially set to 5.7V and was incremented by 0.2V after each run to a maximum voltage of 6.5V. Testing ended when the device underwent a DSEE or when VCC reached 6.5V. The device was considered to have experienced a DSEE if the current on the PVIN or VCCEXT pins changed by ±5%.

The results of VCCEXT DSEE testing are displayed in Table 4. None of the DUTs exhibited DSEEs during testing. Therefore, the device should be operated with a maximum value of VCCEXT = 6.5V to be robust against DSEE.

Table 4. ISL74420SLH VCCEXT DSEE Test Results

VCCEXT (V)	DUT #	RUN #	Result	I_{PVIN} (±1%)			I_{VCCEXT} (±1%)		
				Pre (mA)	Post (mA)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)
5.7	9	429	Pass	21.5	21.4	-0.465	56	56	0.000
5.9	9	430	Pass	21.4	21.3	-0.467	59	59	0.000
6.1	9	431	Pass	21.3	21.3	0.000	62	61	-1.613
	10	434	Pass	21.4	21.4	0.000	62	62	0.000
6.3	9	432	Pass	21.3	21.2	-0.469	64	63	-1.563
	10	435	Pass	21.4	21.4	0.000	64	64	0.000
	11	437	Pass	21.4	21.6	0.935	65	65	0.000
	12	439	Pass	20.5	20.5	0.000	65	65	0.000
6.5	9	433	Pass	21.1	21.1	0.000	66	69	3.030
	10	436	Pass	21.4	21.4	0.000	67	68	1.493
	11	438	Pass	21.6	21.5	-0.463	68	68	0.000
	12	440	Pass	20.5	20.4	-0.488	67	67	0.000

DSEE testing indicates that the device should be operated with the following maximum parameter set to be robust against DSEE: PVIN = 20.7V, VCC = 5.5V, and VCCEXT = 6.5V.

2.2 SET Results

For SET testing, devices were tested in three configurations as given in Table 5. In each of the configurations, PVIN, OUTEN, and VCC_EXT were tied to VCC. SCL and SDA were pulled-up to VCC through 4.7kΩ provided by the I^2C dongle. OSCTUNE was grounded through a 12.7kΩ resistor. The ambient temperature was 25°C.

Table 5. ISL74420SLH SET Test Conditions

Configuration	Number of Devices Tested	Operation Mode	VCC (V)	PRESCL	MASTER	CLKIN
#1	4	Leader Mode using Internal Oscillator	3	GND	VCC	GND
#2	4	Follower Mode	3	VCC	GND	25MHz
#3	4	Leader Mode using External Clock	3	GND	VCC	50MHz

The frequencies of each clock for each configuration are shown in Table 6.

Table 6. ISL74420SLH SET Test Conditions: Clock Frequencies

Configuration	Number of Devices Tested	Operation Mode	CLKOUT0 (MHz)	CLKOUT1 (MHz)	CLKOUT2 (kHz)	CLKOUT3 (kHz)
#1	4	Leader Mode using Internal Oscillator	48	24	333.33	100
#2	4	Follower Mode	25	3.125	43.403	13.021
#3	4	Leader Mode using External Clock	50	25	347.222	104.167

A SET was defined to be when the frequency on one of the CLKOUT pins deviated beyond ±2% of its operating frequency. Additionally, SEFIs were events in which the READY signal pulled low. Oscilloscope triggers were set to capture events where READY pulled below 1V or the frequency on one of the CLKOUT channels deviated beyond ±2% of its operating frequency.

Additionally, the I^2C registers were continually read to monitor for SEUs.

The results of SET testing for the ISL74420SLH are displayed in Table 7. The results are summarized in Table 8.

No SEUs in the I^2C registers were observed.

Table 7. ISL74420SLH SET Test Results

Configuration	Run #	DUT #	Fluence (ions/cm^2)	# of CLKOUT0 SETs	# of CLKOUT1 SETs	# of CLKOUT2 SETs	# of CLKOUT3 SETs	# of SEFIs
#1	441	13	1E7	1	0	0	0	0
	442	14	1E7	4	1	0	0	0
	443	15	1E7	33	0	0	0	0
	444	16	1E7	73	1	0	0	0
#2	445	17	1E7	0	0	0	0	0
	446	18	1E7	0	0	0	0	0
	447	19	1E7	0	0	0	0	0
	448	20	1E7	0	0	0	0	0
#3	449	21	1E7	0	0	0	0	0
	450	22	1E7	0	0	0	0	0
	451	23	1E7	0	0	0	0	0
	452	24	1E7	0	0	0	0	0

Table 8. ISL74420SLH SET Test Results Summary

TC	# of DUTs	Total Fluence (ions/cm^2)	# of CLKOUT 0 SETs	CLKOUT 0 SET σ (μm^2)	# of CLKOUT 1 SETs	CLKOUT 1 SET σ (μm^2)	# of CLKOUT 2 SETs	CLKOUT 2 SET σ (μm^2)	# of CLKOUT 3 SETs	CLKOUT 3 SET σ (μm^2)	# of SEFIs
#1	4	4.0E7	111	277.5	2	5	0	2.5	0	2.5	0
#2	4	4.0E7	0	2.5	0	2.5	0	2.5	0	2.5	0
#3	4	4.0E7	0	2.5	0	2.5	0	2.5	0	2.5	0

SETs only occurred when the ISL74420SLH operated in leader mode using the internal oscillator. All 111 captures on CLKOUT0 were frequency deviation events during which the frequency of the CLKOUT pulse changed beyond the ±2% window. However, no pulses were missed during any of the events. Figure 2 shows a typical CLKOUT0 capture. There was not a localized SET event, and the pulses are visually indistinguishable.

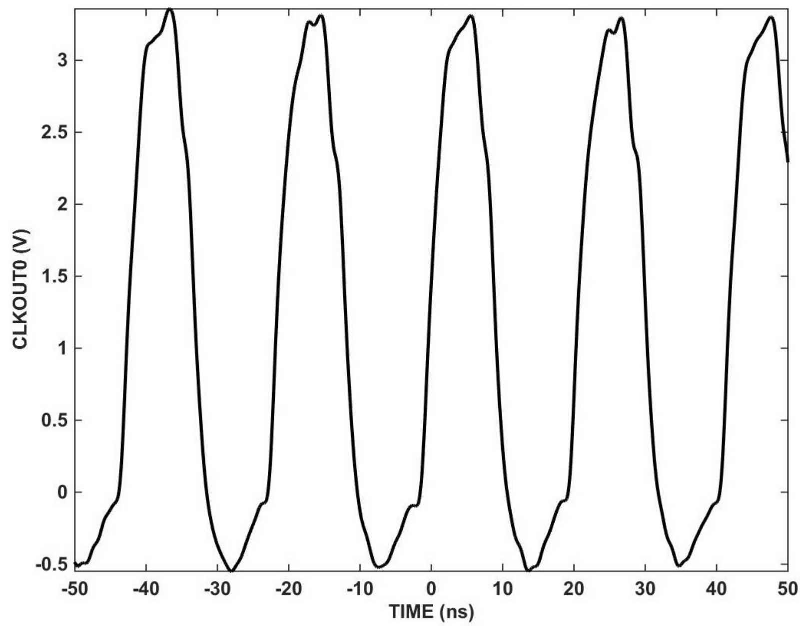

Figure 2. Typical SET Capture on CLKOUT0

Figure 3 shows the distribution of the CLKOUT0 triggered frequency deviations. The red lines indicate the ±2% window.

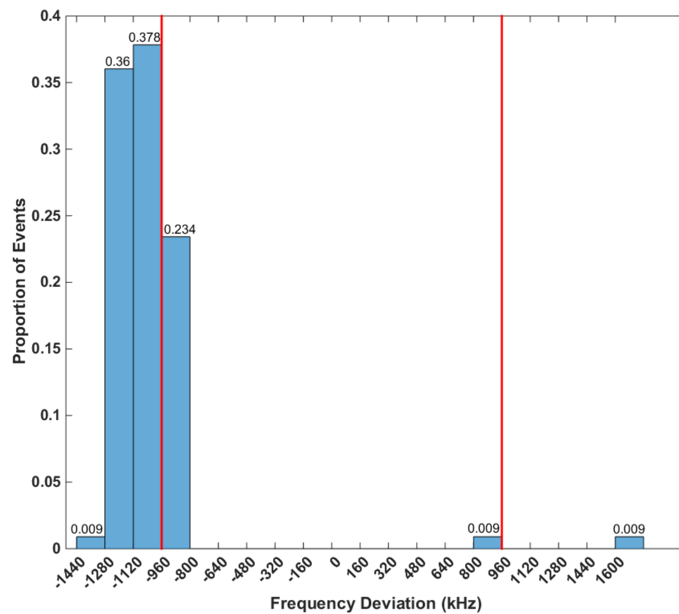

Figure 3. CLKOUT0 Triggered Frequency Deviations

All the frequency deviations on CLKOUT0 recovered by the next pulse.

The two captures on CLKOUT1 were also frequency deviations. Figure 4 shows a typical capture on CLKOUT1. Similar to the captures on CLKOUT0, there was a not a localized SET, and the pulses were visually indistinguishable.

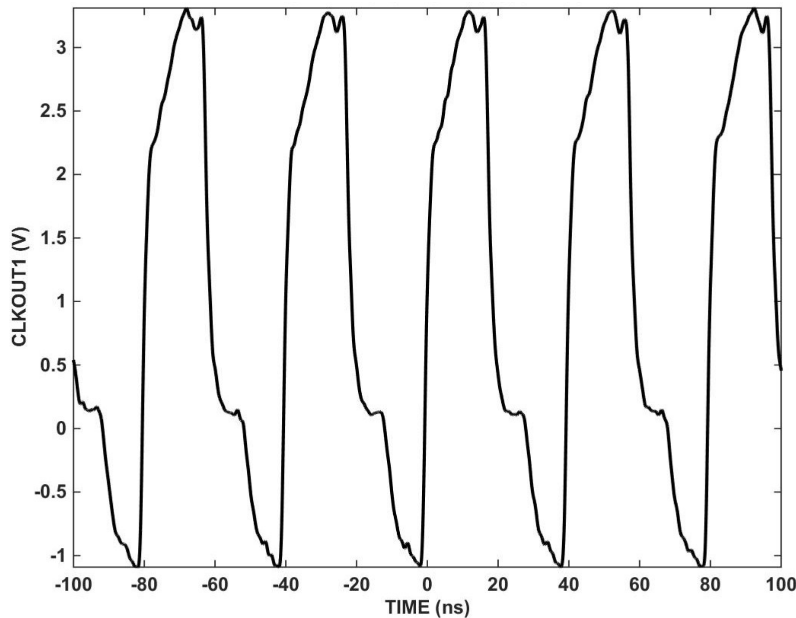

Figure 4. Typical SET Capture on CLKOUT1

Figure 5 shows the distribution of the CLKOUT1 triggered frequency deviations. The red lines indicate the ±2% window.

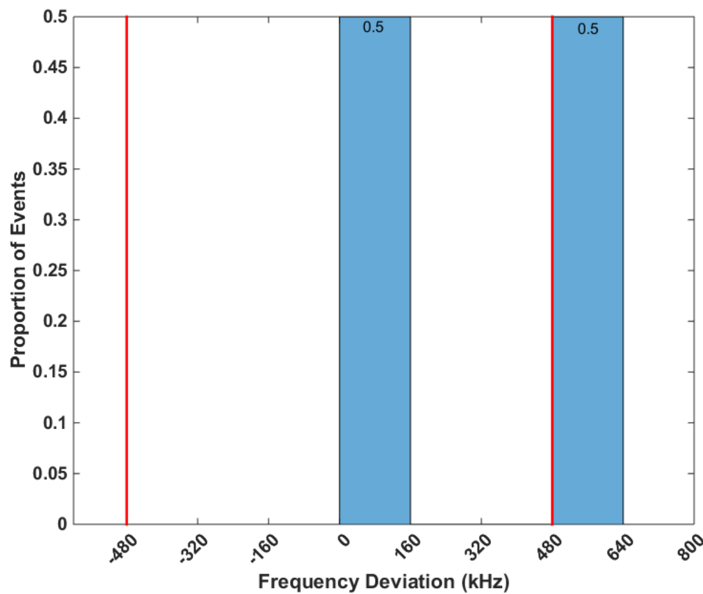

Figure 5. CLKOUT1 Triggered Frequency Deviations

One of the events had 12 pulses with frequency deviations beyond the ±2% window while the other had 13 pulses beyond the window.

CLKOUT2 and CLKOUT3 did not have any SETs. THE ISL74420SLH did not exhibit any SEFIs.

3. Discussion and Conclusion

All SEE testing was performed with normal incidence gold for a LET of 86.3MeV·cm^2/mg at the surface of the device.

DSEE testing demonstrated the device could be operated with the following maximum parameter set to be robust against DSEE: PVIN = 20.7V, VCC = 5.5V, and VCCEXT = 6.5V.

The ISL74420SLH did not exhibit any missing pulse events, SEFIs, or SEUs.

There were 111 frequency deviation SETs on CLKOUT0 and 2 frequency deviation SETs on CLKOUT1 when operating the ISL74420SLH in leader mode using the internal oscillator. However, given the rarity of the events, the immediate recovery on CLKOUT0, and the lack of a well-defined signature, the frequency deviation SETs are fairly innocuous.

4. Revision History

Revision	Date	Description
1.00	Jun 20, 2025	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

© 2025 Renesas Electronics Corporation. All rights reserved.