ISL71090SEH

Single Event Effects (SEE)

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Introduction

The intense proton and heavy ion environment encountered in space applications can cause a variety of single event effects in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI) and Single Event Burnout (SEB). SEE can lead to system-level performance issues including disruption, degradation and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. This report discusses the results of SEE testing performed on the ISL71090SEH product family of precision references.

Product Description

The ISL71090SEH is an ultra low noise, high DC accuracy precision voltage reference product family with a wide input range of 4V to 30V. Four voltage variants are available, 1.25V (ISL71090SEH12), 2.5V (ISL71090SEH25), 5.0V (ISL71090SEH50) and 7.5V (ISL71090SEH75). The ISL71090SEH uses Intersil's PR40 Advanced Bipolar technology to achieve sub $2\mu V_{P-P}$ noise at 0.1Hz and achieve 0.15% accuracy over-temperature and total ionizing dose radiation. Implementation in an advanced bonded wafer SOI process using deep trench isolation results in fully isolated structures and latch-up free performance, whether electrically or single event (SEL) caused.

Product Documentation

For more information about the ISL71090SEH, refer to the documentation shown below.

- ISL71090SEH12, ISL71090SEH25, ISL71090SEH50, ISL71090SEH75 Datasheets
- SMD: 5962-13211
- AN1847 - "ISL71090SEHxx User Guide"
- AN1849 - "Total Dose Testing of the ISL71090SEH Precision Voltage Reference"

SEE Test Objectives

The ISL71090SEH was tested to determine its susceptibility to SEB and to characterize its SET behavior over various linear energy transfer (LET) ion levels.

SEE Test Facility

Testing was performed at the Texas A&M University (TAMU) Cyclotron Institute heavy ion facility. This facility is coupled to a K500 super-conducting cyclotron, which is capable of generating a wide range of test particles with the various energy, flux and fluence levels needed for advanced radiation testing.

SEE Test Setup

SEE testing is carried out with the sample in an active configuration. A schematic of the ISL71090SEH SEE test fixture is shown in Figure 1 on page 2. The test circuit is configured to accept an input voltage from 4V to 30V and generate the nominal output voltage. The output current of the reference was adjusted using fixed load resistors on test board. The output capacitor, C_4, and the compensation capacitor C_2 were varied for some tests between 0.1µF to 10µF and 1nF to 10nF respectively.

Four ISL71090SEH test fixtures were mounted to a test jig, which could be moved with respect to the ion beam. The parts were assembled in dual in-line packages with the metal lid removed for beam exposure. Using 20-foot coaxial cables, the test jig was connected to a switch box in the control room, which contained all of the monitoring equipment. The switch box allowed any one of the four test circuits to be controlled and monitored remotely. Later testing utilized a board with four units mounted to allow them to be irradiated and monitored simultaneously.

Digital multimeters were used to monitor input voltage (V_{IN}), output voltage (V_{OUT}) and input current (I_{IN}). LeCroy *wave*Runner 4-channel digital oscilloscopes were used to set the trigger levels and to monitor, capture and store key signal waveforms. Table 1 shows the scope configurations used during the testing.

TABLE 1. OSCILLOSCOPE CONFIGURATIONS

SCOPE	CHANNEL 1	TRIGGER SIGNAL	TRIGGER LEVEL
1	V_{OUT}	V_{OUT}	$\Delta V = \pm 20mV$
2	V_{OUT}	V_{OUT}	$\Delta V = \pm 75mV$

SEB Testing

For the SEB tests, conditions were selected to maximize the electrical and thermal stresses on the device under test (DUT), thus insuring worst-case conditions. The input voltage (V_{IN}) was initially set to 35V and then increased in 1V increments. The capacitors were set to C_{OUT} = 0.1µF and C_{COMP} = 1nF. SEB testing was conducted with the ISL71090SEH25, hence the output voltage (V_{OUT}) was 2.5V. Output current (I_{OUT}) was set to 20mA which is the maximum recommended current rating for load regulation of the device. Case temperature was maintained at +125°C by controlling the current flowing into a resistive heater bonded to the underside of the DUT. This ensured that the junction temperature of the DUT exceeded +125°C, which is the maximum junction temperature anticipated for high reliability applications. Four DUTs were irradiated with Au ions at a normal incident angle, resulting in an effective LET of 86.4MeV • cm^2/mg. Table 2 summarizes the results of SEB testing. The chart shows sample size and passing results for an input voltage level of 37V on each device.

The failure criterion for destructive SEE was an increase in operating input current (I_{IN}) greater than 5% measured at 20mA output current. I_{IN} is defined as the total current drawn by the device. Failed devices were not further irradiated.

From a design perspective, all the products in the ISL71090SEH product family are exactly the same in silicon. The output voltage, even though they are different values, are produced the same way and trimmed through a resistor ladder network. All the parts are built in the same process and are functionally equivalent. Therefore, all ISL71090SEH25 SEB results are applicable to the complete product family.

TABLE 2. ISL71090SEH SEB TEST RESULTS. SAMPLES WERE TESTED WITH INCREASING INPUT VOLTAGE (V_{IN}) UNTIL FAILURE.

TEMPERATURE (°C)	LET	SUPPLY CURRENT PRE-EXPOSURE (mA)	SUPPLY CURRENT POST- EXPOSURE (mA)	LATCH EVENTS	CUMULATIVE FLUENCE (PARTICLES/cm^2)	DEVICE ID	SEB/L
+125	86.3	21.364	21.365	0	2.00E+06	1	PASS
+125	86.3	21.379	21.376	0	2.00E+06	2	PASS
+125	86.3	21.359	21.358	0	2.00E+06	3	PASS
+125	86.3	21.356	21.354	0	2.00E+06	4	PASS
		Total Events		0			
		Overall Fluence			8.00E+06		
		Total Units				4	

NOTE: The chart shows sample size and pass results for the input voltage level of 37V as well as the total effective fluence for each level.

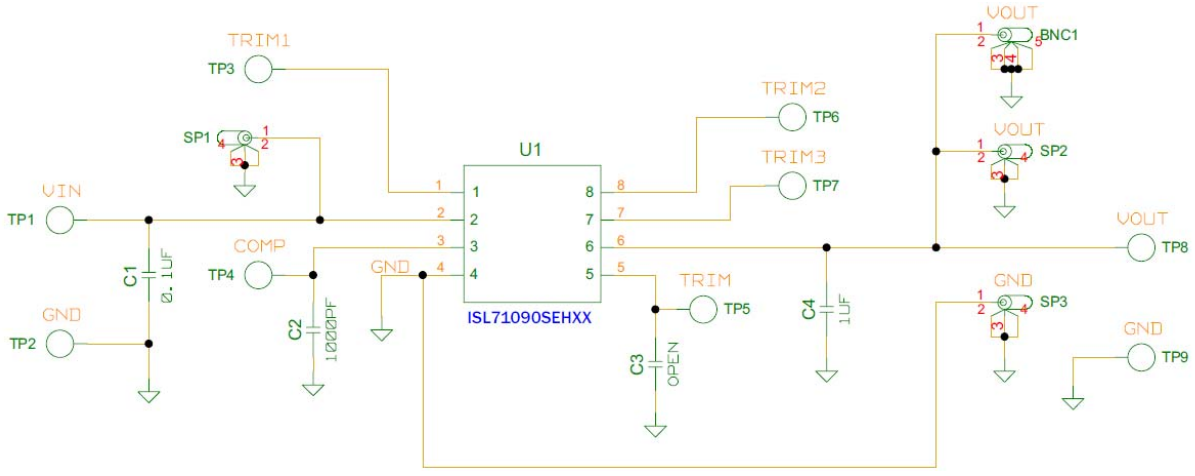

FIGURE 1. SCHEMATIC OF THE ISL71090SEH SEE TEST CIRCUIT

SET Testing of ISL71090SEH25, 2.5V Output Samples

The first set of SET testing of the ISL71090SEH family was done on four samples of the ISL71090SEH25, which were irradiated at room temperature across a range of LET from 2.7MeV•cm^2/mg to 86.4MeV•cm^2/mg to observe SET performance. Samples were separately tested to V_{IN} of 4V and 30V. The parts were configured with 0.1µF output capacitor, 1nF compensation capacitor and 20mA load current to set up the worst conditions for negative going transients. Table 3 shows the SET summary giving the cross section for each input voltage and LET level. Figure 2 is the LET threshold plot produced from the SET summary table.

Figures 3 through 12 represent output waveform responses of the DUTs at the respective bias conditions and LET levels. The plots are composites of all the transients captured on the scope. This information is useful in quantifying the excursion of the output voltage as a result of SEE induced transients.

The worst case SET appeared for the case of LET = 56 and V_{IN} = 4V with about 340mV in negative SET. The second worst case appeared for LET = 86 and V_{IN} = 4V at about 325mV. The longest recovery times were about 50µs.

TABLE 3. SET SUMMARY OF FULLY FUNCTIONAL ISL71090SEH25 SAMPLES AT 4.0V AND 30V INPUT VOLTAGE., C_{OUT} = 0.1µF, C_{COMP} = 1nF AND I_{OUT} = 20mA. TRIGGER LEVEL FOR THE OUTPUT VOLTAGE SET TO ±20mV.

SUPPLY VOLTAGE (V)	ION/ANGLE	EFF LET (MeV•cm^2/mg)	FLUENCE PER RUN (PARTICLES/cm^2)	NUMBER OF RUNS	TOTAL SET	EVENTS CS (cm^2)
4	Ne/0	2.7	2.00E+06	4	40	5.00E-06
30	Ne/0	2.7	2.00E+06	4	6	7.50E-07
4	Ar/0	8.5	2.00E+06	4	256	3.20E-05
30	Ar/0	8.5	2.00E+06	4	365	4.56E-05
4	Kr/0	28	2.00E+06	4	439	5.49E-05
30	Kr/0	28	2.00E+06	4	754	9.43E-05
4	Kr/60	56	2.00E+06	2	365	9.13E-05
30	Kr/60	56	2.00E+06	2	590	1.48E-04
4	Au/0	86.3	2.00E+06	4	609	7.61E-05
30	Au/0	86.3	2.00E+06	4	944	1.18E-04

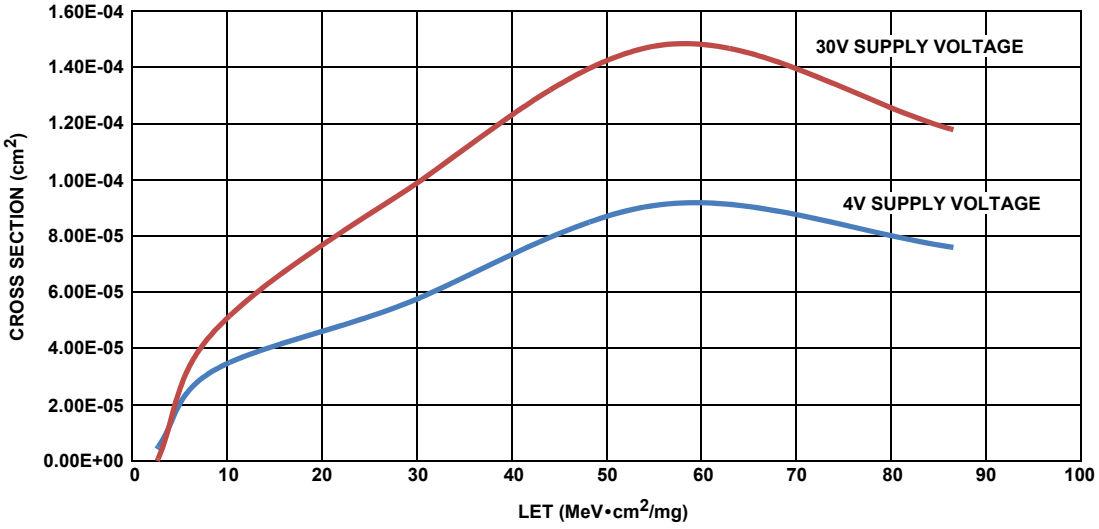

FIGURE 2. ISL71090SEH25 LET THRESHOLD PLOT FOR ±20mV TRIGGER WINDOW WITH C_{OUT} = 0.1µF, C_{COMP} = 1nF AND I_{OUT} = 20mA

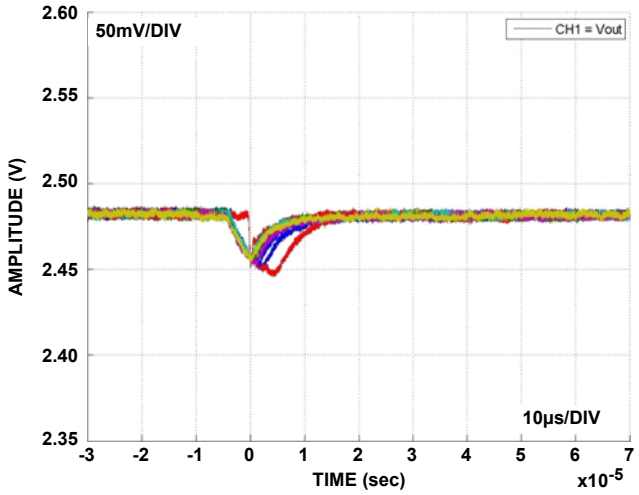

FIGURE 3. COMPOSITE SET PLOT FOR ISL71090SEH25 AT LET 2.7 V_{IN} = 4V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 1nF

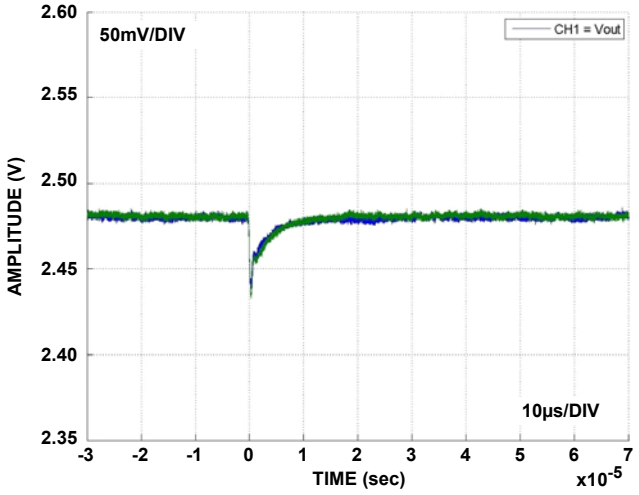

FIGURE 4. COMPOSITE SET PLOT FOR ISL71090SEH25 AT LET 2.7 V_{IN} = 30V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 1nF

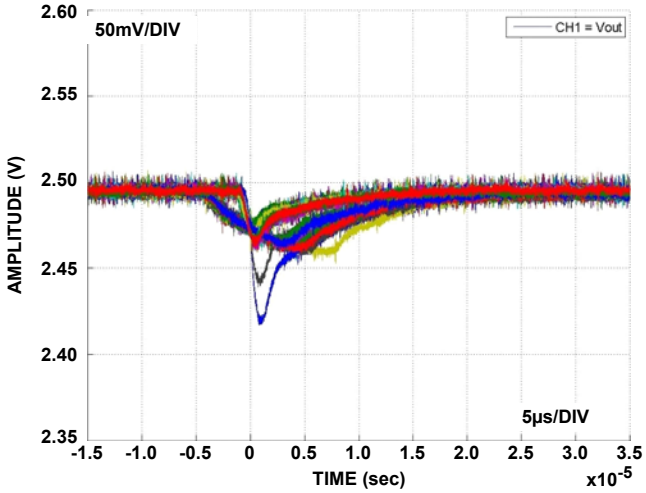

FIGURE 5. COMPOSITE SET PLOT FOR ISL71090SEH25 AT LET 8.5 V_{IN} = 4V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 1nF

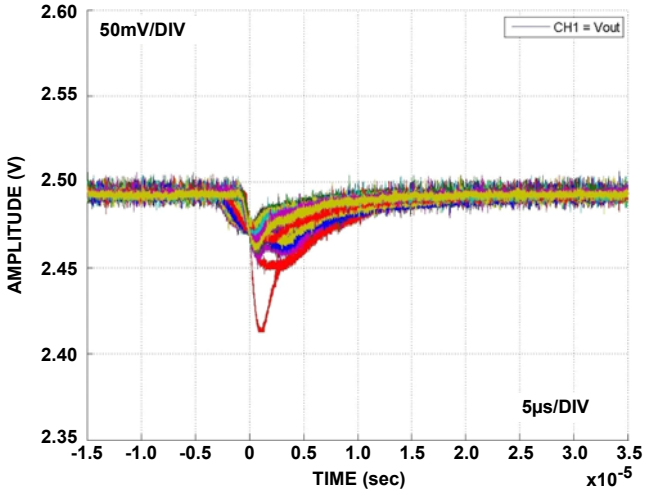

FIGURE 6. COMPOSITE SET PLOT FOR ISL71090SEH25 AT LET 8.5 V_{IN} = 30V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 1nF

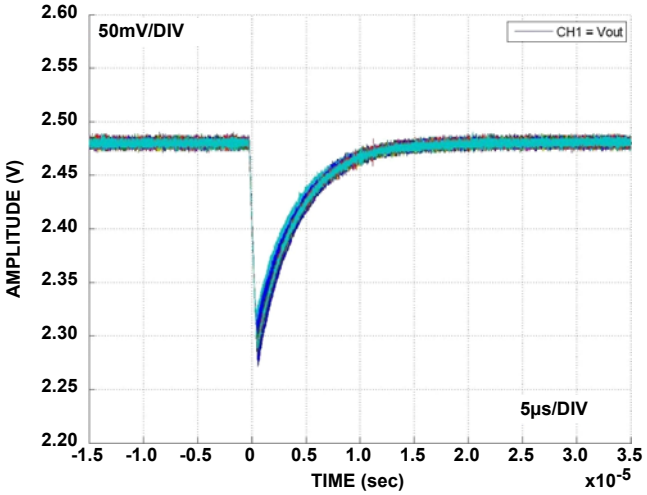

FIGURE 7. COMPOSITE SET PLOT FOR ISL71090SEH25 AT LET 28 V_{IN} = 4V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 1nF

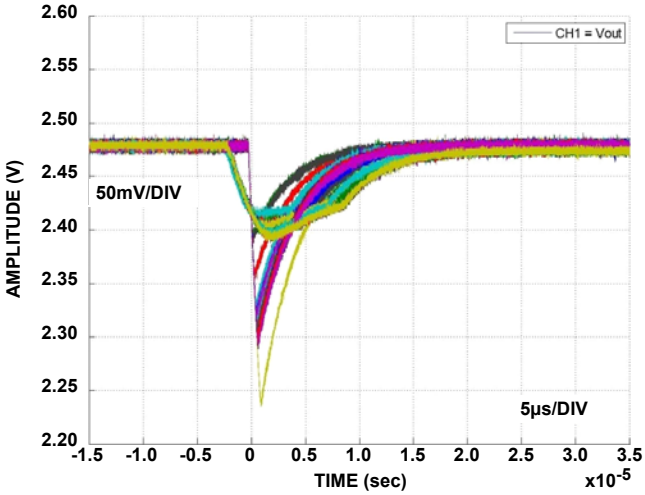

FIGURE 8. COMPOSITE SET PLOT FOR ISL71090SEH25 AT LET 28 V_{IN} = 30V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 1nF

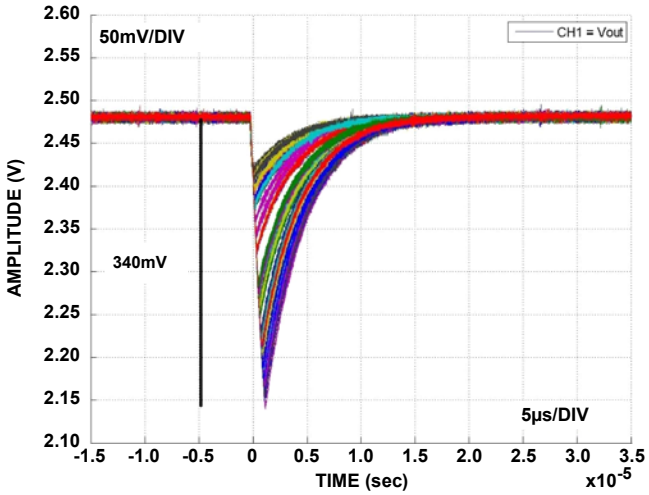

FIGURE 9. COMPOSITE SET PLOT FOR ISL71090SEH25 AT LET 56 V_{IN} = 4V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 1nF

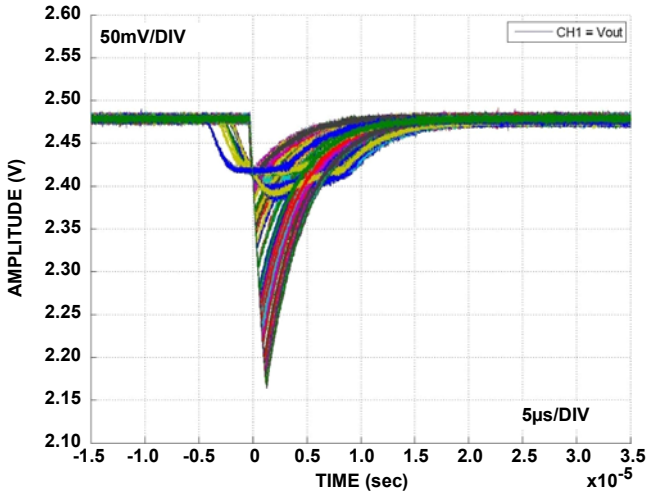

FIGURE 10. COMPOSITE SET PLOT FOR ISL71090SEH25 AT LET 56 V_{IN} = 30V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 1nF

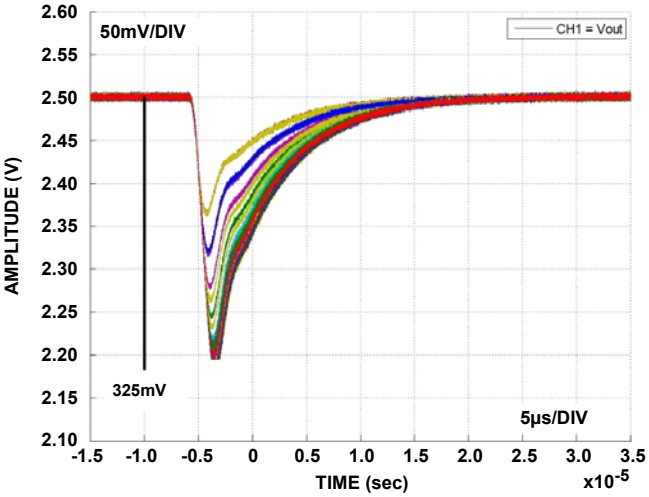

FIGURE 11. COMPOSITE SET PLOT FOR ISL71090SEH25 AT LET 86 V_{IN} = 4V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 1nF. THE SCOPE CAPTURE WAS TRUNCATED AT 2.2V

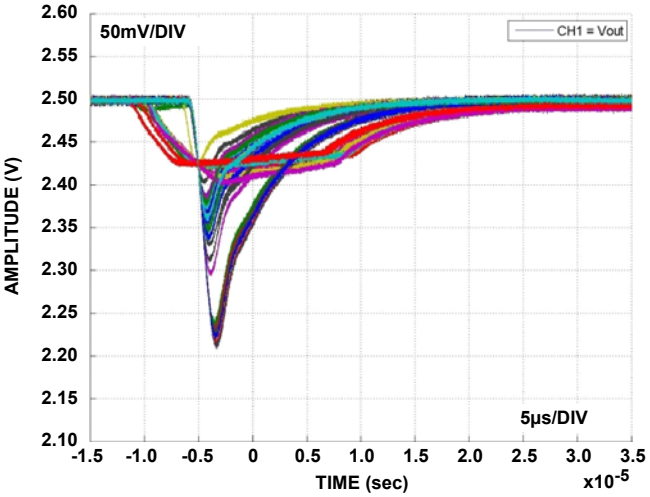

FIGURE 12. COMPOSITE SET PLOT FOR ISL71090SEH25 AT LET 86 V_{IN} = 30V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 1nF

SET Testing of ISL71090SEH12, 1.25V Output Samples

Two samples of the ISL71090SEH12 were irradiated at room temperature at LET 58 to observe SET performance. Samples were separately tested to V_{IN} of 4V and 30V. Table 4 shows the SET summary for this initial testing.

Figures 13 and 14 are composite plots of all the transients captured on the scope in this SET test condition for the ISL71090SEH12. Again these two parts were operated with C_{OUT} = 0.1µF, C_{COMP} = 1nF, and I_{OUT} = 20mA.

TABLE 4. SET SUMMARY OF FULLY FUNCTIONAL ISL71090SEH12 SAMPLES AT 4.0V AND 30V INPUT VOLTAGE. TRIGGER LEVEL FOR THE OUTPUT VOLTAGE SET TO ±20mV.

SUPPLY VOLTAGE (V)	ION/ANGLE	EFF LET (MeVcm^2/mg)	FLUENCE PER RUN (PARTICLES/cm^2)	NUMBER OF RUNS	TOTAL SET	EVENTS CS (cm^2)
4	Pr/0	58	2.00E+06	2	150	7.5E-05
30	Pr/0	58	2.00E+06	2	256	1.28E-04

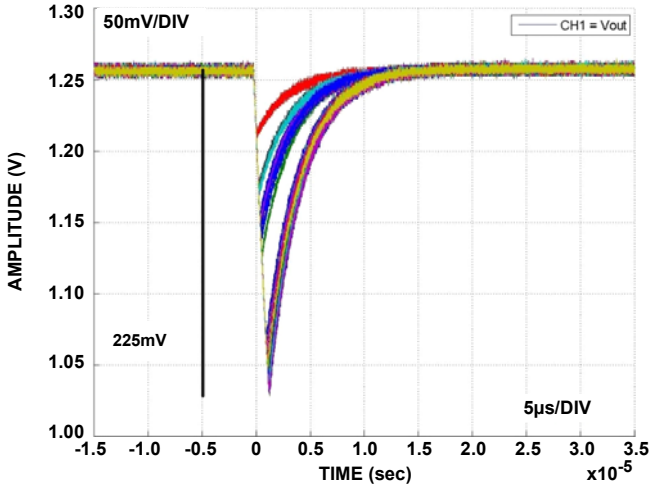

FIGURE 13. COMPOSITE SET PLOT FOR ISL71090SEH12 AT LET 58 V_{IN} = 4V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 1nF

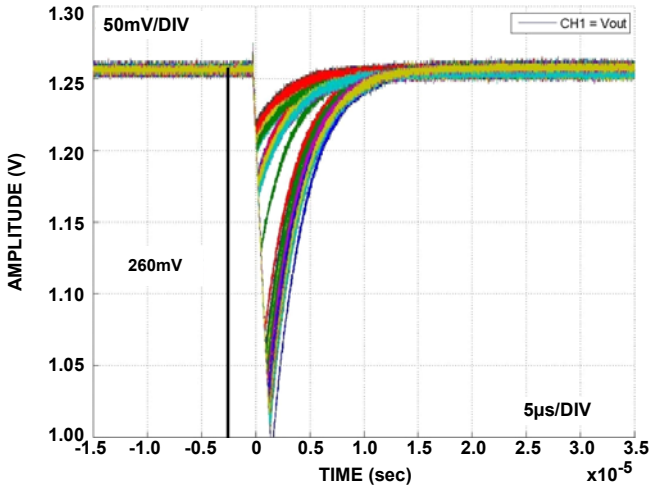

FIGURE 14. COMPOSITE SET PLOT FOR ISL71090SEH12 AT LET 58 V_{IN} = 30V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 1nF. THE SCOPE CAPTURE WAS TRUNCATED AT 1.0V

SET Testing of ISL71090SEH75, 7.50V Output Samples

Four samples of the 7.5V part, ISL71090SEH75, were run for SET with I_{OUT} = 20mA, C_{OUT} = 0.1µF, V_{IN} = 9.2V and 30V, at LET = 8.5, 28, and 56 MeV•cm^2/mg. The summary of the testing is below. Table 5 provides the SET count versus LET summary and Figure 15 shows a plot of the SET cross section (events/fluence). The first two parts had C_{OUT} = 0.1µF and C_{COMP} = 1nF (datasheet recommendation). Composite SET plots for one of these two parts are shown in Figures 16 and 17.

TABLE 5. SET SUMMARY OF FULLY FUNCTIONAL ISL71090SEH75 SAMPLES AT 9.2V AND 30V INPUT VOLTAGE. TRIGGER LEVEL FOR THE OUTPUT VOLTAGE SET TO ±75mV.

SUPPLY VOLTAGE (V)	LET (MeV•cm^2/mg)	FLUENCE (PARTICLES/cm^2)	EVENTS (±75mV)	σ (cm^2)
9.2	8.5	8.00E+06	342	4.28E-05
30	8.5	8.00E+06	430	5.38E-05
9.2	28	8.00E+06	866	1.08E-04
30	28	8.00E+06	1186	1.48E-04
9.2	56	8.00E+06	827	1.03E-04
30	56	8.00E+06	1359	1.70E-04

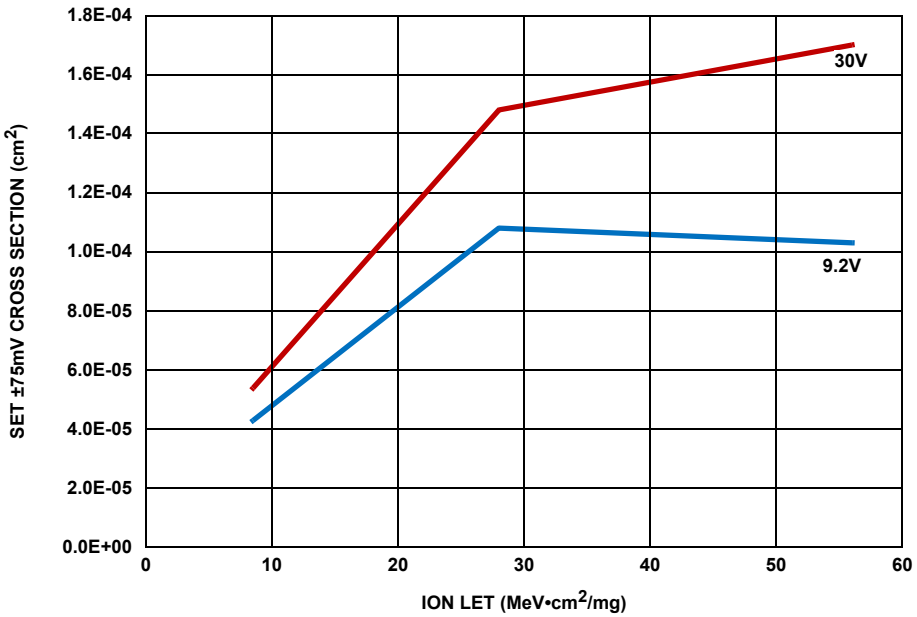

FIGURE 15. ISL71090SEH75 LET THRESHOLD PLOT FOR ±75mV TRIGGER WINDOW WITH C_{OUT} = 0.1µF AND I_{OUT} = 20mA

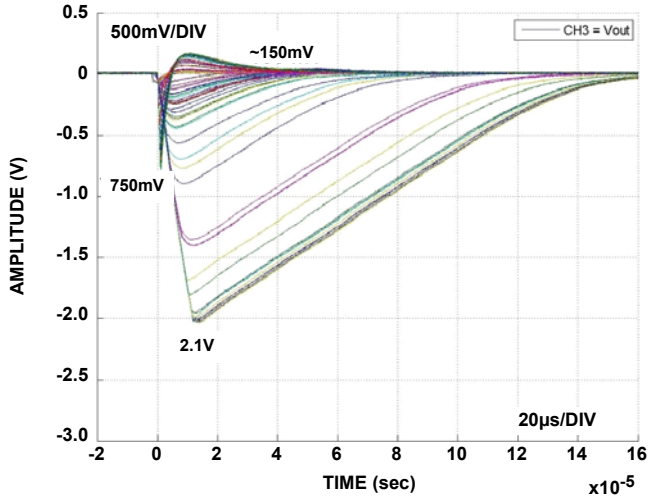

FIGURE 16. COMPOSITE SET PLOT FOR ISL71090SEH75 AT LET 56 V_{IN} = 9.2V, C_{OUT} = 0.1µF, C_{COMP} = 1nF

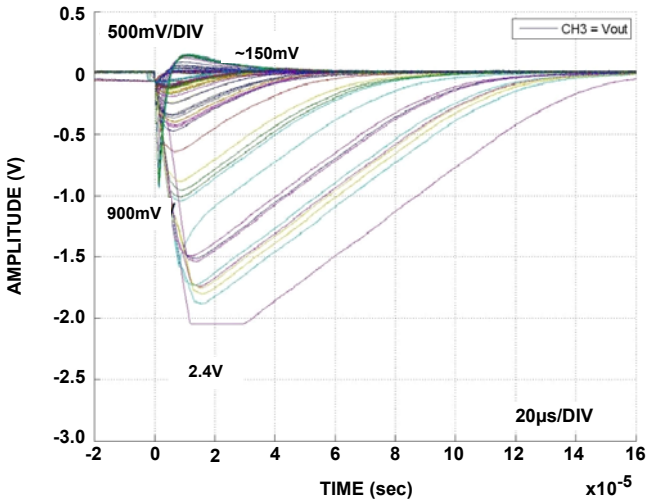

FIGURE 17. COMPOSITE SET PLOT FOR ISL71090SEH75 AT LET 56 V_{IN} = 30V, C_{OUT} = 0.1µF, C_{COMP} = 1nF

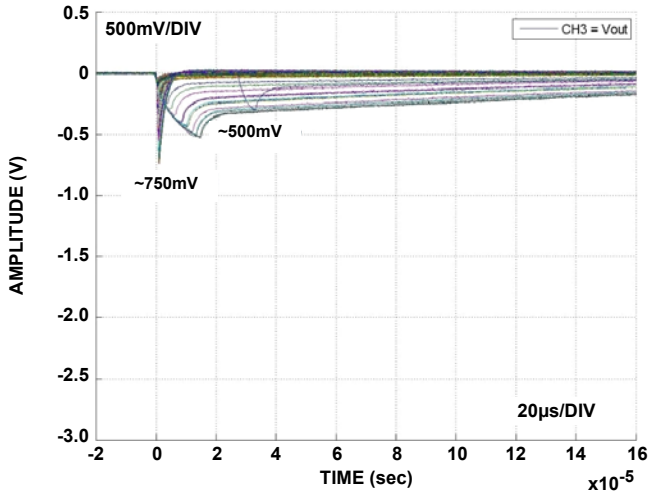

FIGURE 18. COMPOSITE SET PLOT FOR ISL71090SEH75 AT LET 56 V_{IN} = 9.2V, C_{OUT} = 0.1µF, C_{COMP} = 10nF

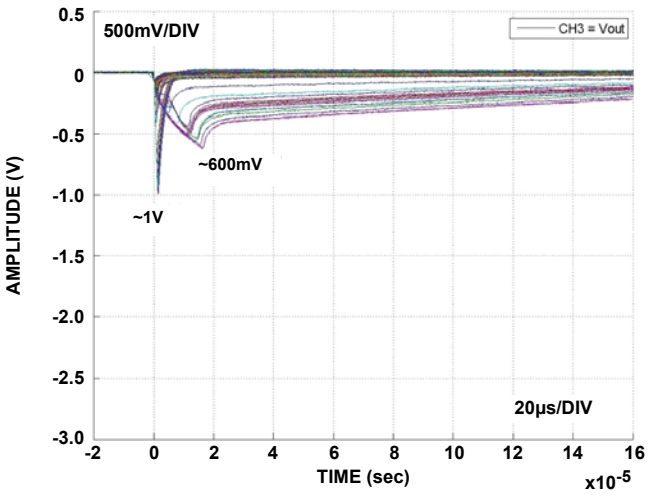

FIGURE 19. COMPOSITE SET PLOT FOR ISL71090SEH75 AT LET 56 V_{IN} = 30V, C_{OUT} = 0.1µF, C_{COMP} = 10nF

The SET displayed above exhibit two forms. The first is a very rapid drop in voltage to close to -1V from regulation and followed by a rapid recovery and substantial overshoot (100mV to 150mV). The type exhibits a slower and prolonged drop in output voltage with terminal values -2.5V from regulation. Recovery from the second form is slower but does not show a pronounced overshoot.

Two more ISL71090SEH75 parts were then tested with C_{COMP} = 10nF but still with C_{OUT} = 0.1µF. The results from one of these parts are shown in Figures 18 and 19.

The higher value of C_{COMP} significantly reduced the SET. The long slow SET was reduced from ~2.5V to ~600mV and the sharp SET was essentially unchanged with a magnitude of about 1V but without the recovery overshoot. So, from an SET mitigation perspective, the bandwidth limiting of the larger C_{COMP} is preferable.

The SET resulting from ions (Ar) with LET = 8.5MeV • cm^2/mg are shown in Figures 20 and 21. Even at this low LET the part exhibited SET of 400mV magnitude.

Four more ISL71090SEH75 parts were run for SET testing to explore the impact of capacitor selection as described in Table 6 on page 9.

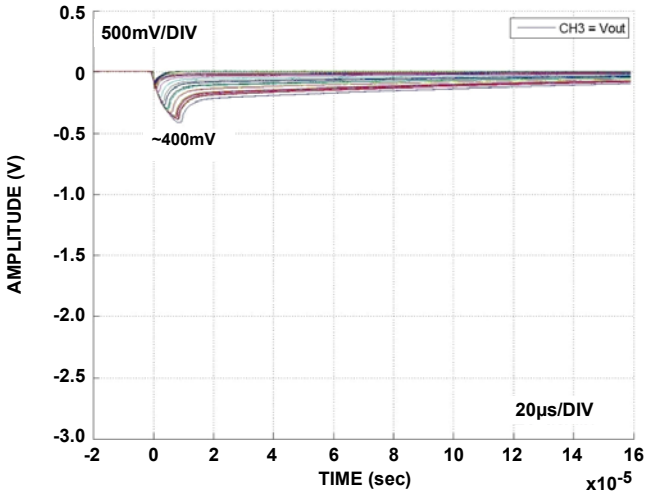

FIGURE 20. COMPOSITE SET PLOT FOR ISL71090SEH75 AT LET 8.5 V_{IN} = 9.2V, C_{OUT} = 0.1µF, C_{COMP} = 10nF

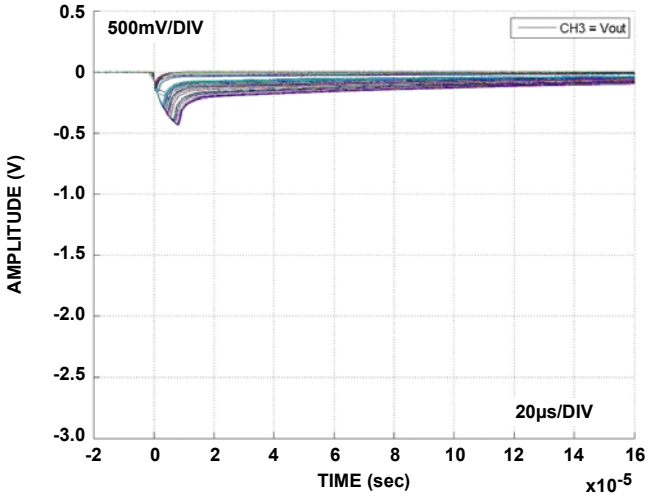

FIGURE 21. COMPOSITE SET PLOT FOR ISL71090SEH75 AT LET 8.5 V_{IN} = 30V, C_{OUT} = 0.1µF, C_{COMP} = 10nF

TABLE 6. SUMMARY OF CONDITIONS FOR SECOND ROUND OF SET RUNS ON THE ISL71090SEH75

RUN	LET (MeV•cm²/mg)	IOUT (mA)	VIN (V)	SET COUNTS (±20mV), 4E+06 ION/CM²			
				C_{OUT} = 1µF C_{COMP} = 1nF	C_{OUT} = 1µF C_{COMP} = 10nF	C_{OUT} = 10µF C_{COMP} = 10nF	
				DUT 1	DUT 2	DUT 3	DUT 4
311	28	-10	9.2	832	87	210	55
312			30	1074	115	312	71
313		20	9.2	869	231	224	72
314			30	**1193**(Figure 22)	238	**304**(Figure 24)	97
211	8.5	-10	9.2	221	52	60	40
212			30	317	69	93	50
213		20	9.2	265	67	55	60
214			30	314	83	91	72
111	2.7	-10	9.2	154	28	21	22
112			30	133	6	2	2
113		20	9.2	147	12	20	25
114			30	**120**(Figure 23)	17	16	27

NOTE: Bold entries with superscripts are shown as composite plot figures.

Figure 22 shows a composite of large negative going SET for DUT1 run 314. The worst of these SET bottom out at about -1.4V deviation. These are about 175µs at return to cross nominal before overshooting about 100mV. Certainly not all of the SET are this severe, but a good number are. Even at LET of 2.7MeV•cm^2/mg (DUT1 run 114) Figure 23 shows a few SET to -600mV. Clearly the part is sensitive to lower LET ions. Comparing Figures 22 and 24 shows the impact of going to larger capacitors (C_{OUT} from 1µF to 10µF and C_{COMP} from 1nF to 10nF). The change reduces worst SET for LET 27 deviations from -1.4V to 0.18V, though the recovery time is considerably stretched out.

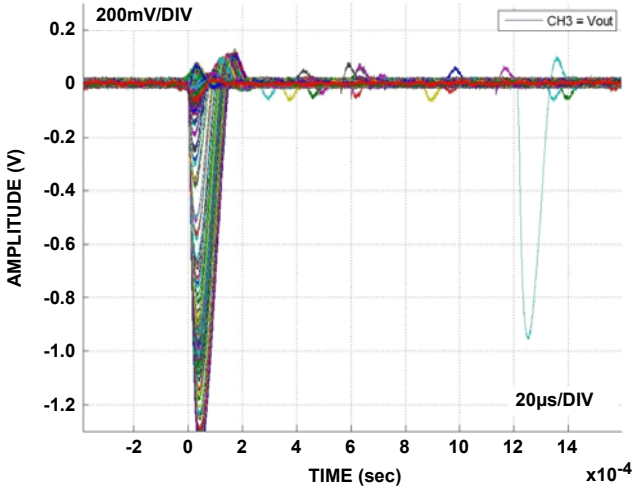

FIGURE 22. COMPOSITE SET PLOT FOR ISL71090SEH75 AT LET 28 V_{IN} = 30V, I_{OUT} = 20mA, C_{OUT} = 1µF, C_{COMP} = 1nF

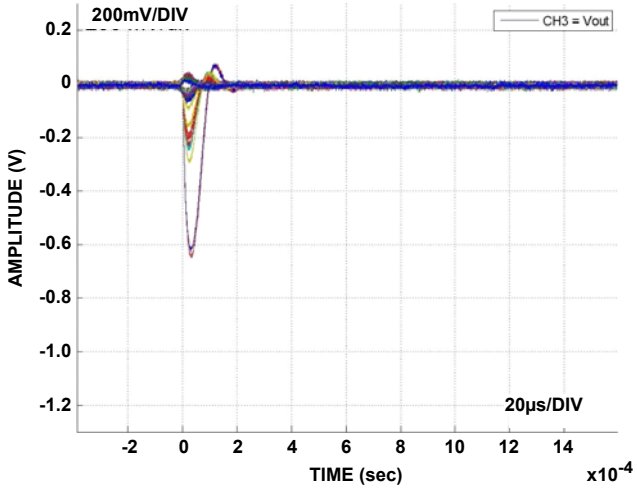

FIGURE 23. COMPOSITE SET PLOT FOR ISL71090SEH75 AT LET 2.7 V_{IN} = 30V, I_{OUT} = 20mA, C_{OUT} = 1µF, C_{COMP} = 1nF

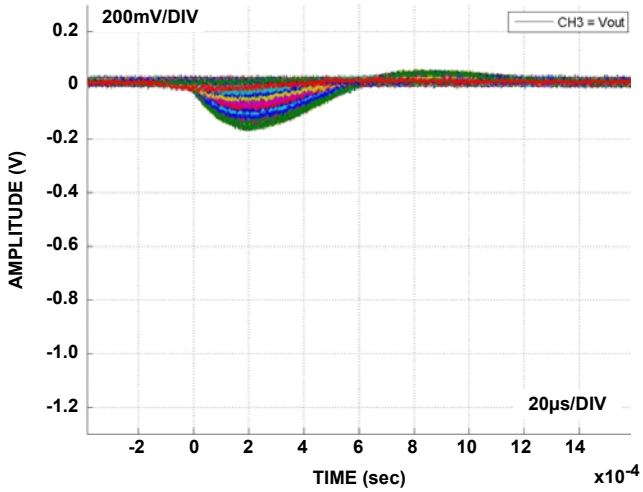

FIGURE 24. COMPOSITE SET PLOT FOR ISL71090SEH75 AT LET 28, V_{IN} = 30V, I_{OUT} = 20mA, C_{OUT} = 10µF, C_{COMP} = 10nF

SET Testing of ISL71090SEH50, 5.0V Output Samples

Four samples of the 5.0V part, ISL71090SEH50, were run for SET with I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 10nF, V_{IN} = 7V and 30V, at LET = 8.5, 28 and 56MeV • cm^2/mg. The C_{COMP} was set to 10nF as it was determined to be better at suppressing SET on the 7.5V device. Table 7 summarizes the SET event counts versus LET and bias conditions. Figure 25 provides plots of the SET cross section versus LET. The composite SET plots for one device in each of these six irradiation runs appear in Figures 26 through 31.

TABLE 7. SET SUMMARY OF FULLY FUNCTIONAL ISL71090SEH50 SAMPLES AT 7V AND 30V INPUT VOLTAGE. TRIGGER LEVEL FOR THE OUTPUT VOLTAGE SET TO ±50mV.

SUPPLY VOLTAGE (V)	LET (MeV • cm^2/mg)	FLUENCE (PARTICLES/cm^2)	EVENTS (±50mV)	σ (cm^2)
7	8.5	8.00E+06	375	4.69E-05
30	8.5	8.00E+06	442	5.53E-05
7	28	8.00E+06	743	9.29E-05
30	28	8.00E+06	1073	1.34E-04
7	56	8.00E+06	950	1.19E-04
30	56	8.00E+06	1308	1.64E-04

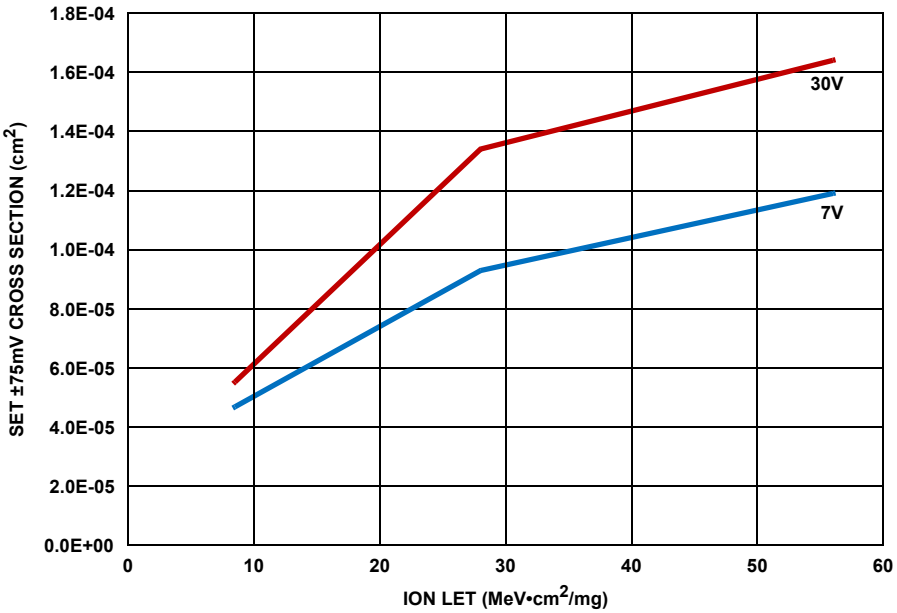

FIGURE 25. ISL71090SEH50 LET THRESHOLD PLOT FOR ±50mV TRIGGER WINDOW WITH C_{OUT} = 0.1µF AND I_{OUT} = 20mA

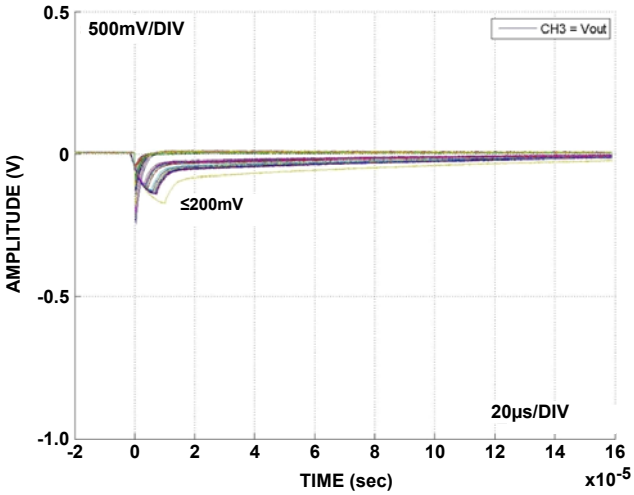

FIGURE 26. COMPOSITE SET PLOT FOR ISL71090SEH50 AT LET 8.5 V_{IN} = 7V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 10nF

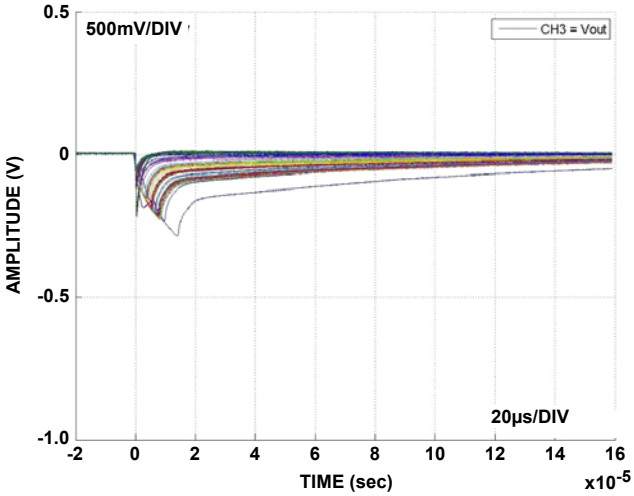

FIGURE 27. COMPOSITE SET PLOT FOR ISL71090SEH50 AT LET 8.5 V_{IN} = 30V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 10nF

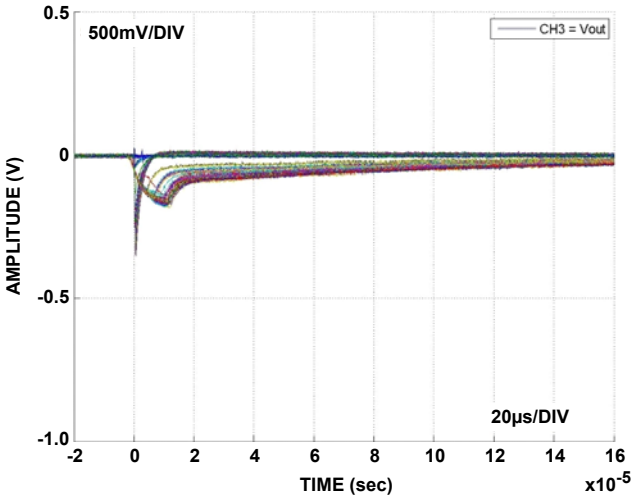

FIGURE 28. COMPOSITE SET PLOT FOR ISL71090SEH50 AT LET 28 V_{IN} = 7V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 10nF

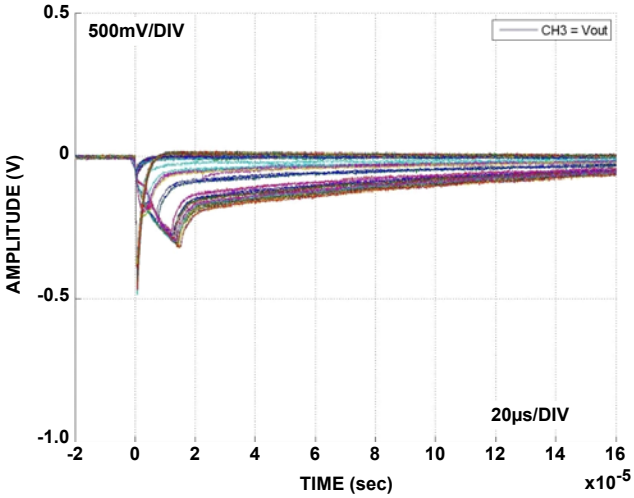

FIGURE 29. COMPOSITE SET PLOT FOR ISL71090SEH50 AT LET 28 V_{IN} = 30V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 10nF

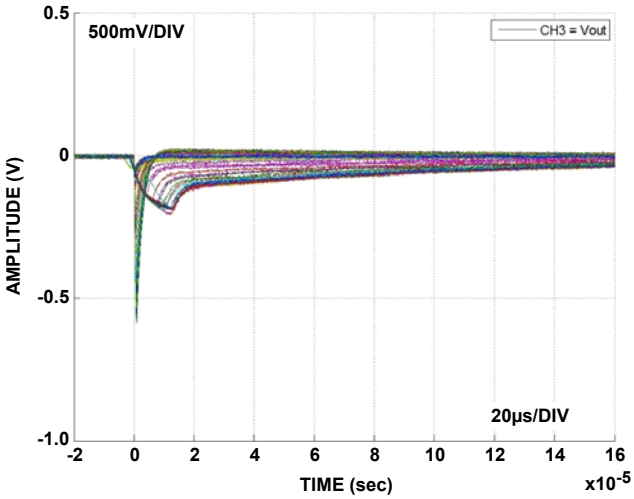

FIGURE 30. COMPOSITE SET PLOT FOR ISL71090SEH50 AT LET 56 V_{IN} = 7V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 10nF

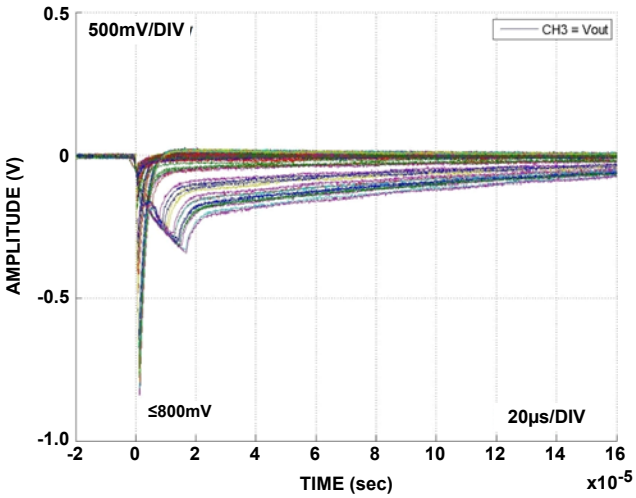

FIGURE 31. COMPOSITE SET PLOT FOR ISL71090SEH50 AT LET 56 V_{IN} = 30V, I_{OUT} = 20mA, C_{OUT} = 0.1µF, C_{COMP} = 10nF

The SET exhibited by the ISL71090SEH50 fall into two basic categories; fast negative spike and slow negative ramp and recovery similar to the 7.5V reference. The fast spikes can be as large as 800mV for LET 56 and V_{IN} = 30V. Under the same conditions the slow (20µs) negative ramp can reach 300mV. The disturbances can take significantly over 160µs to recover. Even at LET = 8.5MeV•cm^2/mg (Figures 23 and 24), there are SET of approximately 200mV.

More SET testing of the ISL71090SEH50 took place to look at the impact of higher C_{OUT} values. The summary of the testing done and the resulting oscilloscope captures is presented in Table 8.

Significant SET were captured on DUT1 (C_{OUT} = 1µF, C_{COMP} = 1nF). Figure 32 on page 14 displays a composite plot for LET = 28MeV•cm^2/mg and V_{IN} = 30V that range from -550mV to +70mV and a characteristic under damped response. The captures stopped at 150µs before the output had recovered fully. It is interesting that the initiating SET appears as a fast fall on the output, but the output follows a slow linear loop response recovery.

Figure 33 on page 14 shows that a change to C_{OUT} = 10µF and C_{COMP} = 10nF almost eliminate the SET resulting from LET = 28MeV•cm^2/mg at V_{IN} = 30V, the same conditions as in Figure 32. Comparison shows the significant reduction in the SET deviation although a long settling time is still evident.

Figure 34 on page 14 shows that leaving C_{OUT} at 1µF but increasing C_{COMP} to 10nF provides significant improvement over the case in Figure 32 (C_{OUT} = 1µF, C_{COMP} = 1nF) but not as much as with C_{OUT} = 10µF.

Finally, reducing the LET to 2.7MeV•cm^2/mg for DUT1 (C_{OUT} = 1µF, C_{COMP} = 1nF) provides moderate suppression of the SET magnitudes as shown in Figure 35 on page 14. The worst case SET deviations are only about 200mV or one third of those seen at LET 28 in Figure 32. Clearly the change in capacitance is much more effective at limiting the SET deviation than the reduction in LET.

TABLE 8. SUMMARY OF QUAD TESTING OF ISL71090SEH50 PARTS BOLD ENTRIES WITH SUPERSCRIPTS ARE SHOWN AS COMPOSITE PLOT FIGURES

RUN	LET (MeV•cm^2/mg)	IOUT (mA)	VIN (V)	SET COUNTS (±20mV), 4E+06 ION/cm^2			
				C_{OUT} = 1µF C_{COMP} = 1nF	C_{OUT} = 1µF C_{COMP} = 10nF	C_{OUT} = 10µF C_{COMP} = 10nF	
				DUT 1	DUT 2	DUT 3	DUT 4
301	28	-10	7	689	60	53	61
302			30	1022	85	84	34
303		20	7	707	218	121	45
304			30	**879**(Figure 32)	**224**(Figure 34)	**117**(Figure 33)	87
201	8.5	-10	7	203	30	2	0
202			30	237	18	2	0
203		20	7	195	43	2	1
204			30	247	59	45	35
101	2.7	-10	7	141	16	0	0
102			30	139	0	0	0
103		20	7	122	2	0	0
104			30	**129**(Figure 35)	9	0	3

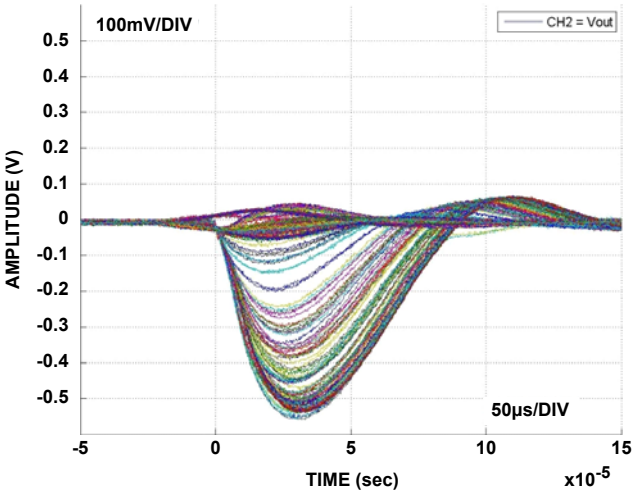

FIGURE 32. COMPOSITE SET PLOT FOR ISL71090SEH75 AT LET 28
V_{IN} = 30V, I_{OUT} = 20mA, C_{OUT} = 1µF, C_{COMP} = 1nF

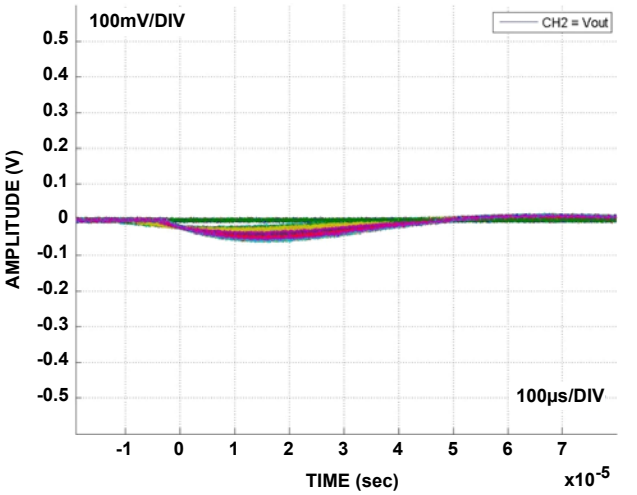

FIGURE 33. COMPOSITE SET PLOT FOR ISL71090SEH75 AT LET 28
V_{IN} = 30V, I_{OUT} = 20mA, C_{OUT} = 10µF, C_{COMP} = 10nF

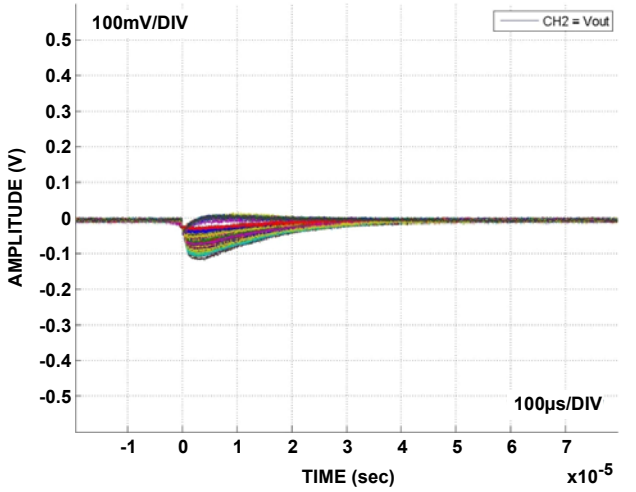

FIGURE 34. COMPOSITE SET PLOT FOR ISL71090SEH75 AT LET 28
V_{IN} = 30V, I_{OUT} = 20mA, C_{OUT} = 1µF, C_{COMP} = 10nF

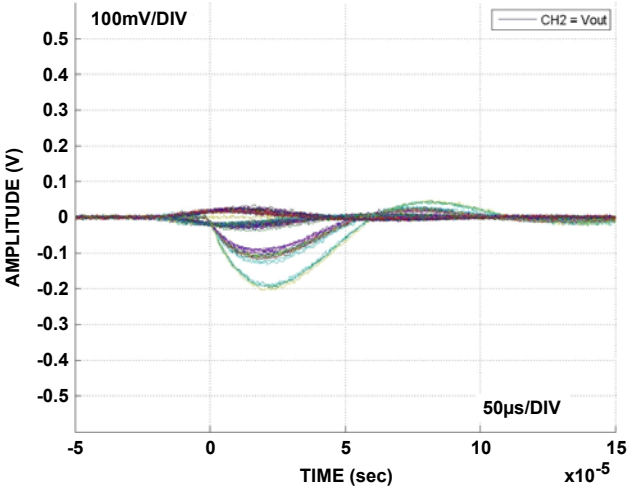

FIGURE 35. COMPOSITE SET PLOT FOR ISL71090SEH75 AT LET 2.7
V_{IN} = 30V, I_{OUT} = 20mA, C_{OUT} = 1µF, C_{COMP} = 1nF

Role of C_{OUT} in SET of ISL71090SEHxx

After running the various types with C_{OUT} = 0.1µF, it was decided to go back and look at the results with larger C_{OUT} to see if the SET magnitudes reduced. Toward that end, two parts of the ISL71090SEH25 were tested at LET 86 with C_{OUT} = 1.0µF and 10.0µF. Composite plots of the SET appear in Figures 36 and 37.

The reduction of I_{OUT} (20mA to 10mA) and the increase of C_{OUT} (0.1µF to 1µF) took the negative SET at LET 86 from over 325mV (Figure 11) down to roughly 108mV, but pushed the recovery time to beyond 50µs. The 10x increase in capacitance did not realize a 10x reduction in the SET, even with the 2x reduction in I_{OUT}. Only a reduction of SET by about 3x was achieved with both the reduction in I_{OUT} and the increase in C_{OUT}.

A further reduction in SET was sought with a further increase in C_{OUT} to 10µF. This was accompanied with an increase in the compensation capacitor from 1nF to 10nF. The resulting composite plot of SET is in Figures 36 and 37.

Increasing C_{OUT} to 10µF further reduced the negative SET at LET of 86 to about 30mV but also prolonged the recovery time. Clearly the size of C_{OUT} serves to mitigate the SET magnitudes, but not in proportion to capacitance value. The 10x increase from 1µF to 10µF only reduced the SET by about 3x (for the same I_{OUT}). To be sure, the smallest SET was found to be with the largest C_{OUT}, but the capacitance benefit was about equal to the square root of the capacitance ratio; a 10x reduction in SET was realized in going from 0.1µF to 10µF.

Later tests on the 5.0V and 7.5V versions of the references demonstrated clear SET suppression at lower LET (28, 8.5 and 2.7MeV•cm^2/mg) with the larger capacitance values. Even in this most favorable of conditions, a very few SET of 20mV were noted for LET of 2.7MeV•cm^2/mg.

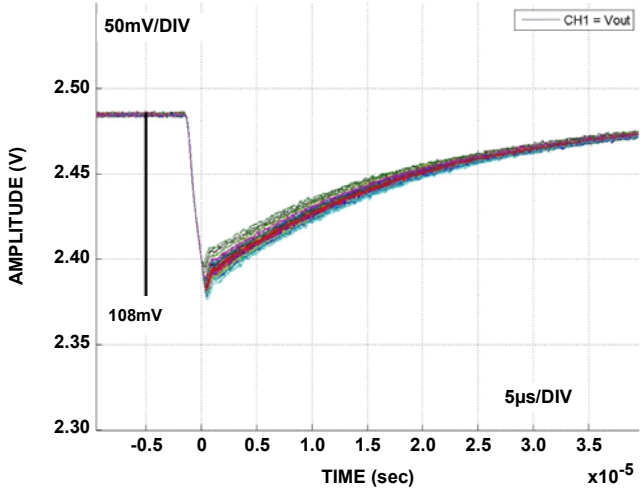

FIGURE 36. COMPOSITE SET PLOT FOR ISL71090SEH25 AT LET 86, V_{IN} = 4V, I_{OUT} = 10mA, C_{OUT} = 1µF, C_{COMP} = 1nF

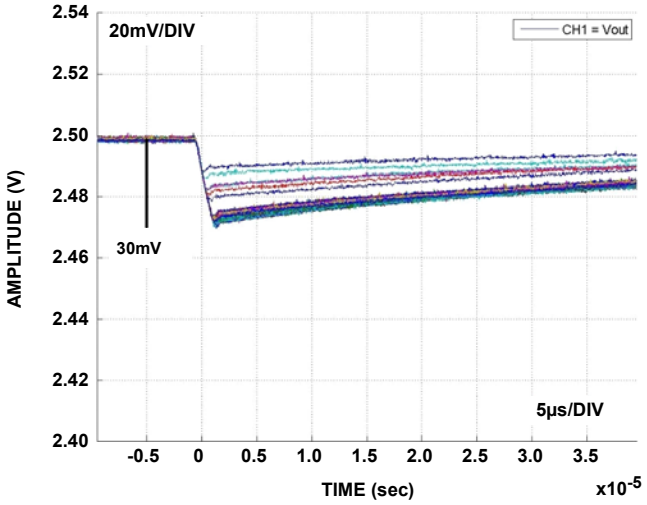

FIGURE 37. COMPOSITE SET PLOT FOR ISL71090SEH25 AT LET 86, V_{IN} = 4V, I_{OUT} = 20mA, C_{OUT} = 10µF, C_{COMP} = 10nF

Conclusion

SEE testing of the ISL71090SEH precision reference product family has demonstrated that the devices are not susceptible to single event damage (SEB) at an LET of 86.3MeV•cm^2/mg with an input voltage of 37V and a load current of 20mA. This represents conditions that are over 20% above the recommended input voltage of 30V and 100% of the load regulation drive capability of the IC (20mA).

SET testing demonstrated that all transients can be confined to be predominately negative if C_{COMP} is selected to be large (10nF). This was demonstrated in the testing of the 7.5V version with C_{COMP} both 1nF (Figures 16 and 17) and 10nF (Figures 18 and 19). In addition, a larger C_{OUT} (10µF) suppresses SET magnitude (Figures 32 and 33). In both cases the extra capacitance limits the SET magnitude, but the SET disturbance duration is stretched out, so capacitor selection represents a compromise between SET magnitude and duration. For maximum SET magnitude suppression the capacitors should be C_{OUT} = 10µF and C_{COMP} = 10nF. It should be noted that even at LET = 2.7MeV•cm^2/mg the 2.5V part showed a nominal cross section of 1.2E-05 cm^2 for SET more than 20mV. At LET = 2.7MeV•cm^2/mg the 5.0V part showed a nominally larger cross section of 3.2xE-05 cm^2 for SET more than 20mV. This is to be expected as the 20mV criteria is a smaller fractional perturbation on the higher nominal output. It should also be noted that SET magnitude scales with the output voltage, so that the 7.5V reference exhibits the largest SET.

Based on this testing, the selection of C_{OUT} = 10µF and C_{COMP} = 10nF seems best from an SET suppression perspective. However, this has bandwidth implications and does not eliminate all SET even at low LET (less than or equal to 2.7MeV•cm^2/mg). The user is encouraged to carefully consider the selection and implications of the capacitance values.

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