ISL70321SEH

Neutron Testing of the ISL70321SEH Radiation Hardened Quad Power Supply Sequencer

This report summarizes results of 1MeV equivalent neutron testing of the ISL70321SEH radiation tolerant quad power supply sequencer. The test was conducted to determine the sensitivity of the part to displacement damage (DD) caused by neutron or proton environments. Neutron fluences ranged from 5×10^{11}n/cm^2 to 1×10^{13}n/cm^2.

Product Description

The ISL70321SEH is a radiation tolerant and SEE mitigated power supply sequencer designed to control Point-of-Load (POL) regulators with enable pins. Up to four power supplies can be sequenced by a single device or multiple devices can be easily cascaded to sequence an unlimited number of power supplies for dense RF applications in EW, radar and SIGINT platforms. The sequencer requires only two feedback resistors per power supply and a single resistor to set the rising and falling delay. The device features precision input comparators with an input threshold voltage of 600mV ±1.5% for the highest possible accuracy when monitoring the power supply voltages.

The ISL70321SEH is offered in an 18 lead 10mm×12mm CDFP package or in die form and is fully specified across the military ambient temperature range of -55°C to +125°C. With minimal external component count, precision voltage monitoring and SET mitigation, the ISL70321SEH is the ideal choice to control many of today's spaceborne power systems.

A typical application schematic for the ISL70321SEH is shown in Figure 1.

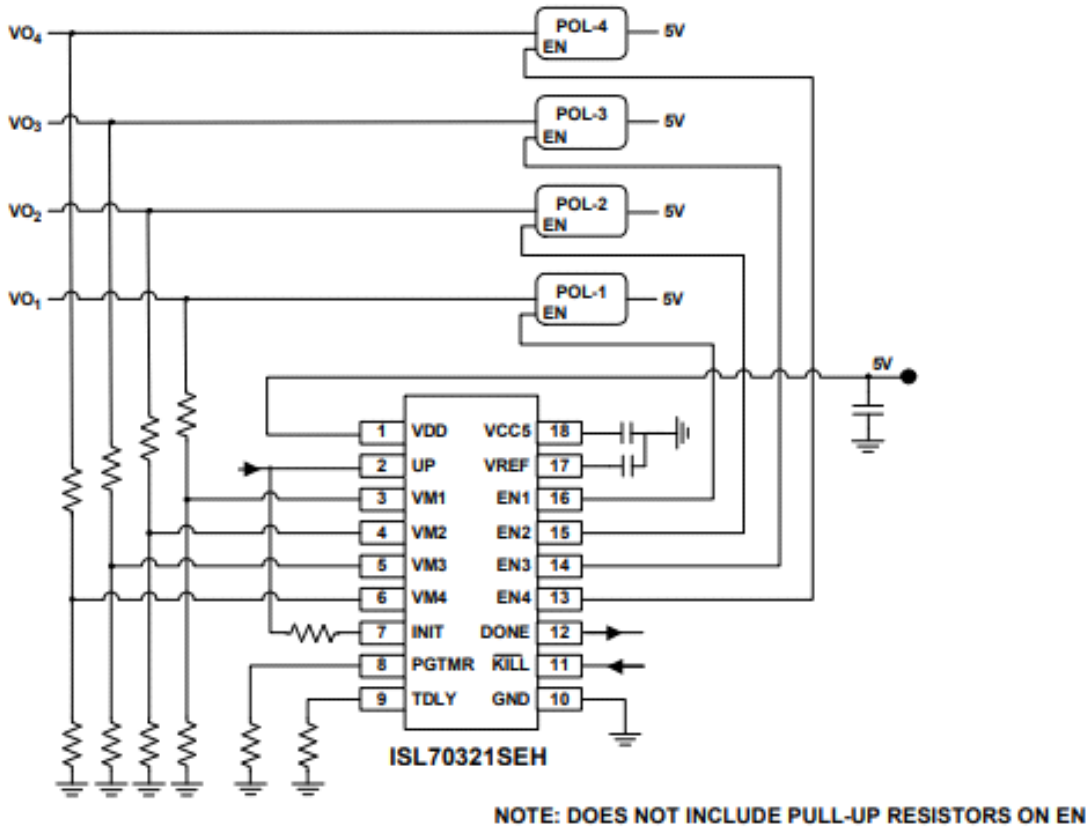

Figure 1. ISL70321SEH Typical Application Schematic

Contents

1. Test Description

1.1 Irradiation Facility

Neutron fluence irradiations were performed on the test samples on August 31, 2021, at the University of Massachusetts, Lowell (UMASS Lowell) fast neutron irradiator per Mil-STD-883G, Method 1017.2, with each part unpowered during irradiation. The target irradiation levels were 5×10^{11}n/cm^2, 2×10^{12}n/cm^2, and 1×10^{13}n/cm^2. As neutron irradiation activates many of the heavier elements found in a packaged integrated circuit, the parts exposed at the higher neutron levels required (as expected) some cooldown time before being shipped back to Renesas (Palm Bay, FL) for electrical testing.

1.2 Test Fixturing

No formal irradiation test fixturing is involved, as these DD tests are bag tests in the sense that the parts are irradiated with all leads unbiased.

1.3 Radiation Dosimetry

Table 1 shows dosimetry from UMASS Lowell indicating the total accumulated gamma dose and actual neutron fluence exposure levels for each set of samples.

Table 1. ISL70321SEH Neutron Fluence Dosimetry Data

Irradiation	Requested Fluence (n/cm^2)	Reactor Power (kW)	Time (s)	Fluence Rate (n/cm^2-s)[1] [2]	Gamma Dose (rad(Si))[3]	Measured Fluence (n/cm^2)[4]
CRF#62106-A	5.00E+11	10	617	8.10E+08	70	5.38E+11
CRF#62106-B	2.00E+12	100	247	8.10E+09	281	2.05E+12
CRF#62106-C	1.00E+13	1000	123	8.10E+10	1401	1.14E+13

1. Dosimetry method: ASTM E-265
2. The neutron fluence rate is determined from *Initial Testing of the New Ex-Core Fast Neutron Irradiator at UMass Lowell* (6/18/02). Validated on 6/07/2011 under the Trident II D5LE neutron facility study by Navy Crane.
3. Based on reactor power at 1000kW, the gamma dose is 41±5.3% krad(Si)/hr as mapped by TLD-based dosimetry.
4. Validated by S-32 flux monitors.

1.4 Characterization Equipment and Procedures

Electrical testing was performed before and after irradiation using the Renesas production automated test equipment (ATE). All electrical testing was performed at room temperature.

1.5 Experimental Matrix

Testing proceeded in general accordance with the guidelines of MIL-STD-883 TM 1017. The experimental matrix consisted of five samples to be irradiated at 5×10^{11}n/cm^2, five to be irradiated at 2×10^{12}n/cm^2, and five to be irradiated at 1×10^{13}n/cm^2. The actual levels achieved, which are shown in Table 2, were 5.38×10^{11}n/cm^2, 2.05×10^{12}n/cm^2, and 1.14×10^{13}n/cm^2. Three control units were used.

The 15 ISL70321SEH samples were drawn from Lot 5STWBEH. Samples were packaged in the standard hermetic 18 lead ceramic (CDFP) production package. Samples were processed through burn-in before irradiation and were screened to the SMD limits at room, low, and high temperatures before the start of neutron testing.

2. Results

Neutron testing of the ISL70321SEH is complete and the results are reported in the balance of this report. It should be understood when interpreting the data that each neutron irradiation was performed on a different set of samples; this is not total dose testing, where the damage is cumulative.

2.1 Attributes Data

Table 2. ISL70321SEH Attributes Data

1 MeV Fluence, (n/cm^2)		Sample Size	Pass[1]	Fail	Notes
Planned	Actual				
5×10^{11}	5.38×10^{11}	5	5	0	All passed
2×10^{12}	2.05×10^{12}	5	5	0	All passed
1×10^{13}	1.14×10^{13}	5	5	0	All passed

1. A Pass indicates a sample that passes all SMD limits

2.2 Variables Data

The plots in Figure 2 through Figure 22 show data plots for key parameters before and after irradiation to each level. The plots show the mean of each parameter as a function of neutron irradiation. The plots also include error bars at each downpoint, representing the minimum and maximum measured values of the samples, although in some plots the error bars might not be visible because of their values compared to the scale of the graph. While the applicable electrical limits taken from the SMD are also shown, it should be noted that these limits are provided for guidance only as the ISL70321SEH is not specified for the neutron environment.

All samples passed the post-irradiation SMD limits after all three exposures up to and including 1.14×10^{13}n/cm^2.

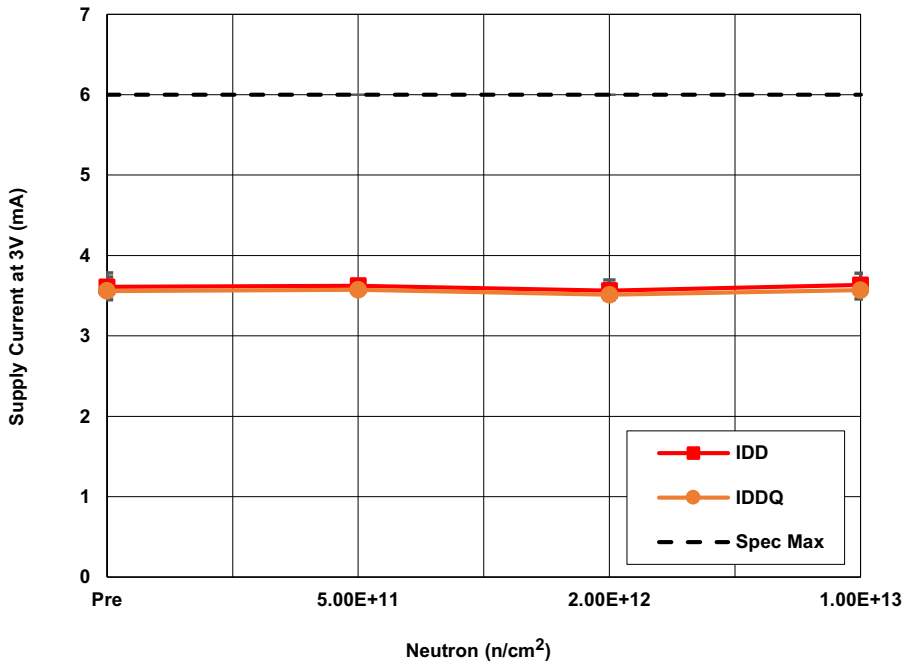

Figure 2. ISL70321SEH quiescent (I_{DDQ}) and operating (I_{DD}) supply current at V_{DD} = 3V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 6mA maximum.

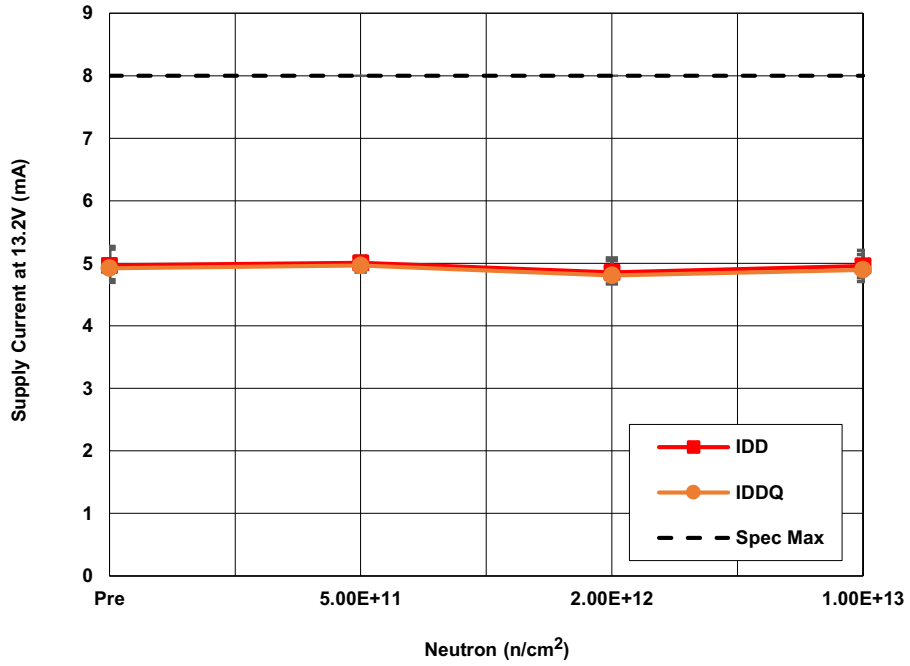

Figure 3. ISL70321SEH quiescent (I_{DDQ}) and operating (I_{DD}) supply current at V_{DD} = 13.2V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 8mA maximum.

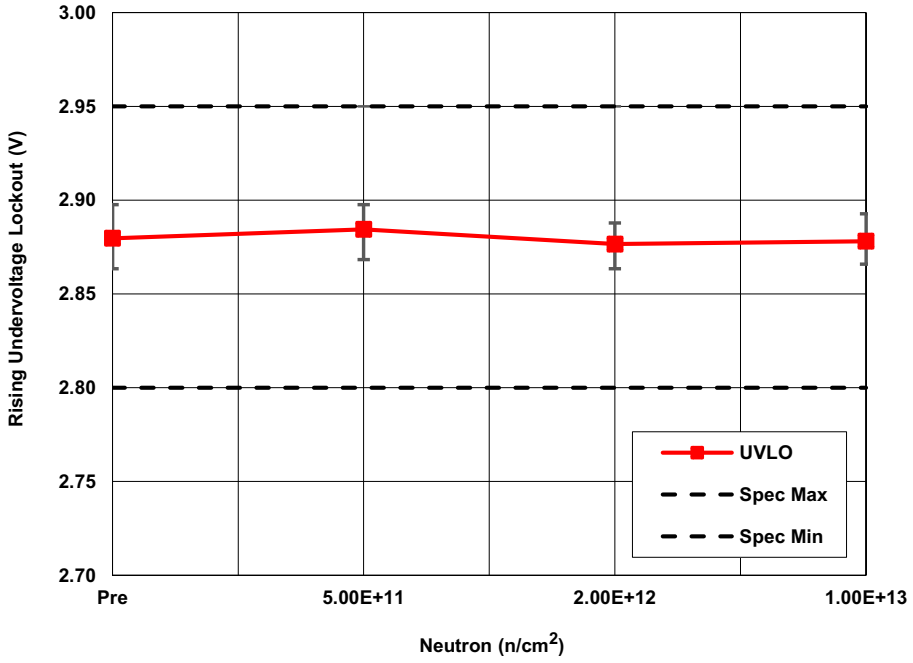

Figure 4. ISL70321SEH rising undervoltage lockout (UVLO) voltage following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 2.80V minimum and 2.95V maximum.

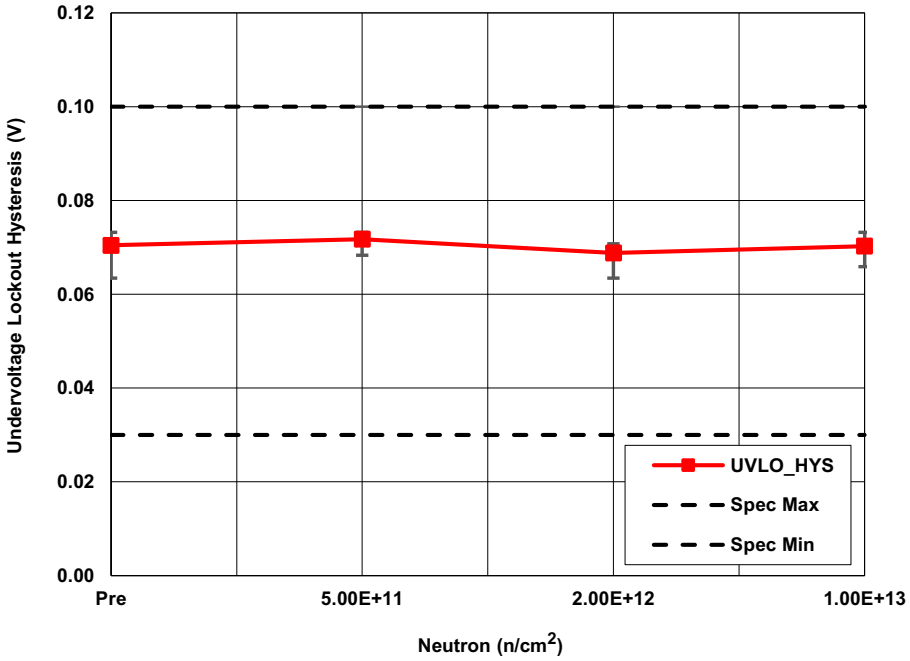

Figure 5. ISL70321SEH undervoltage lockout hysteresis (UVLO_HYS) voltage following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 0.03V minimum and 0.1V maximum.

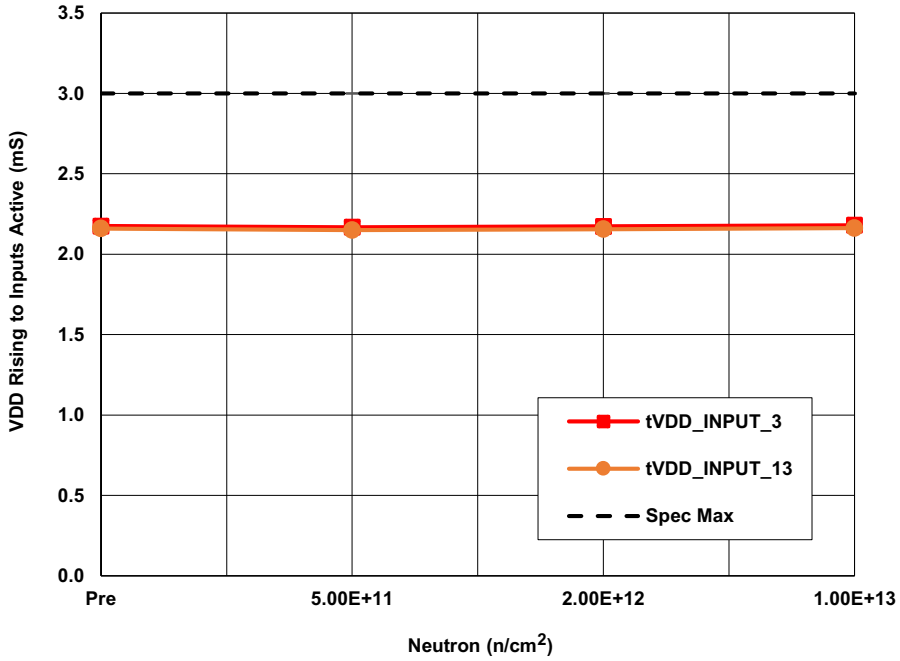

Figure 6. ISL70321SEH time from V_{DD} rising to inputs active (t_{VDD_INPUT}) at V_{DD} = 3V and 13.2V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 3ms maximum.

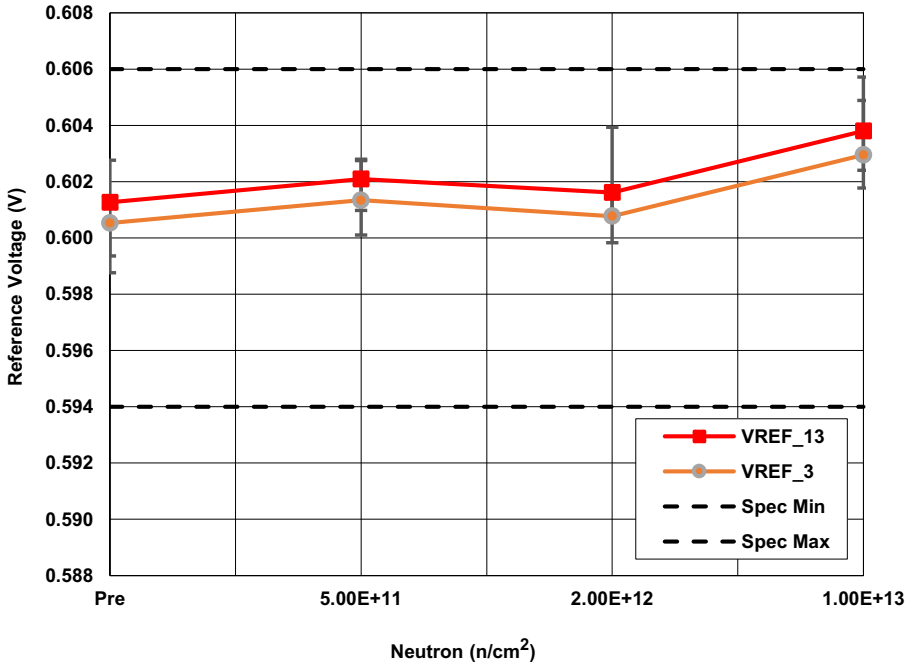

Figure 7. ISL70321SEH reference voltage (V_{REF}) at V_{DD} = 3V and 13.2V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 0.594V minimum and 0.606V maximum.

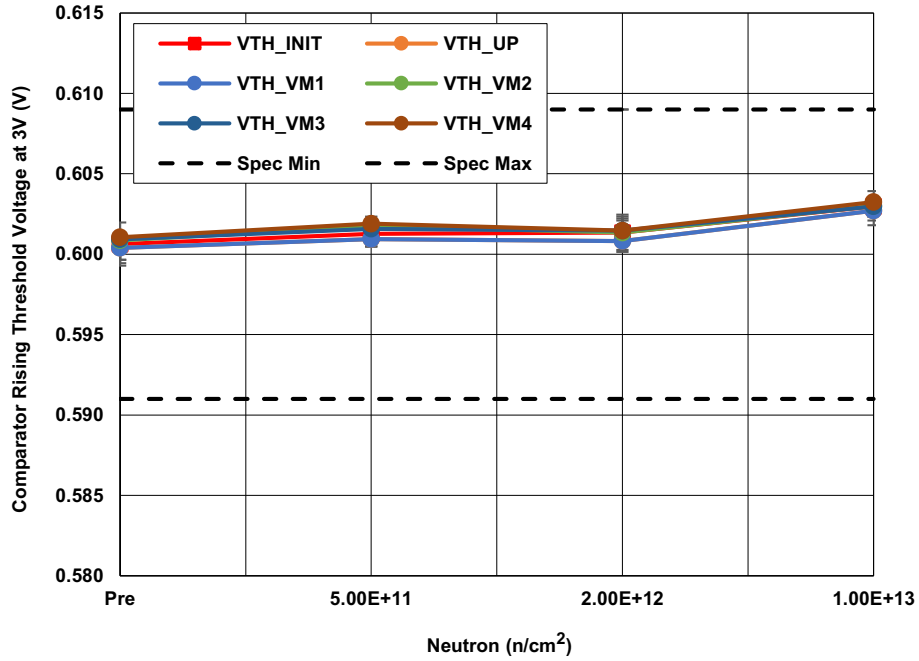

Figure 8. ISL70321SEH comparator rising threshold voltage (V_{TH}) at V_{DD} = 3V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 0.591V minimum and 0.609V maximum.

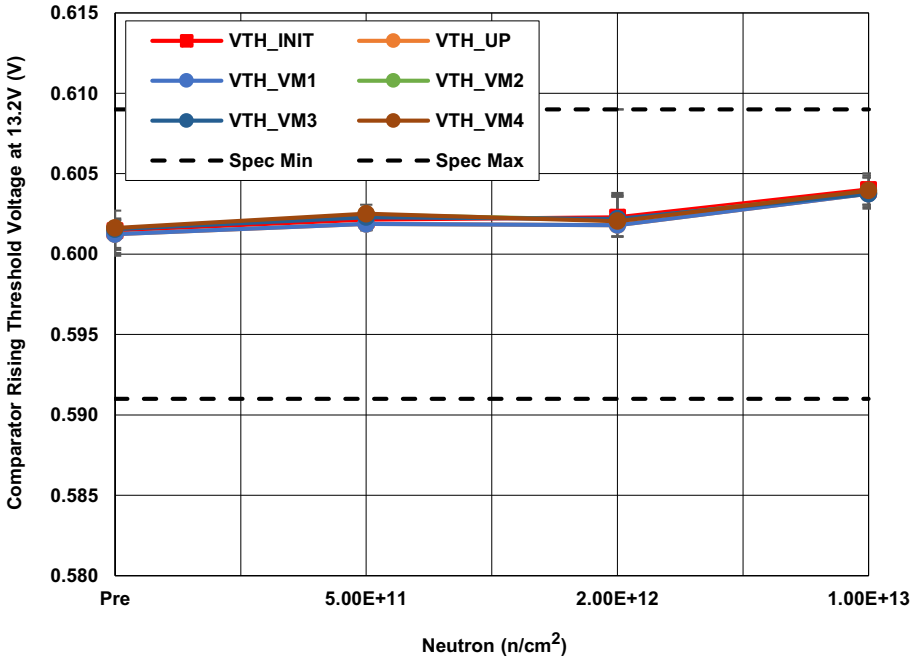

Figure 9. ISL70321SEH comparator rising threshold voltage (V_{TH}) at V_{DD} = 13.2V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 0.591V minimum and 0.609V maximum.

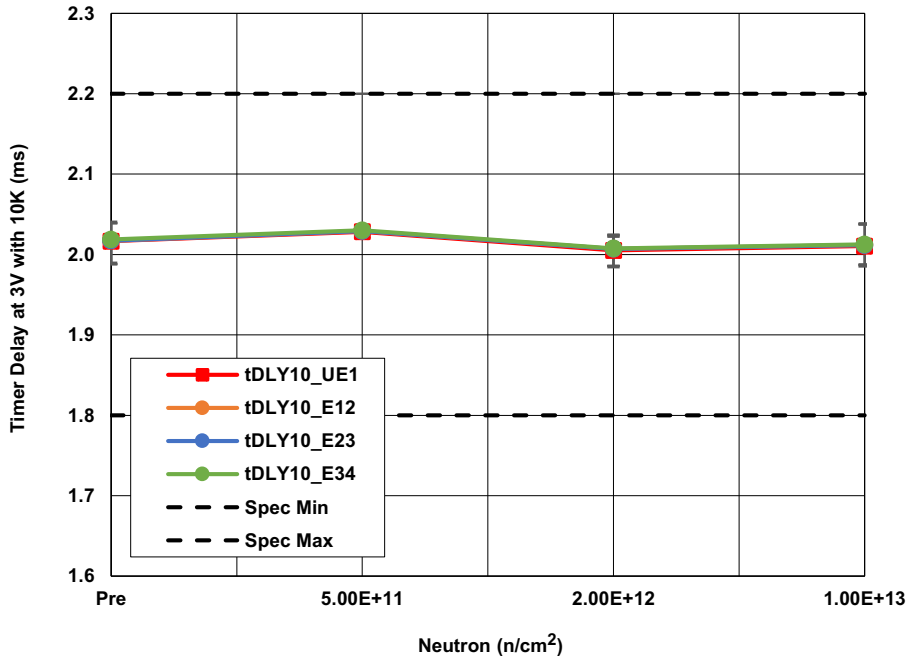

Figure 10. ISL70321SEH timer delay with 10KΩ resistor (t_{DLY_10}) at V_{DD} = 3V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 1.8ms minimum and 2.2ms maximum.

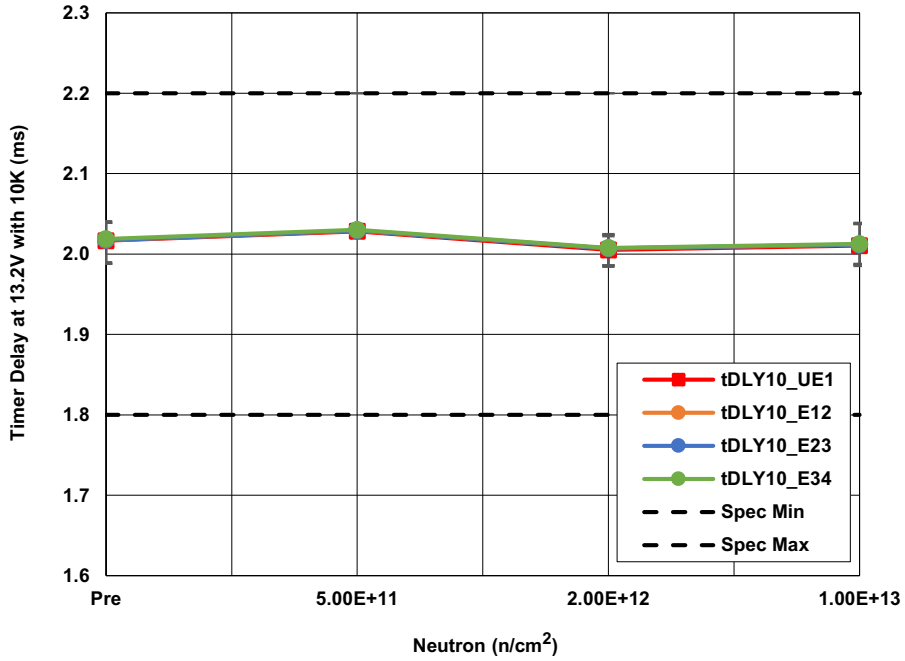

Figure 11. ISL70321SEH timer delay with 10kΩ resistor (t_{DLY_10}) at V_{DD} = 13.2V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 1.8ms minimum and 2.2ms maximum.

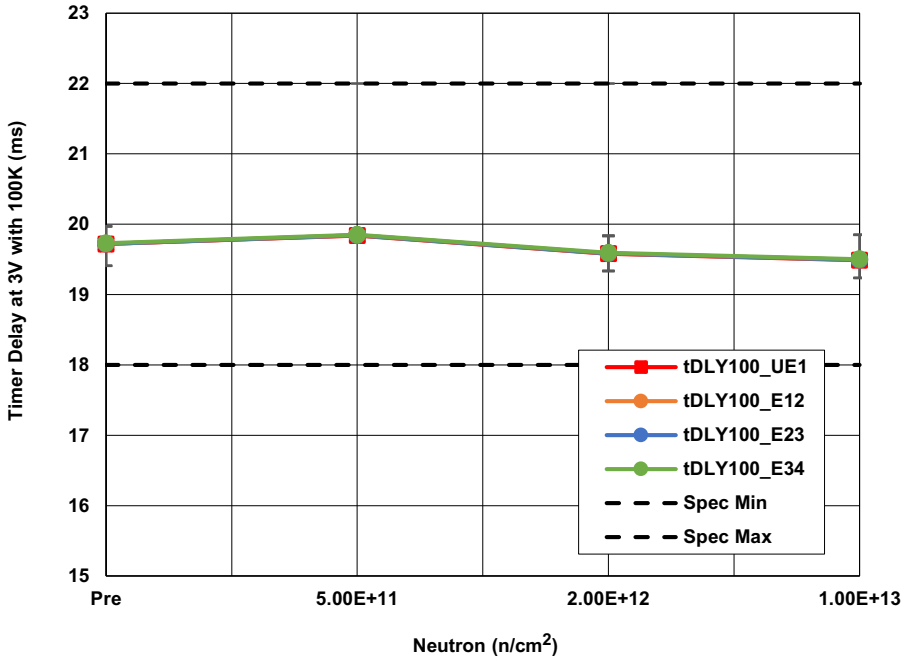

Figure 12. ISL70321SEH timer delay with 100kΩ resistor (t_{DLY_100}) at V_{DD} = 3V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 18ms minimum and 22ms maximum.

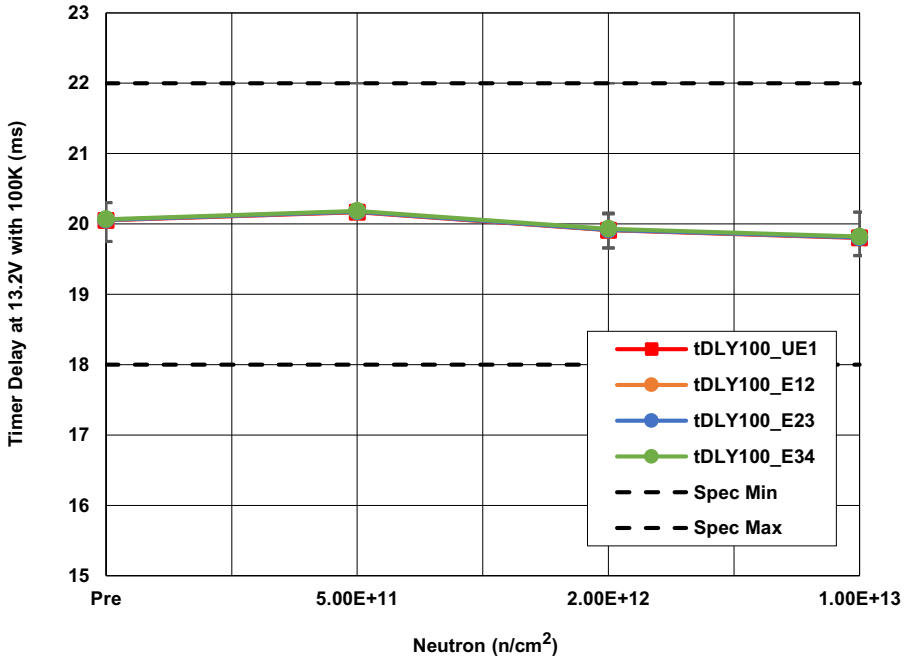

Figure 13. ISL70321SEH timer delay with 100kΩ resistor (t_{DLY_100}) at V_{DD} = 13.2V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 18ms minimum and 22ms maximum.

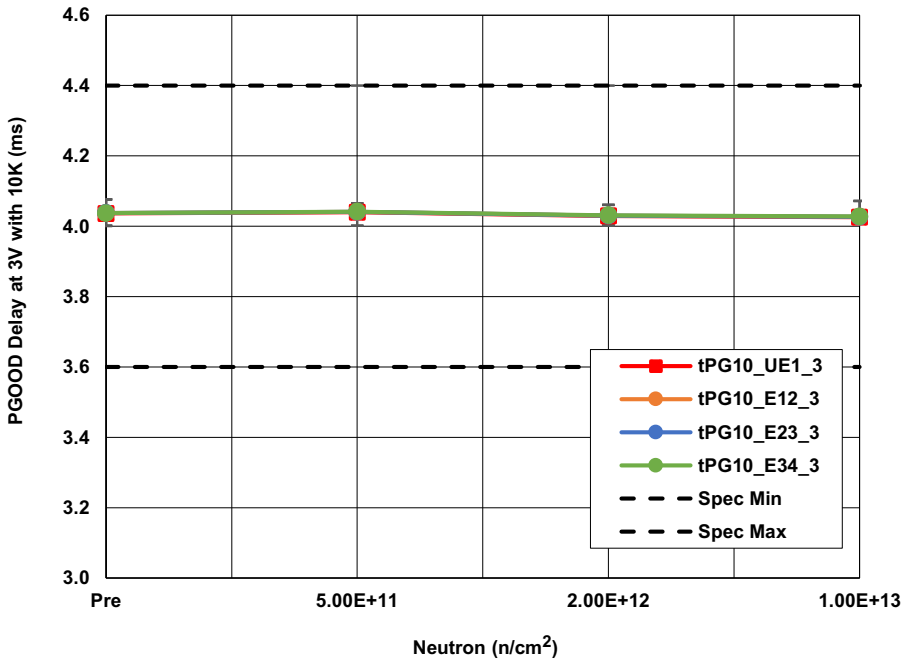

Figure 14. ISL70321SEH power-good delay with 10kΩ resistor (t_{PG_10}) at V_{DD} = 3V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 3.6ms minimum and 4.4ms maximum.

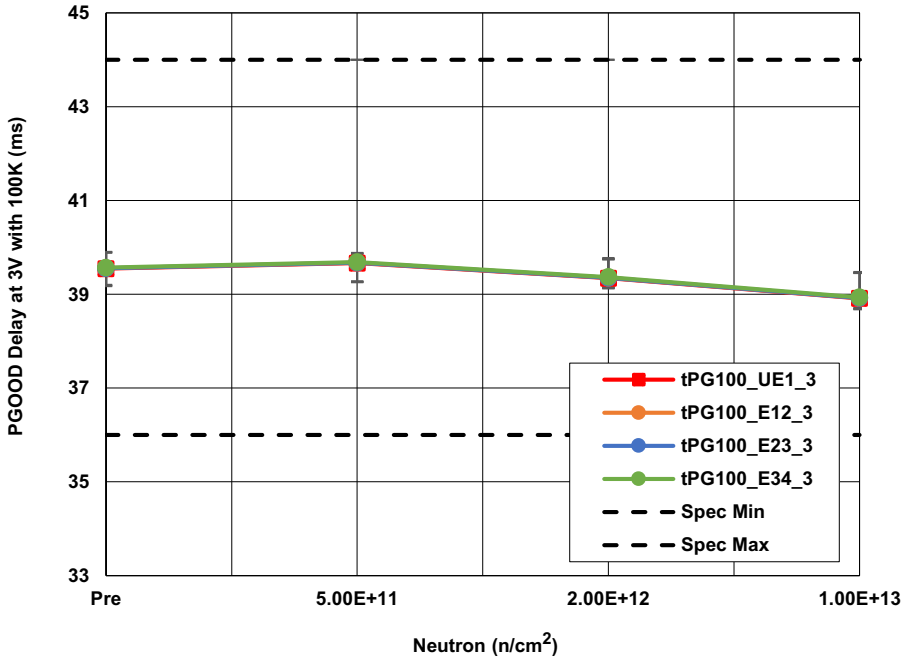

Figure 15. ISL70321SEH power-good delay with 10kΩ resistor (t_{PG_10}) at V_{DD} = 13.2V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 3.6ms minimum and 4.4ms maximum.

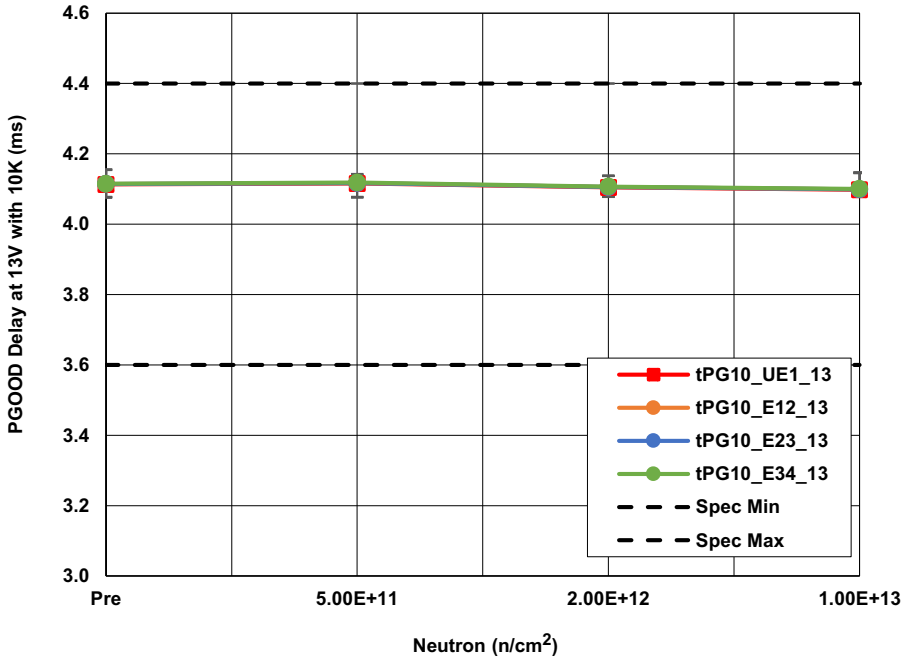

Figure 16. ISL70321SEH power-good delay with 100kΩ resistor (t_{PG_100}) at V_{DD} = 3V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 36ms minimum and 44ms maximum.

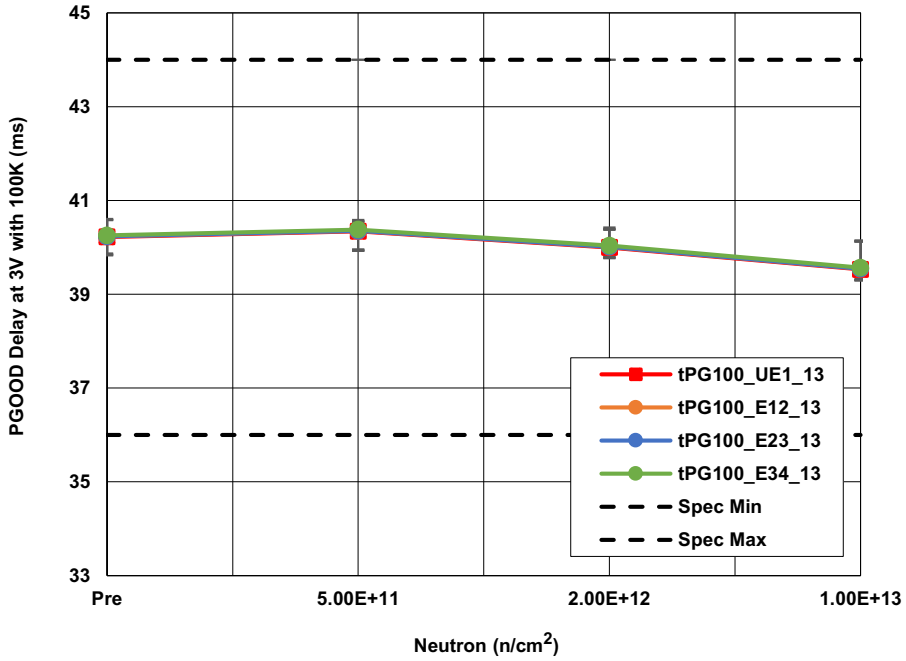

Figure 17. ISL70321SEH power-good delay with 100kΩ resistor (t_{PG_100}) at V_{DD} = 13.2V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limits are 36ms minimum and 44ms maximum.

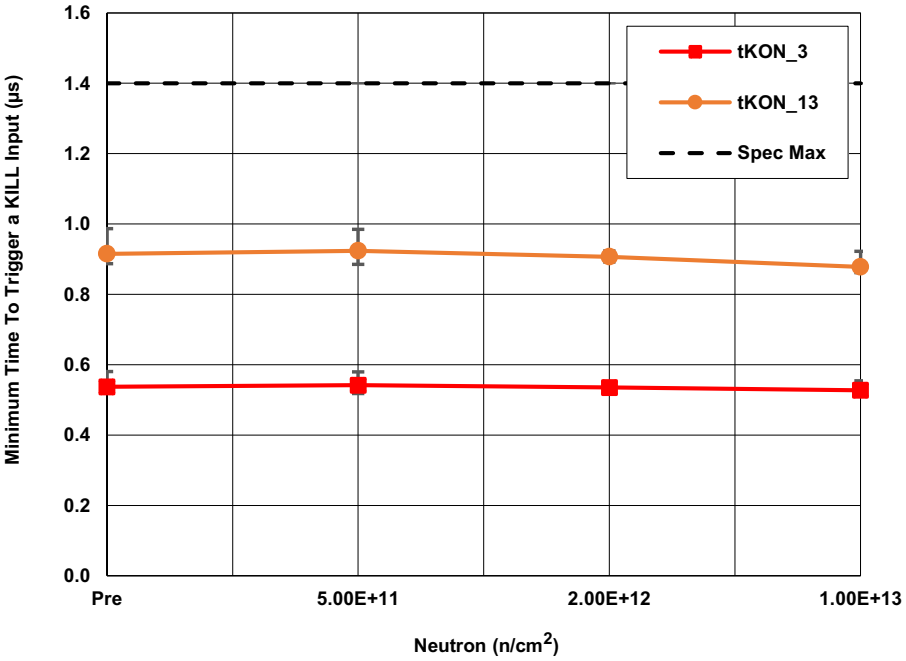

Figure 18. ISL70321SEH minimum time to trigger a KILL input (t_{KON}) at V_{DD} = 3V and 13.2V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 1.4µs maximum.

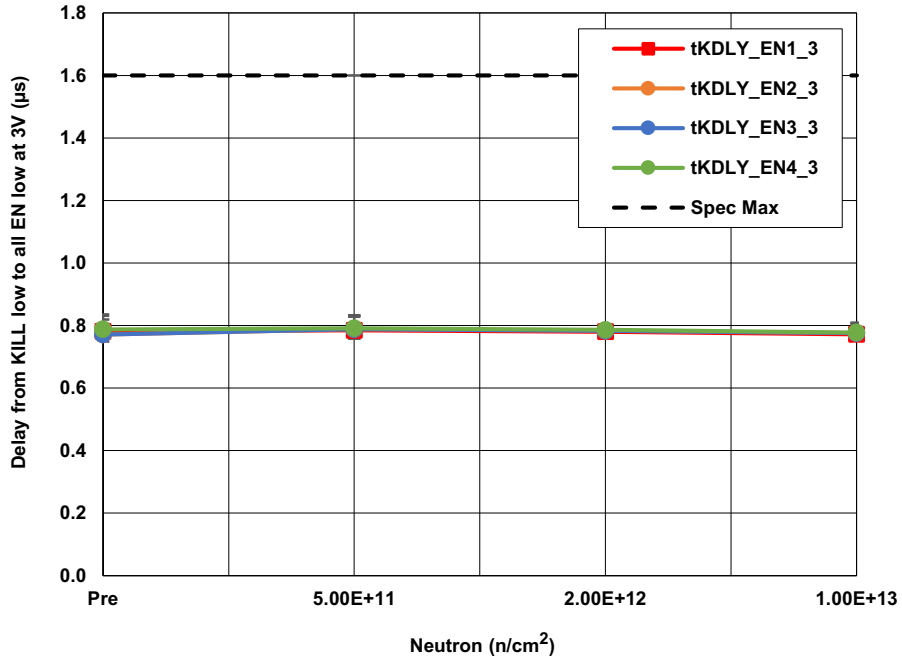

Figure 19. ISL70321SEH delay from KILL low to EN1 - EN4 Low (t_{KDLY}) at V_{DD} = 3V irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 1.6µs maximum.

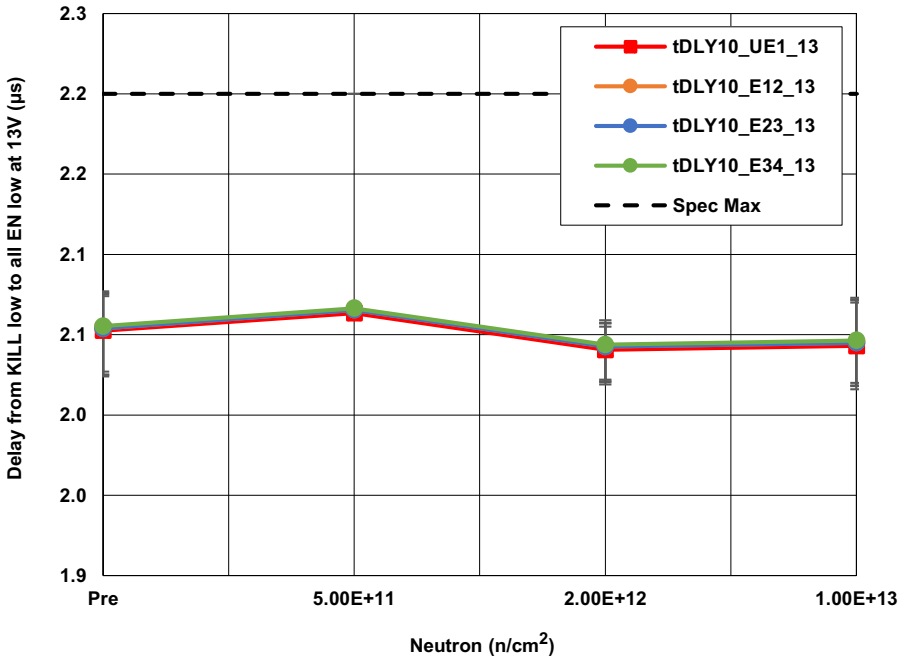

Figure 20. ISL70321SEH delay from KILL low to EN1 - EN4 Low (t_{KDLY}) at V_{DD} = 13.2V irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 2.2µs maximum.

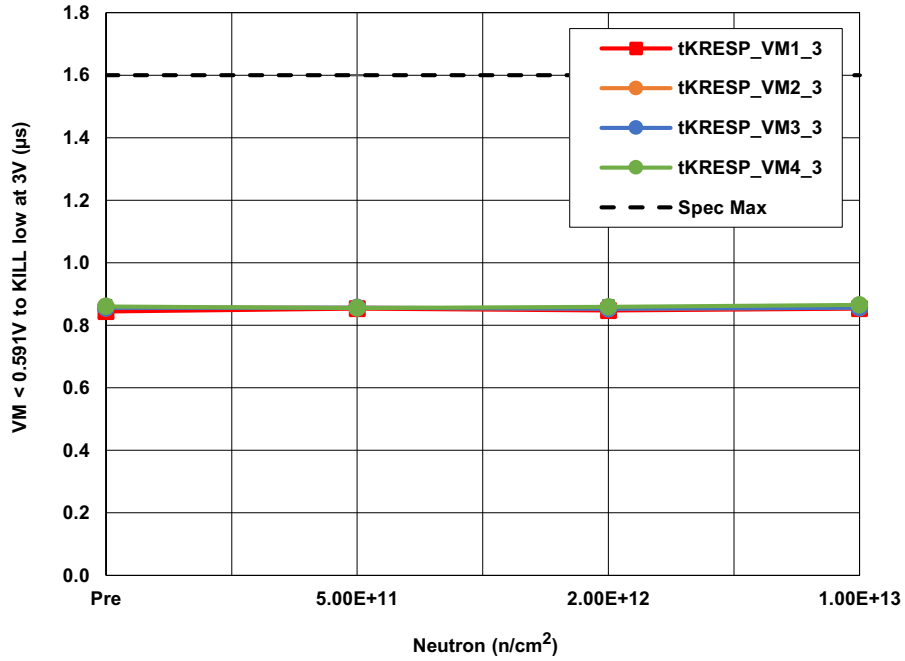

Figure 21. ISL70321SEH delay from VM < 0.591V to KILL Low (t_{KRESP}) at V_{DD} = 3V irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 1.6µs maximum.

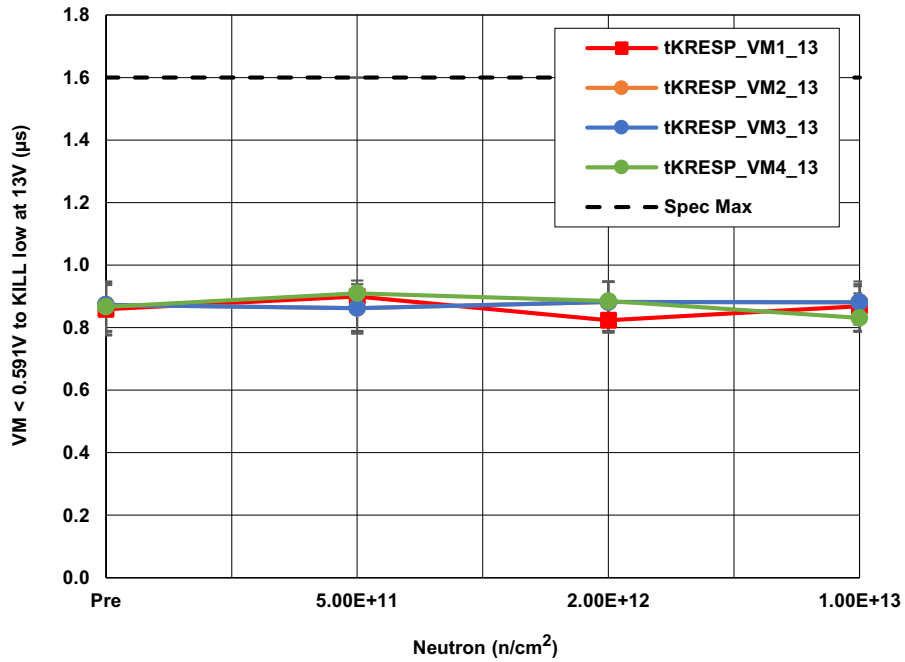

Figure 22. ISL70321SEH delay from VM < 0.591V to KILL Low (t_{KRESP}) at V_{DD} = 13.2V irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The SMD limit is 1.6µs maximum.

3. Discussion and conclusion

This document reports the results of 1MeV equivalent neutron testing of the ISL70321SEH radiation hardened the ISL70321SEH radiation tolerant quad power supply sequencer. Parts were tested at actual fluences of $5.4\times10^{11}n/cm^2$, $2.1\times10^{12}n/cm^2$ and $1.1\times10^{13}n/cm^2$. The results of key parameters before and after irradiation to each level are plotted in Figure 2 through Figure 22. The plots show the mean of each parameter as a function of neutron irradiation, with error bars that represent the minimum and maximum measured values. The figures also show the applicable electrical limits taken from the SMD, but it should be noted that these limits are provided for guidance only as the ISL70321SEH is not specified for the neutron environment.

All samples passed the post-irradiation SMD limits after all exposures up to and including $1.1\times10^{13}n/cm^2$.

4. Revision History

Revision	Date	Description
1.00	Mar 23, 2022	Initial release.

Appendix

Table 3. Reported Parameters

Fig.	Parameter	Symbol	Test Conditions	Low Limit	High Limit	Units
2	3V Quiescent Supply Current	IDDQ_3	UP and INIT = 0.5V	-	6	mA
	3V Operating Supply Current	IDD_3	UP and INIT = 0.7V with EN tied to VM to 5V			
3	13.2V Quiescent Supply Current	IDDQ_13	UP and INIT = 0.5V	-	8	mA
	13.2V Operating Supply Current	IDD_13	UP and INIT = 0.7V with EN tied to VM to 5V			
4	Rising Undervoltage Lockout Level	UVLO	V_{DD} rising to V_{REF} rising, VCC5 = 45mA	2.8	2.95	V
5	Undervoltage Lockout Hysteresis	UVLO_hys	UVLO - V_{DD} falling to V_{REF} turn-off	0.03	0.1	V
6	Time from V_{DD} to Inputs being Active	t_{VDD_INPUT}	V_{DD} rising to inputs active, t_{DLY} timer disabled	-	3	ms
7	Reference Voltage	V_{REF}		0.594	0.606	V
8	Comparator rising threshold voltage at 3V	V_{TH}	V_{DD} = 3V	0.591	0.609	V
9	Comparator rising threshold voltage at 13.2V	V_{TH}	V_{DD} = 13.2V	0.591	0.609	V
10	10kΩ Delay Timer	t_{DLY_10}	RSET = 10k, V_{DD} = 3V	1.8	2.2	ms
11	10kΩ Delay Timer	t_{DLY_10}	RSET = 10k, V_{DD} = 13.2V	1.8	2.2	ms
12	100kΩ Delay Timer	t_{DLY_100}	RSET = 100k, V_{DD} = 3V	18	22	ms
13	100kΩ Delay Timer	t_{DLY_100}	RSET = 100k, V_{DD} = 13.2V	18	22	ms
14	10kΩ Power-Good Timer	t_{PG_10}	RSET = 10k, V_{DD} = 3V	3.6	4.4	ms
15	10kΩ Power-Good Timer	t_{PG_10}	RSET = 10k, V_{DD} = 13.2V	3.6	4.4	ms
16	100kΩ Power-Good Timer	t_{PG_100}	RSET = 100k, V_{DD} = 3V	36	44	ms
17	100kΩ Power-Good Timer	t_{PG_100}	RSET = 100k, V_{DD} = 13.2V	36	44	ms
18	Minimum Time to Trigger a KILL Input	t_{KON}	V_{DD} = 3V and 13.2V	-	1.4	µs
19	Delay from KILL low to EN1 - EN4 Low	t_{KDLY}	V_{DD} = 3V	-	1.6	µs
20	Delay from KILL low to EN1 - EN4 Low	t_{KDLY}	V_{DD} = 13.2V	-	1.6	µs
21	VM < 0.591V to KILL Low	t_{KRESP}	V_{DD} = 3V	-	1.6	µs
22	VM < 0.591V to KILL Low	t_{KRESP}	V_{DD} = 13.2V	-	1.6	µs

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