# ISL70002SEH

Total Dose Testing

TR047
Rev.1.00
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## Introduction

This report provides the final results of a low and high dose rate total dose test of the ISL70002SEH point-of-load regulator. The test was conducted to determine the sensitivity of the part to the total dose environment and to determine if the part is low dose rate sensitive. This report summarizes 150krad(Si) and subsequent anneal results for the high and low dose rate tests.

## Product Description

The ISL70002SEH is a total dose and SEE hardened, high efficiency, monolithic, synchronous buck regulator with integrated MOSFETs. This single chip power solution operates across an input voltage range of 3V to 5.5V and provides a tightly regulated output voltage that is externally adjustable from 0.8V to ~85% of the input voltage. Output load current capacity is 12A for $T_J \leq +150ºC$. Two ISL70002SEH devices configured to current share can provide 19A total output current, assuming ±27% worst-case current share accuracy.

The ISL70002SEH uses peak current-mode control with integrated error amp compensation and pin selectable slope compensation. Switching frequency is also pin selectable to either 1MHz or 500kHz. Two devices can be synchronized 180º out of phase to reduce input RMS ripple current.

A high level of integration makes the ISL70002SEH an ideal choice to power small form factor applications. Two devices can be synchronized to provide a complete power solution for large scale digital ICs, like field programmable gate arrays (FPGAs) that require separate core and I/O voltages.

The ISL70002SEH is hardened to achieve a Total Ionizing Dose (TID) rating of 100krad(Si) at both high (50-300rad(Si)/s) and low (<0.01rad(Si)/s) dose rate as specified in MIL-STD-883 Test Method 1019. The part is acceptance tested on a wafer by wafer basis at low dose rate to 50krad(Si) and at high dose rate to 100krad(Si). The ISL70002SEH is also SEE hardened to an LET of 86.4MeV•$cm^2$/mg. The part is implemented in a submicron BiCMOS process optimized for power management applications. The process is in volume production under MIL-PRF-38535 certification and is used for a wide range of commercial power management devices. The block diagram for the ISL70002SEH is shown in Figure 1.

Specifications for radiation hardened QML devices are controlled by the Defense Logistics Agency (DLA) in Columbus, OH. The DSCC Standard Microcircuit Drawing (SMD) 5962-12202 is the controlling document and must be cited when ordering.

## Related Literature

- For a full list of related documents, visit our website
  - ISL70002SEH product page

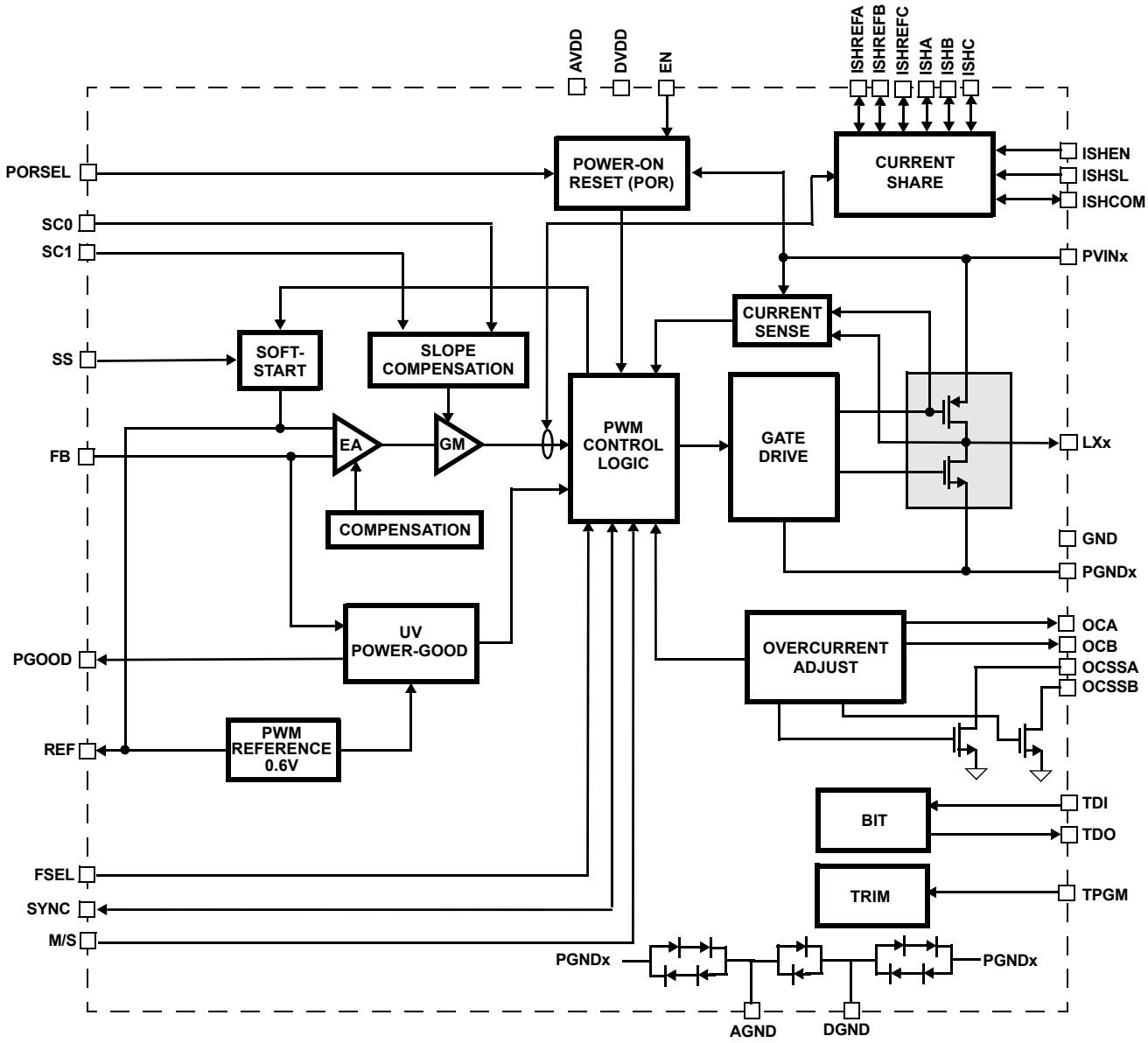
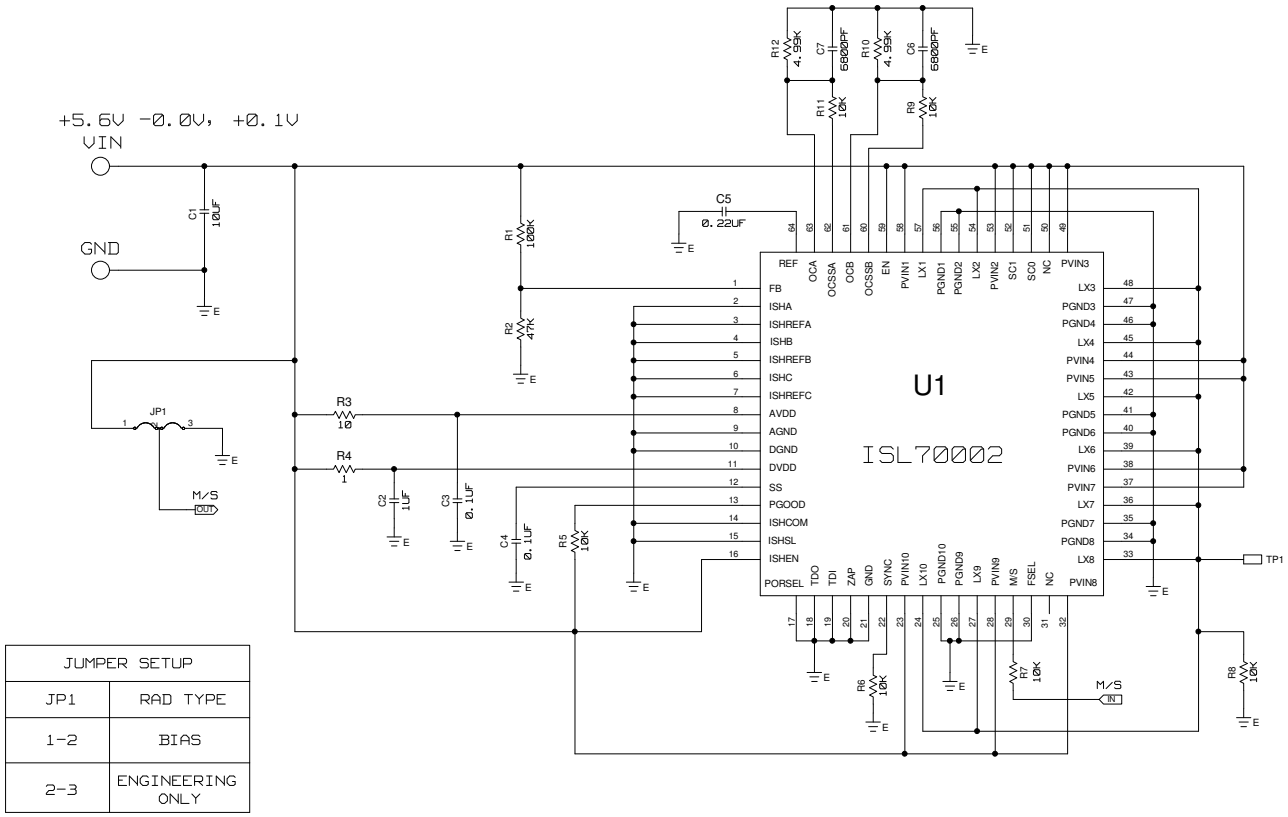



**Figure 1. ISL70002SEH Block Diagram**




| JUMPER SETUP | |
|---|---|
| JP1 | RAD TYPE |
| 1-2 | BIAS |
| 2-3 | ENGINEERING ONLY |

**Figure 2. Irradiation Bias Configuration for the ISL70002SEH, per SMD 5962-12202**

# 1. Test Description

## 1.1 Irradiation Facilities

High dose rate testing was performed using a Gammacell 220 $^{60}$Co irradiator located in the Palm Bay, Florida Intersil facility. Low dose rate testing used a Hopewell Designs N40 vault-type low dose rate irradiator located in the same facility. The high dose rate irradiations were done at 82.1rad(Si)/s and the low dose rate work was performed at 0.010rad(Si)/s, both per MIL-STD-883 Method 1019.7. A PbAl box was used to shield the test fixture and devices under test against low energy, secondary gamma radiation. Post-irradiation anneals were performed under bias in a small temperature chamber.

## 1.2 Test Fixturing

Figure 2 shows the configurations used for biased low and high dose rate testing and for the subsequent biased anneals.

## 1.3 Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using the production Automated Test Equipment (ATE) with datalogging at each downpoint. Downpoint electrical testing was performed at room temperature. Post-irradiation anneals were performed using a small temperature chamber.

## 1.4 Experimental Matrix

Testing proceeded in accordance with the low dose rate sensitivity diagnostic protocol outlined in MIL-STD-883 Test Method 1019. The experimental matrix consisted of six samples irradiated at high dose rate with all pins grounded, six samples irradiated at high dose rate under bias, five samples irradiated at low dose rate with all pins grounded, and five samples irradiated at low dose rate under bias. One control unit was used.

A biased, high temperature anneal at 100ºC for 168 hours was performed following the high dose rate test to evaluate the accelerated aging characteristics of the process. The low dose rate samples were annealed under bias for 24 hours at room temperature followed by a second biased anneal for 168 hours at 100ºC.

Samples of the ISL70002SEH were drawn from lot WPW4J and were packaged in the standard, hermetic, 64 Ld Ceramic Quad Flatpack (CQFP) package; the date code was X1135ABBD. Samples were processed through the standard QML-V burnin screens of 180 hours dynamic and 72 hours static burn-in before irradiation, as required by MIL-STD-883, and were screened to the SMD 5962-12202 SMD limits at room, low, and high temperatures before the start of total dose testing.

## 1.5 Downpoints

Planned irradiation downpoints for both dose rates were 0krad(Si), 15krad(Si), 50krad(Si), 100krad(Si), and 150krad(Si). The high dose rate irradiations were followed by a biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature anneal and a 168-hour high temperature anneal at 100ºC, both under bias.

# 2. Results

## 2.1 Attributes Data

**Table 1. ISL70002SEH Total Dose Test Attributes Data**

| Part | Dose Rate, Rad(Si)/s | Bias | Sample Size | Downpoint | Pass (Note 1) | Fail |
|---|---|---|---|---|---|---|
| ISL70002SEH | 82.1rad(Si)/s | Figure 1 | 6 | Pre-irradiation | 6 | 0 |
| | | | | 15krad(Si) | 6 | 0 |
| | | | | 50krad(Si) | 6 | 0 |
| | | | | 100krad(Si) | 6 | 0 |
| | | | | 150krad(Si) | 6 | 0 |
| | | | | HT anneal | 6 | 0 |
| ISL70002SEH | 82.1rad(Si)/s | Grounded | 6 | Pre-irradiation | 6 | 0 |
| | | | | 15krad(Si) | 6 | 0 |
| | | | | 50krad(Si) | 6 | 0 |
| | | | | 100krad(Si) | 6 | 0 |
| | | | | 150krad(Si) | 6 | 0 |
| | | | | HT anneal | 6 | 0 |
| ISL70002SEH | 0.01rad(Si)/s | Figure 1 | 5 | Pre-irradiation | 5 | -- |
| | | | | 15krad(Si) | 5 | 0 |
| | | | | 50krad(Si) | 5 | 0 |
| | | | | 100krad(Si) | 5 | 0 |
| | | | | 150krad(Si) | 5 | 0 |
| | | | | RT anneal | 5 | 0 |
| | | | | HT anneal | 5 | 0 |
| ISL70002SEH | 0.01rad(Si)/s | Grounded | 5 | Pre-irradiation | 5 | -- |
| | | | | 15krad(Si) | 5 | 0 |
| | | | | 50krad(Si) | 5 | 0 |
| | | | | 100krad(Si) | 5 | 0 |
| | | | | 150krad(Si) | 5 | 0 |
| | | | | RT anneal | 5 | 0 |
| | | | | HT anneal | 5 | 0 |

Note:
1. “Pass” indicates a sample that passes all post-irradiation SMD limits.

## 2.2 Variables Data

The ISL70002SEH is a complex part and plotting all parameters would be a lengthy undertaking. The plots in Figures 3 through 25 show data for representative parameters at all downpoints. The plots show the median as a function of total dose for each of the irradiation conditions. We chose to use the median because of the relatively small sample sizes involved. All parts showed excellent stability over irradiation, with no observed low dose rate sensitivity. Most data is shown for an input (supply) voltage of 5.5V; the corresponding 3.6V data displayed equal stability and is not plotted. Several parameters (Figures 24 and 25) are informational and are not specified in either the datasheet or the SMD, and do not have formal parametric limits.

## 2.3 Variables Data Plots

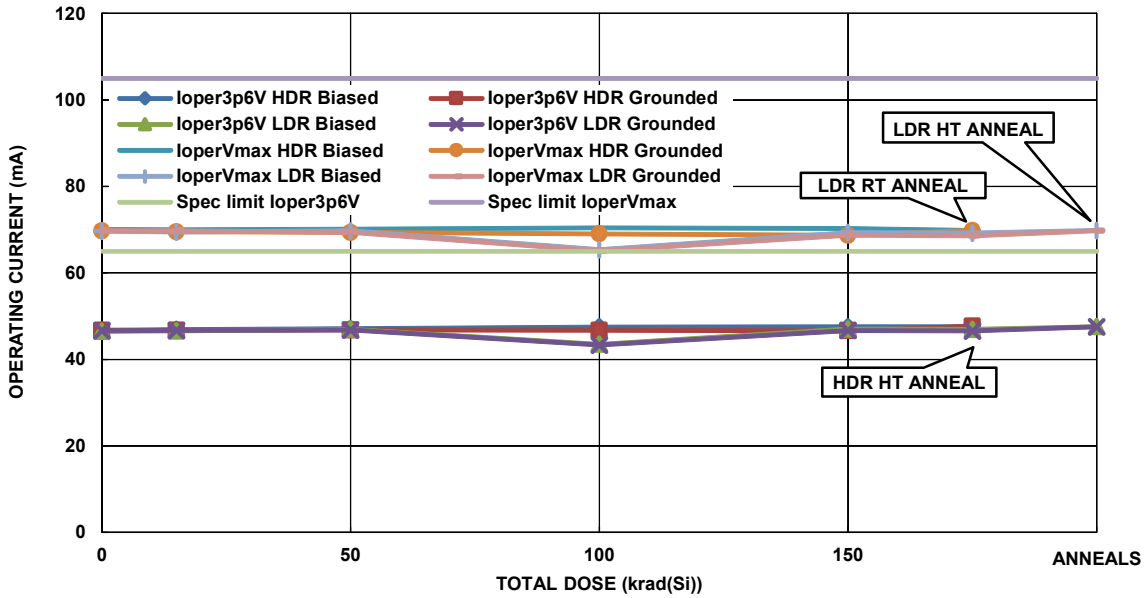



**Figure 3. ISL70002SEH operating current, current share disabled, 5.5V supply, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The SMD limit is 105mA maximum.**

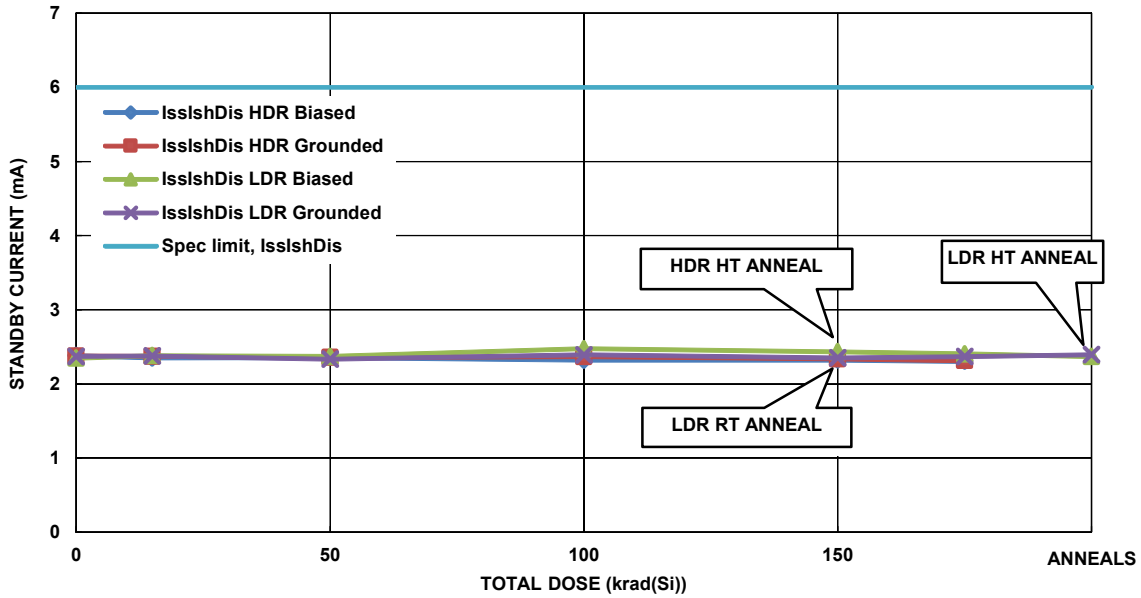



**Figure 4. ISL70002SEH standby supply current, current share disabled, 5.5V supply, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The SMD limit is 6mA maximum.**

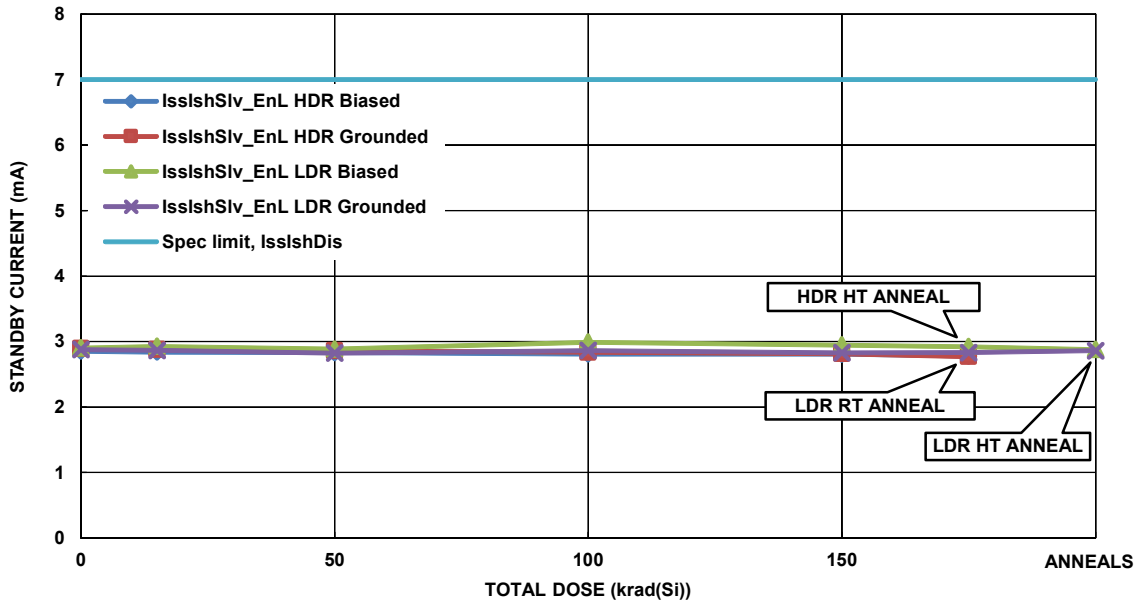



**Figure 5. ISL70002SEH standby supply current, current share enabled, 5.5V supply, master/slave and enable at ground, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The SMD limit is 7mA maximum.**

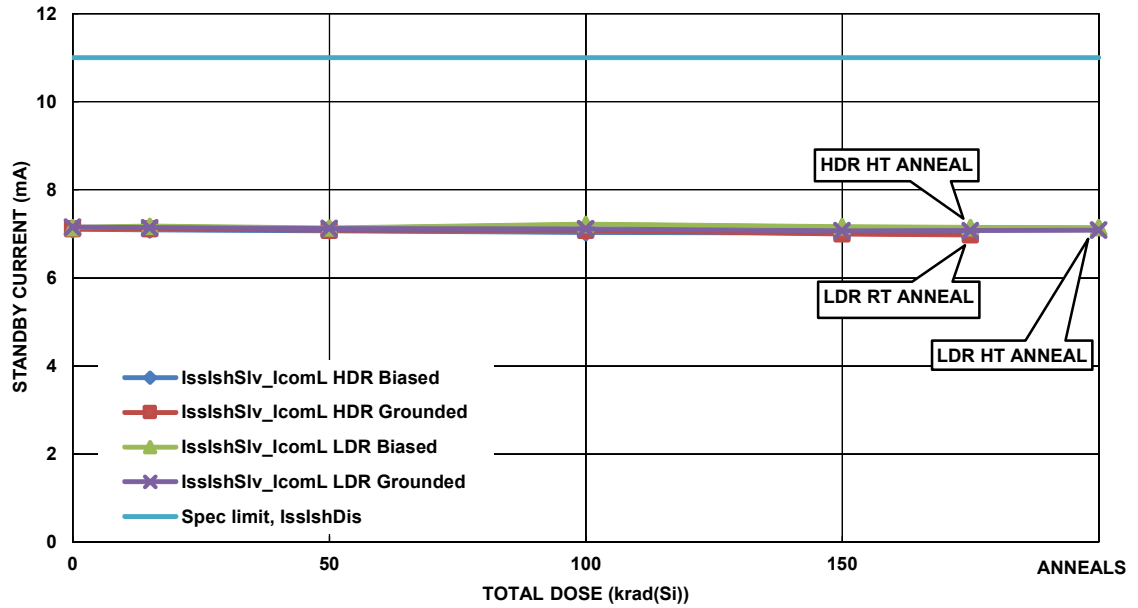



**Figure 6. ISL70002SEH standby supply current, current share enabled, 5.5V supply, master/slave at ground, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The SMD limit is 11mA maximum.**

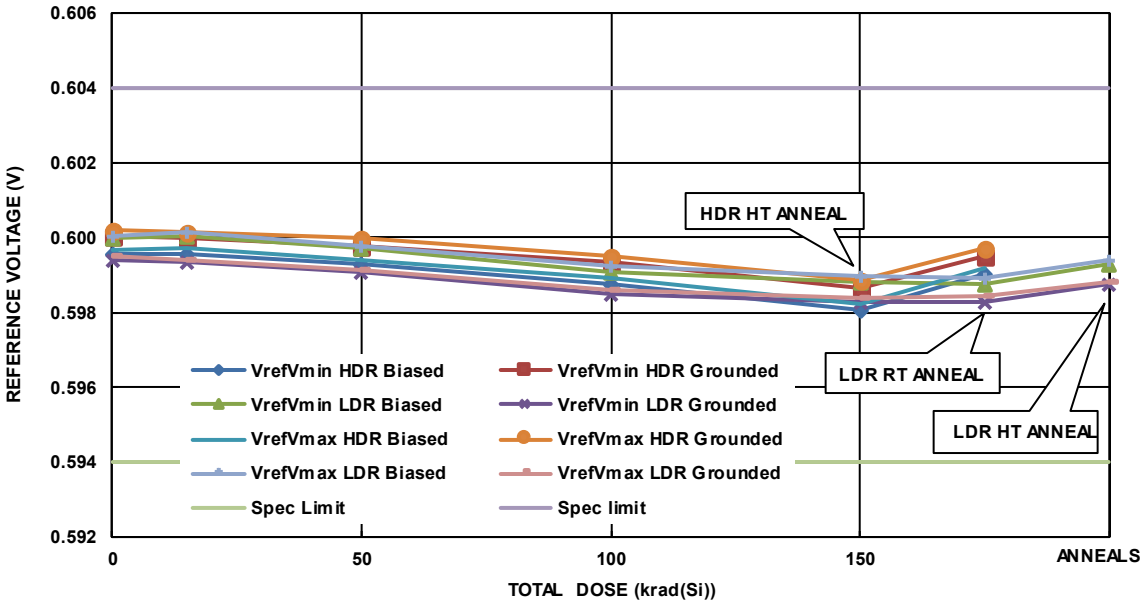



**Figure 7. ISL70002SEH reference voltage for supply voltages of 3.6V (Vmin) and 5.5V (Vmax) as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The SMD post-irradiation limits are 0.594V to 0.604V.**

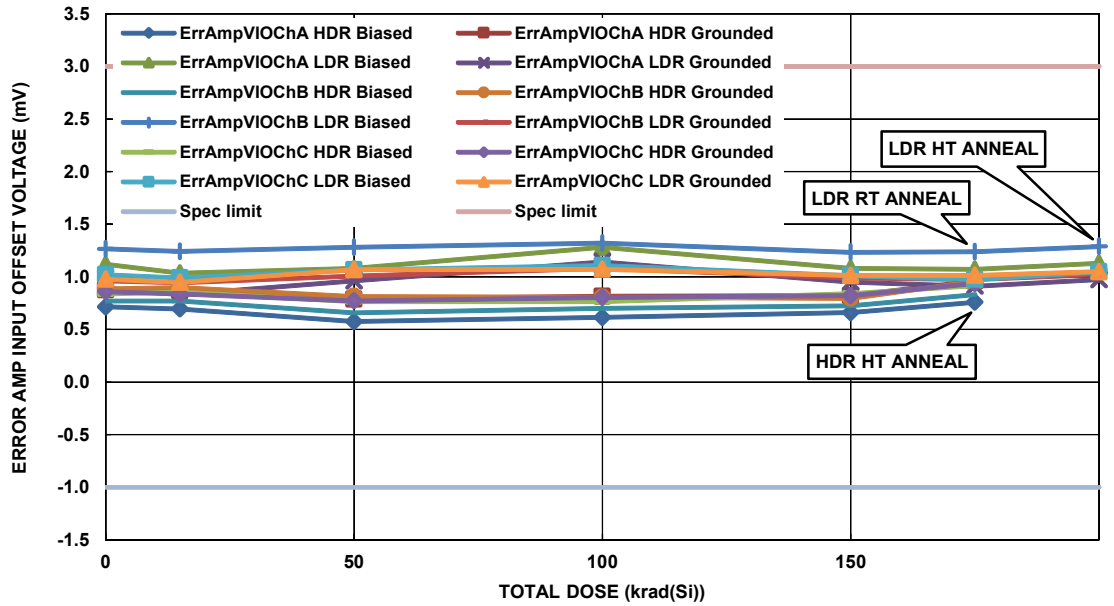



**Figure 8. ISL70002SEH error amplifier input offset voltage, 5.5V supply, each channel, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The SMD limits are -1mV to 3mV.**

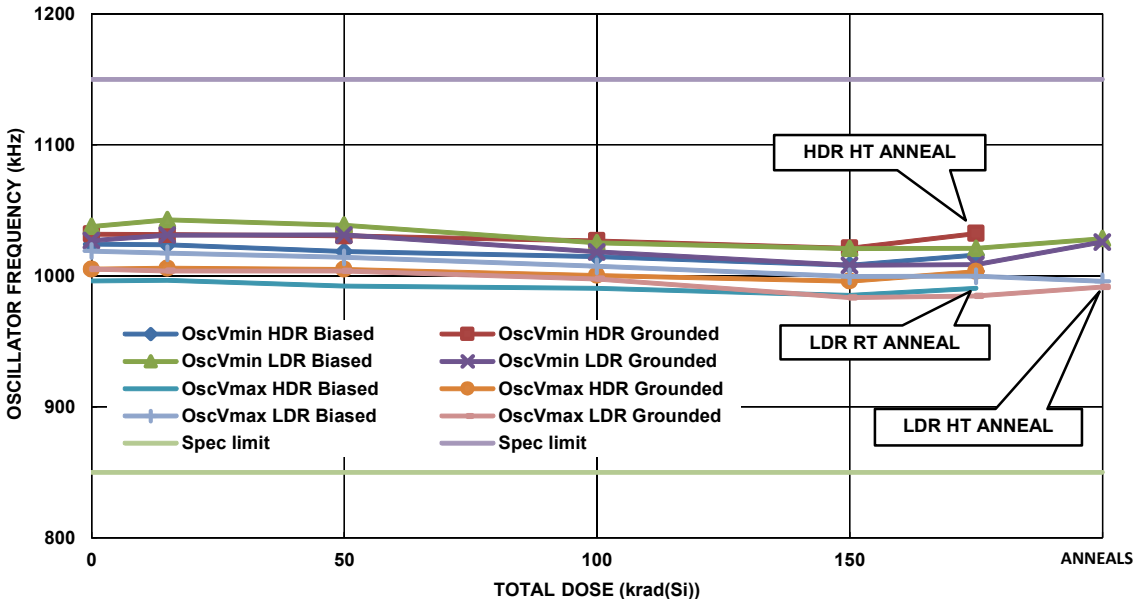



**Figure 9. ISL70002SEH internal oscillator tolerance as a function of total dose irradiation, 5.5V supply, at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The SMD limits are -15% to 15%; for a nominal frequency of 1MHz this translates to a frequency range of 850kHz to 1150kHz.**

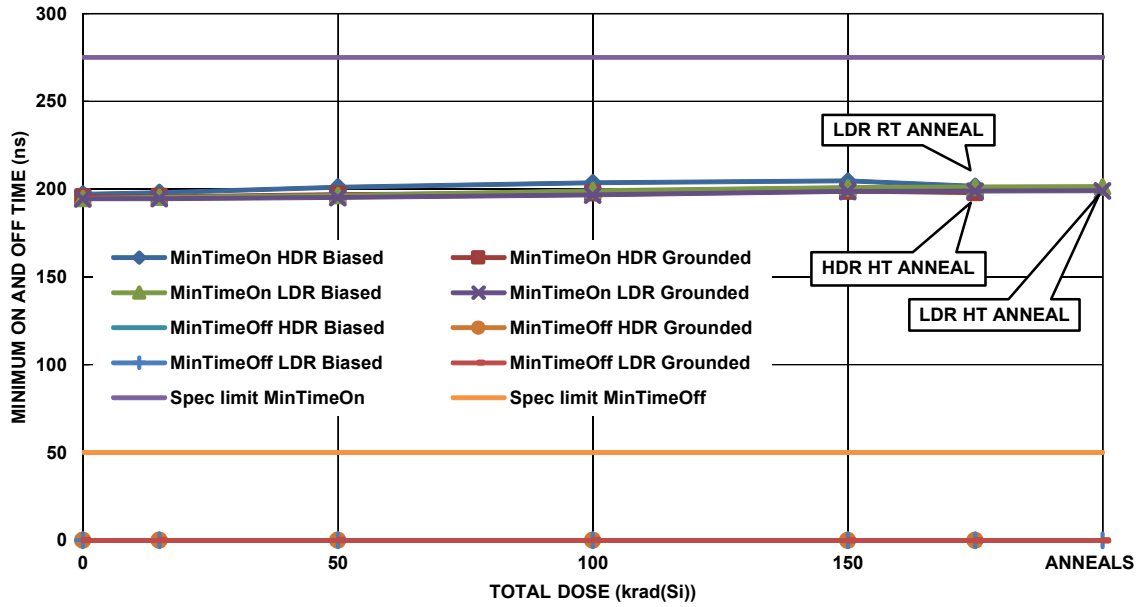



**Figure 10. ISL70002SEH minimum LXx ON and OFF time, 5.5V supply, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The SMD limits are 275ns maximum (ON time) and 50ns maximum (OFF time).**

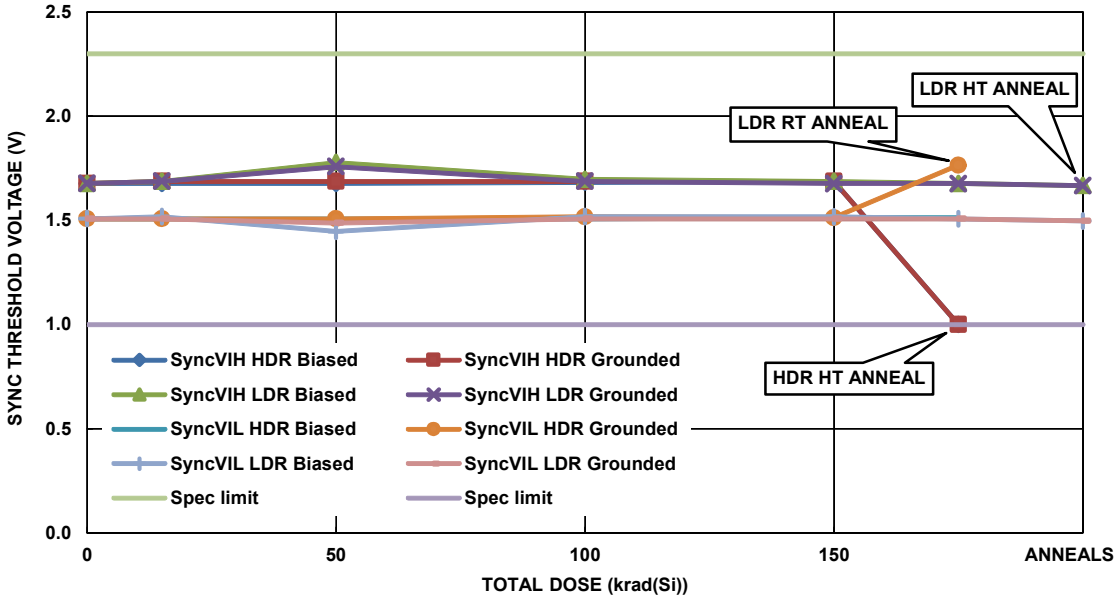



**Figure 11. ISL70002SEH sync input HIGH and LOW threshold voltage, 5.5V supply, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The SMD limits are 2.3V maximum (HIGH) and 1V minimum (LOW).**

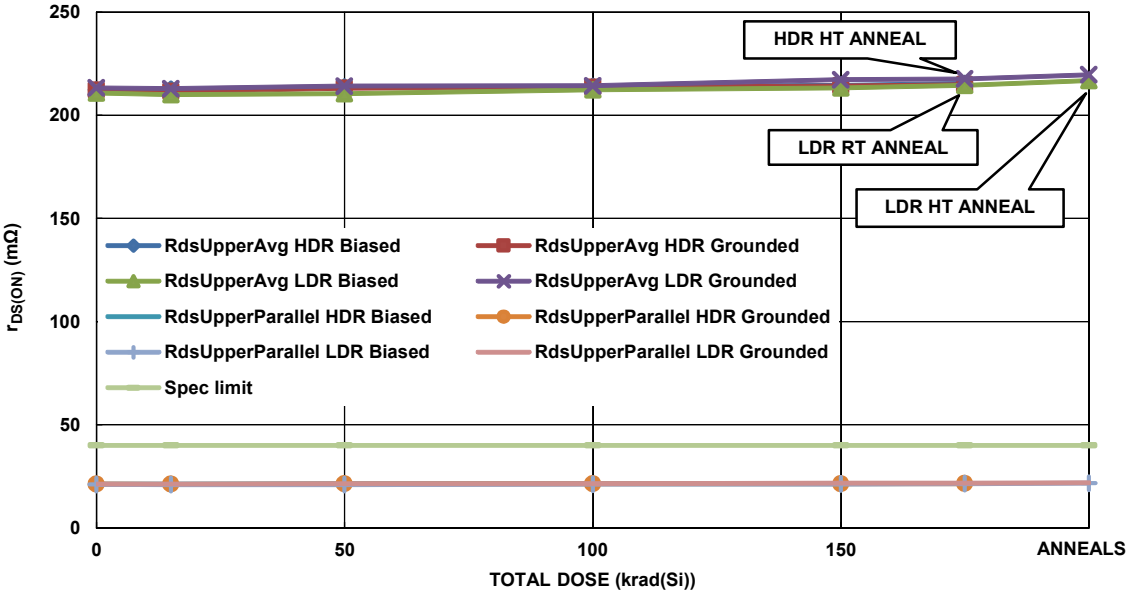



**Figure 12. ISL70002SEH average upper device drain-to-source ON resistance ($r_{DS(ON)}$) and parallel (all ten power blocks) $r_{DS(ON)}$, 5.5V supply, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The SMD parallel $r_{DS(ON)}$ limit is 40mΩ maximum; the average $r_{DS(ON)}$ is not specified.**

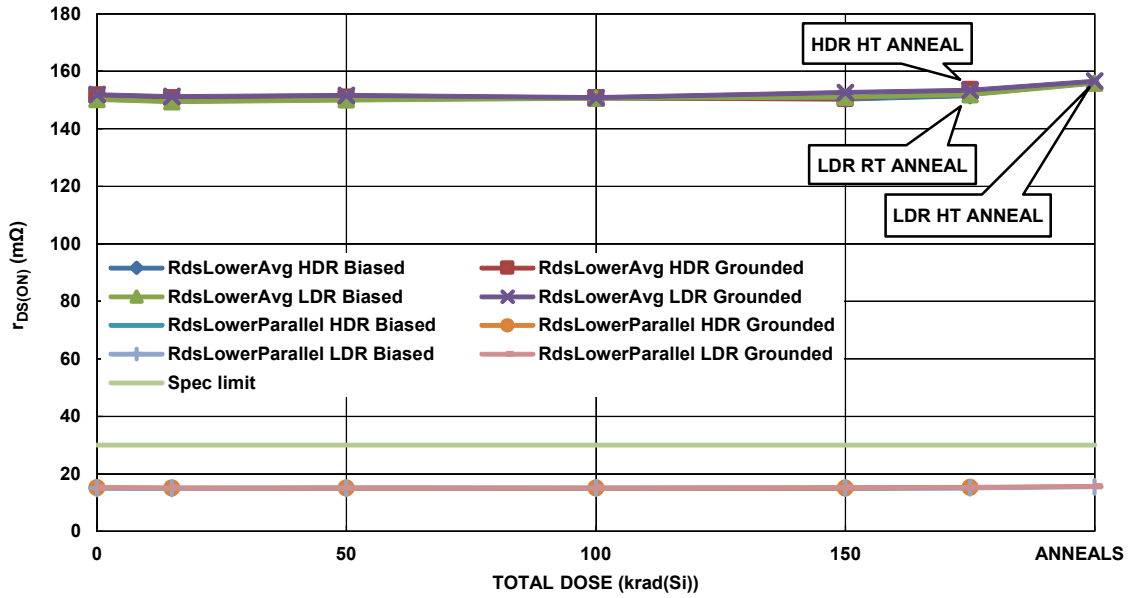



**Figure 13. ISL70002SEH average lower device drain-to-source ON resistance ($r_{DS(ON)}$) and parallel (all ten power blocks) $r_{DS(ON)}$ as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The SMD parallel $r_{DS(ON)}$ limit is 30mΩ maximum; the average $r_{DS(ON)}$ is not specified.**

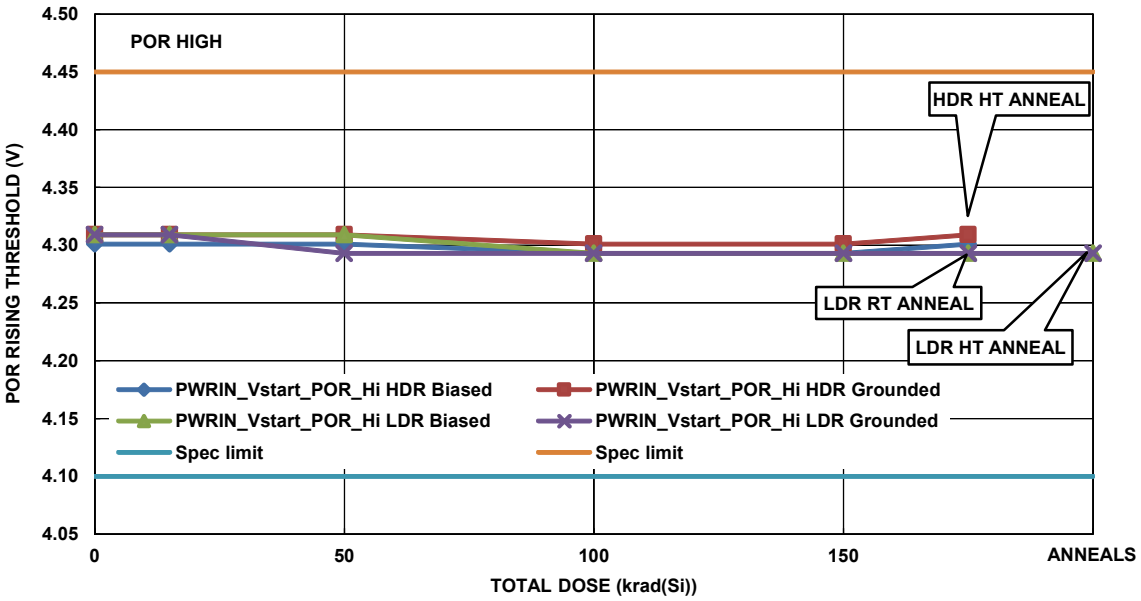



**Figure 14. ISL70002SEH Power-On-Reset (POR) rising threshold, POR select at input voltage, 5.5V supply, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The SMD limits are 4.10V to 4.45V.**

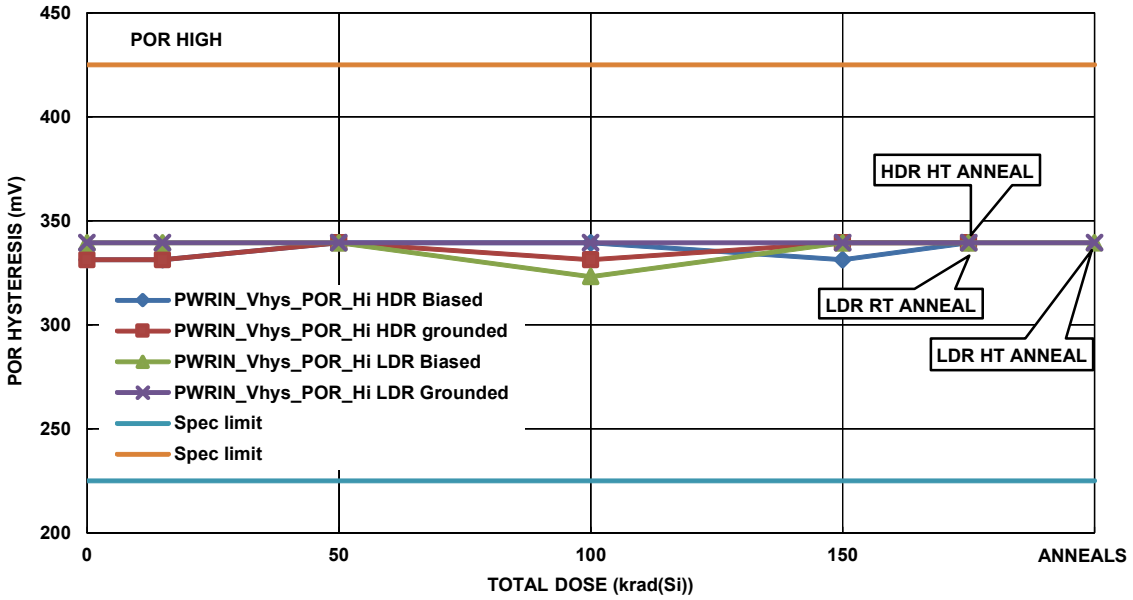



**Figure 15. ISL70002SEH POR hysteresis, POR select at input voltage, 5.5V supply, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The SMD limits are 225mV to 425mV.**

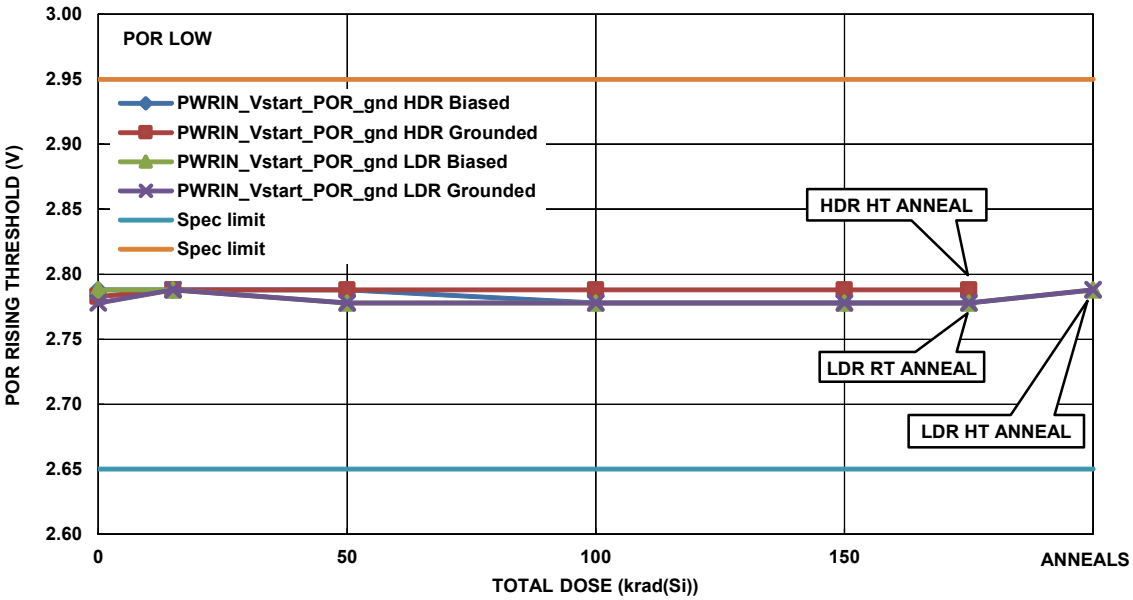



**Figure 16. ISL70002SEH POR rising threshold, POR select at ground, 5.5V supply, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The SMD limits are 2.65V to 2.95V.**

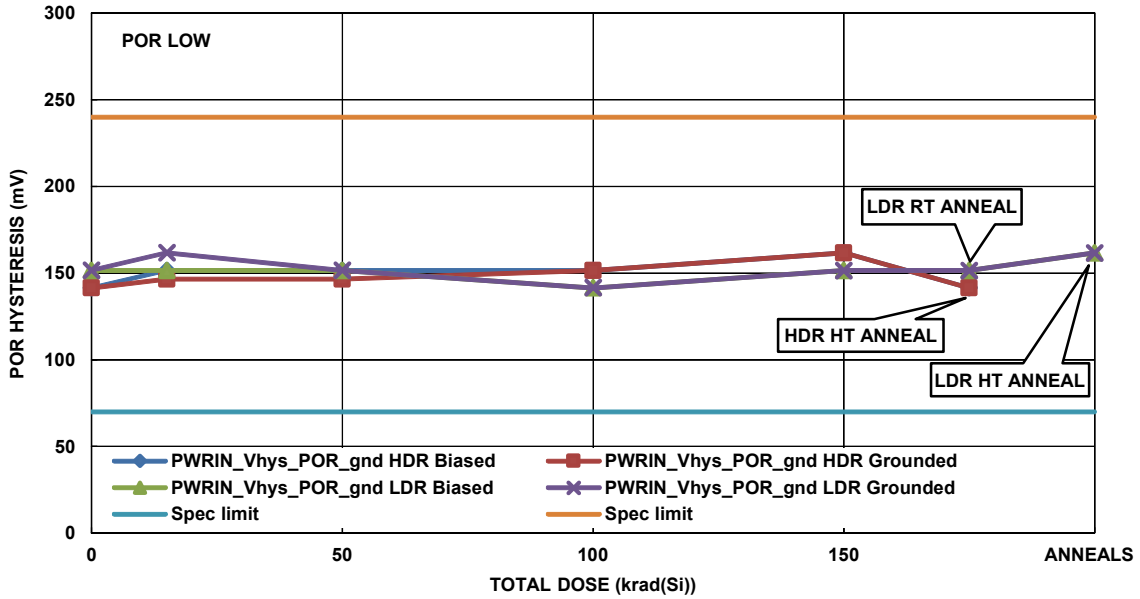



**Figure 17. ISL70002SEH POR hysteresis voltage, POR select at ground, 5.5V supply, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The SMD limits are 70mV to 240mV.**

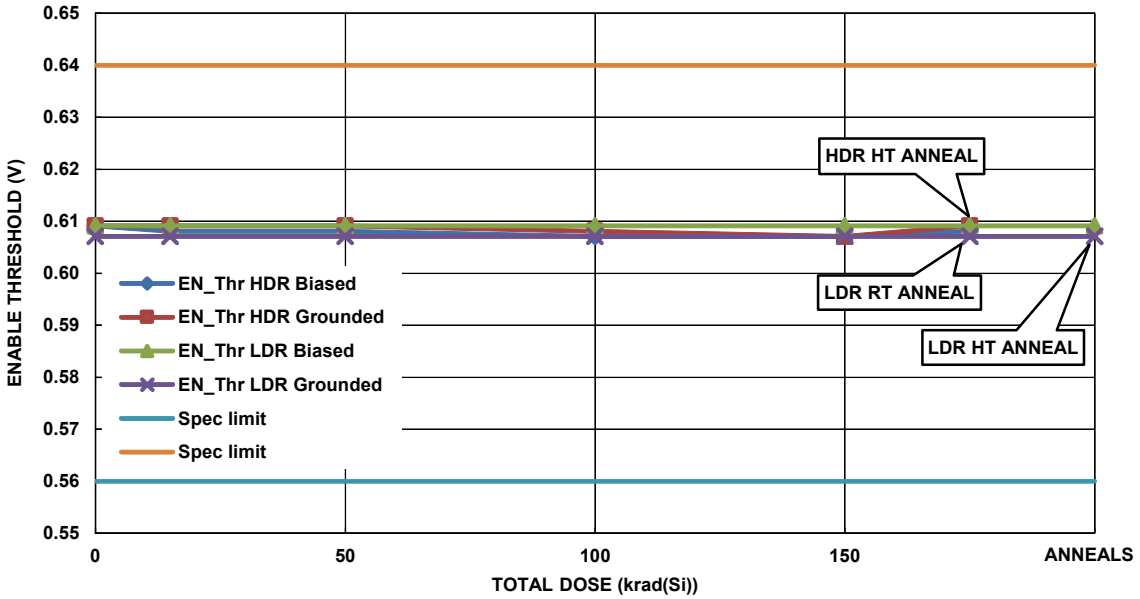



**Figure 18. ISL70002SEH enable rising and falling threshold voltage, 5.5V supply, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The SMD limits are 0.56V to 0.64V.**

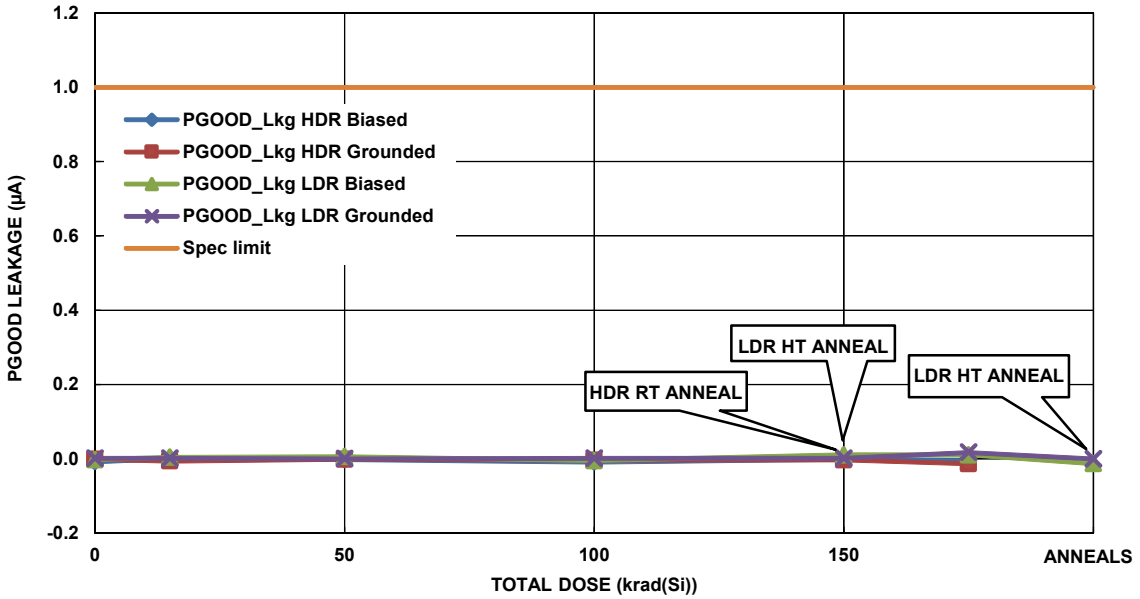



**Figure 19. ISL70002SEH Power-Good (PGOOD) leakage, 5.5V supply, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The SMD limit is 1µA maximum.**

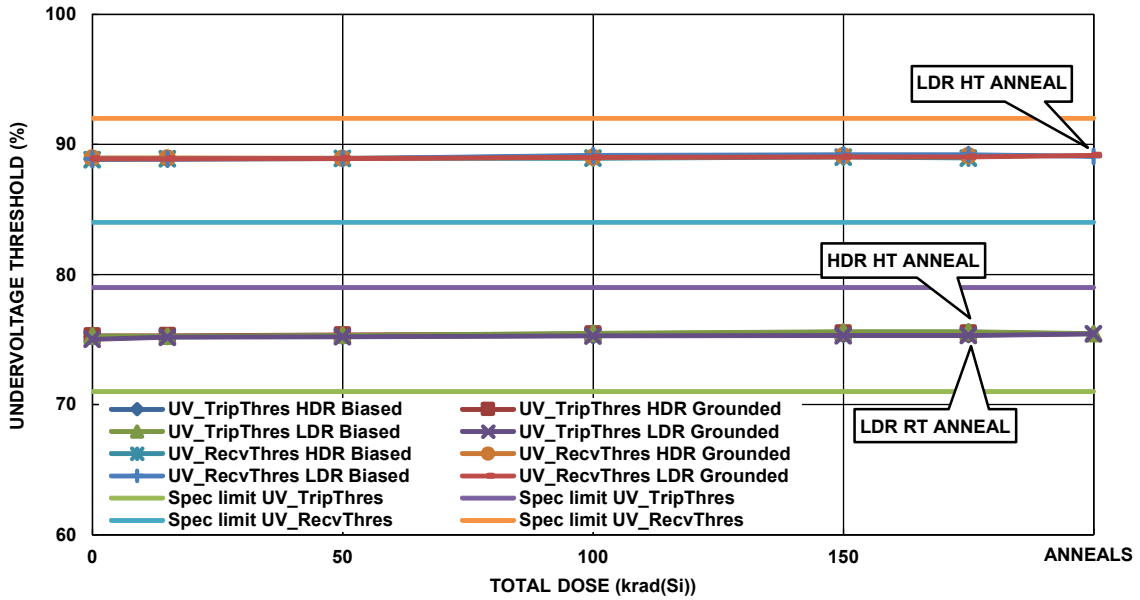



**Figure 20. ISL70002SEH Undervoltage (UV) trip threshold and recovery threshold, 5.5V supply, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The SMD limits are 71% to 79% (UV trip threshold) and 84% to 92% (UV recovery threshold).**

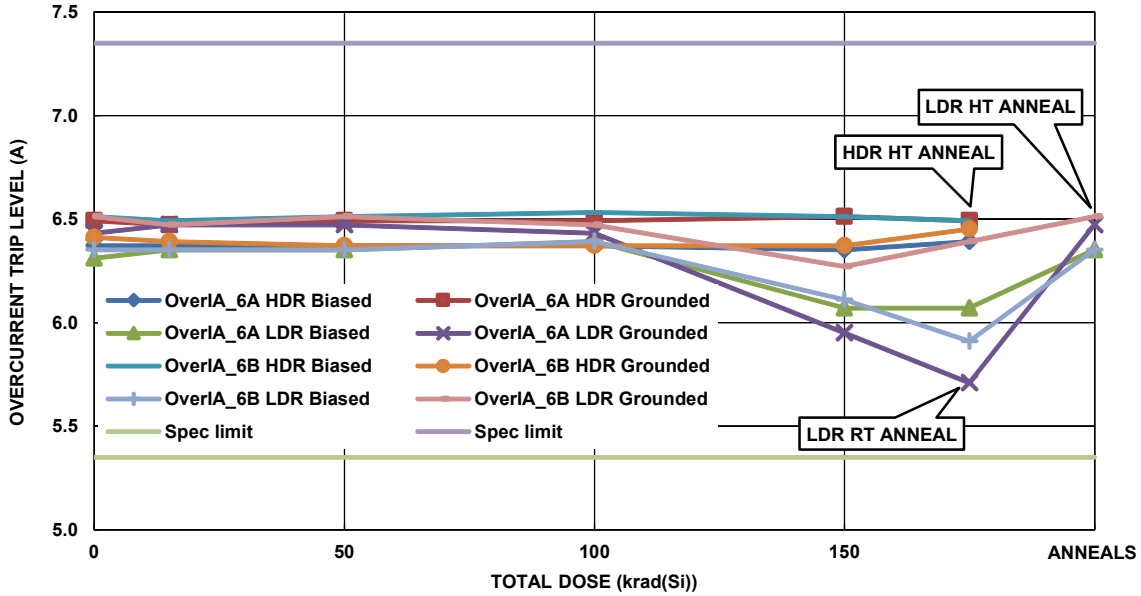



**Figure 21. ISL70002SEH Overcurrent (OC) trip threshold, 6A case, 5.5V supply, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The SMD limits are 5.75A to 7.35A.**

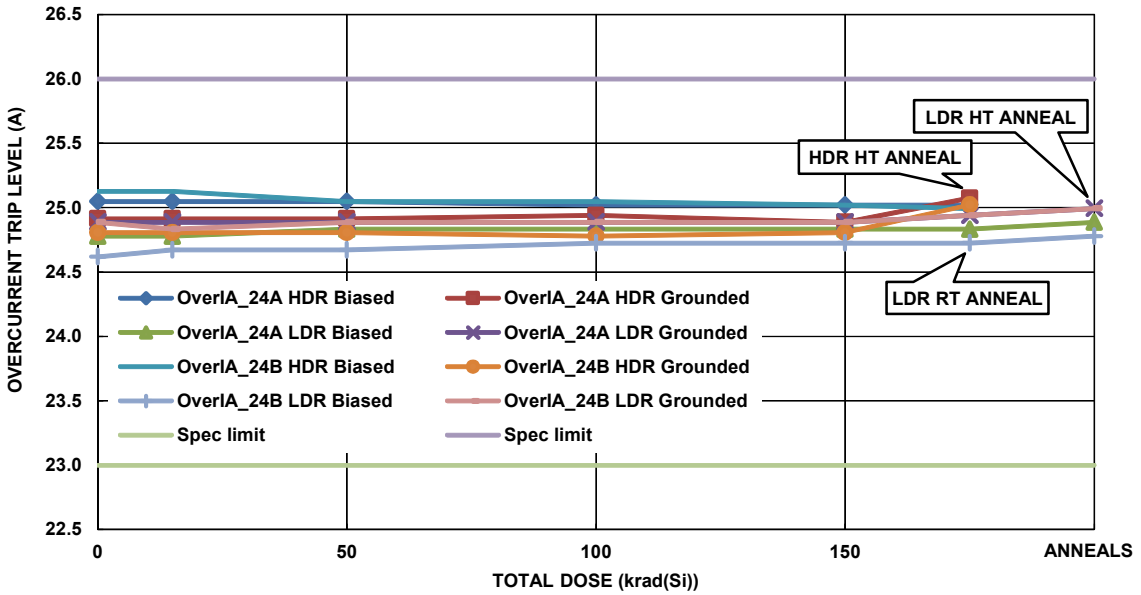



**Figure 22. ISL70002SEH OC trip threshold, 24A case, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The SMD limits are 23A to 26A.**

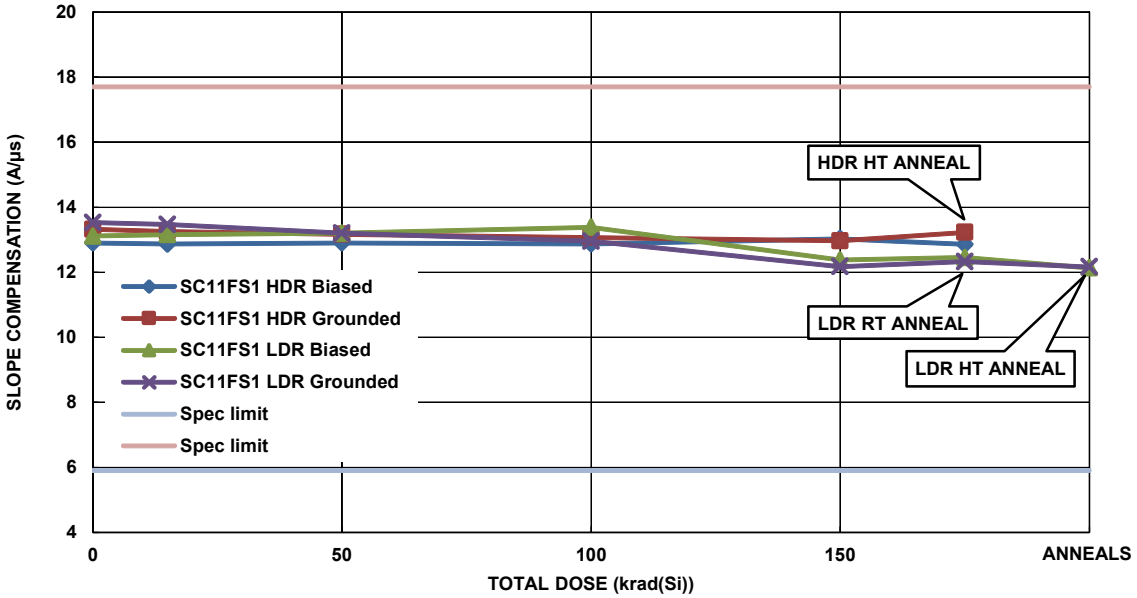



**Figure 23. ISL70002SEH slope compensation referred to $V_{OUT}$, SC1 = SC0 = $V_{IN}$, as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The SMD limits are 5.9A/µs to 17.7A/µs.**

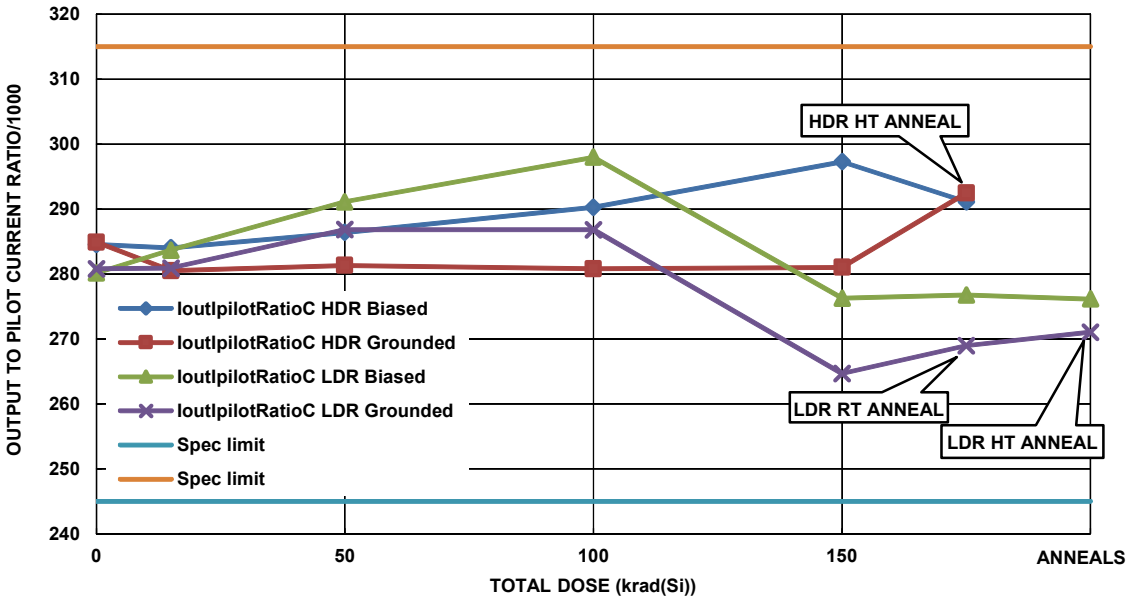



**Figure 24. ISL70002SEH output current to pilot current ratio divided by 1000 as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. The parameter is not specified in the SMD; the ATE limits are 245000 to 315000. This ratio is a dimensionless value.**

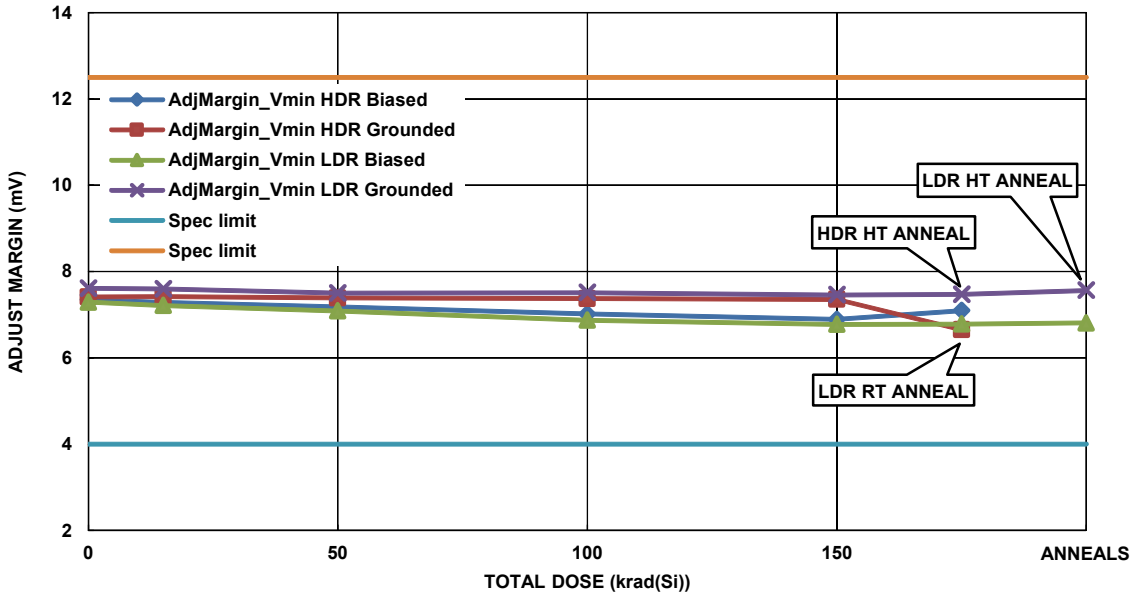



**Figure 25. ISL70002SEH adjust margin at 3.6V supply as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate was 82.1rad(Si)/s. The high dose rate irradiations were followed by a high temperature biased anneal at 100ºC for 168 hours. The low dose rate irradiations were followed by a 24-hour room temperature and a 168-hour 100ºC anneal, both under bias. Sample size for the high dose rate cells was six for each cell, while the low dose rate cells were five samples each. This parameter is not specified in the SMD; the ATE limits are 4mV to 12.5mV.**

# 3. Conclusions

This document reports the results of total dose testing of the ISL70002SEH hardened POL regulator. Parts were tested at low and high dose rates under biased and unbiased conditions as outlined in MIL-STD-883 Test Method 1019.7, to a total dose of 150krad(Si) at each dose rate. A biased, high temperature anneal at 100ºC for 168 hours was performed following the high dose rate test to evaluate the accelerated aging characteristics of the process. The low dose rate samples were annealed under bias for 24 hours at room temperature followed by a second biased anneal for 168 hours at 100ºC.

ATE characterization testing at all downpoints showed no rejects to the datasheet limits. Variables data for selected parameters is presented in Figures 3 through 25.

No low dose rate sensitivity was noted and all parameters showed excellent stability. No differences between biased and unbiased irradiation were noted. The part is not considered dose rate or bias sensitive. The anneals had little effect at either dose rate.

# 4. Appendix

**Table 2. Reported Parameters**

| Figure | Parameter | Limit, Low | Limit, High | Units | Notes |
|---|---|---|---|---|---|
| 3 | Operating Current | - | 105 | mA | $I_{share}$ disabled, 5.5V supply |
| 4 | Standby Supply Current | - | 6 | mA | $I_{share}$ enabled, 5.5V supply |
| 5 | Standby Supply Current | - | 7 | mA | $I_{share}$ disabled, 5.5V supply |
| 6 | Standby Supply Current | - | 11 | mA | 5.5V supply |
| 7 | Reference Voltage | 0.594 | 0.604 | V | 3.6 and 5.5V supply |
| 8 | Error Amplifier Input Offset Voltage | -1 | 3 | mV | 5.5V supply |
| 9 | Internal Oscillator Tolerance | 850 | 1150 | MHz | 5.5V supply |
| 10 | Minimum LXx On and Off Time | - | 275 | ns | 5.5V supply |
| | | - | 50 | | |
| 11 | Sync Input High and Low Threshold Voltage | - | 2.3 | V | 5.5V supply |
| | | 1 | - | V | |
| 12 | Average and Parallel Upper Device $r_{DS(ON)}$ | - | - | mΩ | |
| | | 40 | - | mΩ | |
| 13 | Average and Parallel Lower Device $r_{DS(ON)}$ | - | - | mΩ | |
| | | 30 | - | mΩ | |
| 14 | POR Rising Threshold | 4.10 | 4.45 | V | POR select at supply |
| 15 | POR Hysteresis Voltage | 225 | 426 | mV | POR select at supply |
| 16 | POR Rising Threshold | 2.65 | 2.95 | V | POR select at ground |
| 17 | POR Hysteresis Voltage | 70 | 240 | mV | POR select at ground |
| 18 | Enable Rising and Falling Threshold Voltage | 0.56 | 0.64 | V | 5.5V supply |
| 19 | PGOOD Leakage | - | 1 | µA | 5.5V supply |
| 20 | Undervoltage and Recovery Threshold Voltage | 71 | 79 | % | |
| | | 84 | 92 | | |
| 21 | Overcurrent Trip Threshold | 5.75 | 7.35 | A | 6A case |
| 22 | Overcurrent Trip Threshold | 23 | 26 | A | 24A case |
| 23 | Slope Compensation | 5.9 | 17.7 | A/µs | SC1 = SC0 = $V_{IN}$ |
| 24 | Output to Pilot Current Ratio | 245000 | 315000 | - | ATE limit |
| 25 | Adjust Margin | 4 | 12.5 | mV | ATE limit |

# 5. Revision History

| Rev. | Date | Description |
|---|---|---|
| 1.00 | May 27, 2020 | Updated Figure 7. |
| 0.00 | Aug 31, 2017 | Initial release |

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