Total dose testing of the HS-4080AEH full bridge N-channel MOSFET driver

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1. Introduction and Executive Summary

This report discusses the results of total dose testing of the HS-4080AEH full-bridge N-channel power MOSFET driver. These tests were conducted to provide an assessment of the total dose hardness of the part and its dose rate and bias sensitivity. Samples were irradiated under bias and with all pins grounded at low dose rate and under bias at high dose rate. Following irradiation, the low dose rate samples were subjected to a biased high temperature anneal to evaluate the part's accelerated aging response. The HS-4080AEH is acceptance tested on a wafer by wafer basis to 300 krad(Si) at high dose rate (50 – 300 rad(Si)/s) and to 50 krad(Si) at low dose rate (0.01 rad(Si)/s), assuring TID hardness to the specified level for both dose rates.

The HS-4080AEH and HS-4080ARH differ only in their total dose hardness assurance flows. The HS-4080AEH is acceptance tested on a wafer by wafer basis to 50 krad(Si) at low dose rate (0.01 rad(Si)/s) under biased and grounded conditions and to 300 krad(Si) at high dose rate (50 – 300 rad(Si)/s) under biased conditions. The HS-4080ARH is acceptance tested on a wafer by wafer basis to 300 krad(Si) at high dose rate (50 – 300 rad(Si)/s) under biased conditions.

The HS-4080AEH showed good performance over low and high dose rate irradiation. All samples passed the post-irradiation specifications at the total dose levels specified in the SMD. We observed dose rate sensitivity and bias sensitivity in some parameters, see the Discussion section, and the part is considered moderately low dose rate sensitive. We also saw a few biased high temperature anneal responses in the parts subjected to that procedure, and these responses will be discussed as well.

2. Reference Documents

MIL-STD-883 test method 1019.
HS-4080AEH data sheet.
Standard Microcircuit Drawing (SMD) 5962 – 99617

3: Part Description

The HS-4080AEH and HS-4080ARH are high frequency medium voltage full bridge N-channel power MOSFET drivers. The device includes a TTL-level input comparator, which can be used to facilitate the "hysteresis" and PWM modes of operation. The high side enable HEN pin can be used to force current to freewheel in the bottom two external power MOSFETs while maintaining the upper power MOSFETs off. The HS-4080AEH and HS-4080ARH are well suited for use in distributed DC power supplies and DC/DC converters, since the parts can switch at high frequencies. These devices can also drive medium voltage motors, and two HS-4080ARH or HS-4080AEHs can be used to drive high performance stepper motors, since the short minimum "on-time" can provide fine micro-stepping capability. Short propagation delays maximize control loop crossover frequencies and dead-times, which can be adjusted to near zero to minimize distortion, resulting in precise control of the driven load.

The HS-4080AEH is produced using the Intersil dielectrically isolated (DI) radiation hardened silicon gate (RSG) BiCMOS process. The DI substrate results in assured single-event latchup (SEL) immunity and the parts provide highly reliable performance in harsh radiation environments.

• DLA Standard Microcircuit Drawing	5962-99617
• Maximum bootstrap supply	95V
• Load capacitance, 50ns	1000pF
• User-programmable deadtime	
• Single-supply operation	12V to 18V
• Operating temperature range	-55°C to +125°C
• Radiation environments:	
- High dose rate (50 – 300 rad(Si)/s)	300 krad(Si)
- Low dose rate (0.01 rad(Si)/s)	50 krad(Si)

4: Test Description

4.1 Irradiation Facilities

High dose rate testing was performed at a nominal dose rate of 68 rad(Si)/s using a Gammacell 220™ ^{60}Co irradiator located in the Palm Bay, Florida Intersil facility. Low dose rate testing was performed at 0.01 rad(Si)/s using the Intersil Palm Bay N40 panoramic low dose rate ^{60}Co irradiator. Post-irradiation high temperature biased anneals were performed using a small temperature chamber.

4.2 Test Fixturing

Figure 1 shows the configuration used for biased irradiation. The grounded irradiations were performed in the same fixture type but with all pins hardwired to ground. Post-irradiation high temperature biased anneals were performed using this configuration as well.

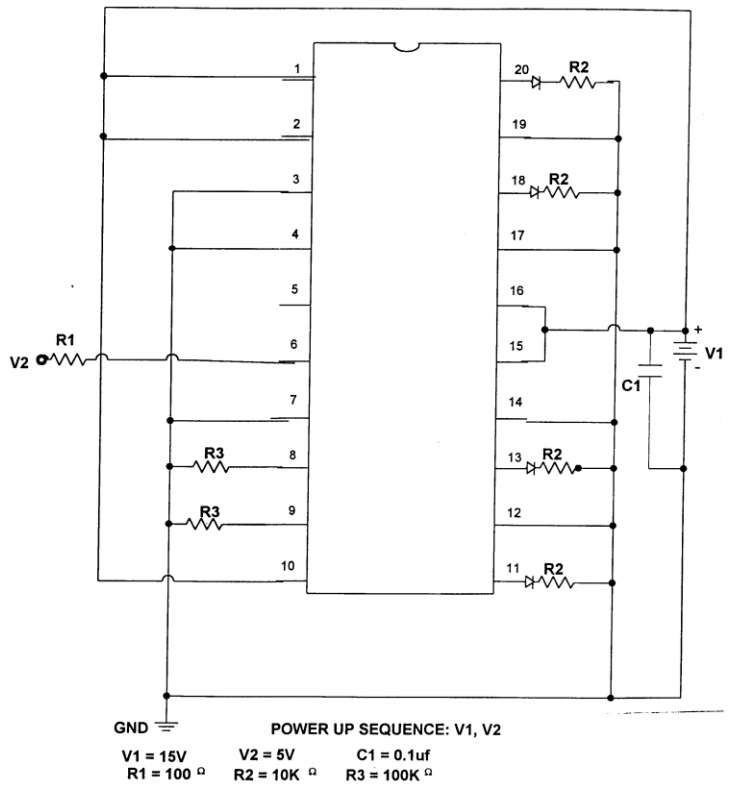

Fig. 1: Biased irradiation configuration for the HS-4080AEH.

4.3 Characterization equipment and procedures

All electrical testing was performed outside the irradiator using the production automated test equipment (ATE) with datalogging at each downpoint. All downpoint electrical testing was performed at room temperature. One control unit was used to verify repeatability.

4.4 Experimental matrix

The experimental matrix is shown in Table 1. Samples of the HS-4080AEH were drawn from preproduction lot G0X0WBEH and were packaged in hermetic 20-pin ceramic flatpacks (package code

CDFP4-F20). Samples were processed through the standard burnin cycle before irradiation, as required by MIL-STD-883, and were screened to the ATE limits at room temperature prior to the test.

A biased post-irradiation high temperature anneal was performed on the post low dose rate irradiation HS-4080AEH samples. The anneal was performed at 100°C for 168 hours using the Fig. 1 bias configuration.

4.5 Downpoints

Downpoints and pass/fail statistics are shown in the attributes data table (Table 1).

5: Results

5.1 Attributes data

Table 1: HS-4080AEH total dose test attributes data.

Part	Dose rate, rad(Si) (Note 1)	Bias	Sample size	Downpoint	Pass (Note 2)	Rejects
HS-4080AEH	HDR	Biased	20	Pre-irradiation	20	
				300 krad(Si)	20	0
HS-4080AEH	LDR	Biased	10	Pre-irradiation	10	
				50 krad(Si)	10	10
				100 krad(Si)	10	10
				150 krad(Si)	10	10
				Anneal	10	
HS-4080AEH	LDR	Grounded	10	Pre-irradiation	10	
				50 krad(Si)	10	10
				100 krad(Si)	10	10
				150 krad(Si)	10	10
				Anneal	10	

Note 1: 'HDR' indicates high dose rate (50 – 300 rad(Si)/s); the actual dose rate for these tests was 68 rad(Si)/s. 'LDR' indicates low dose rate (0.01 rad(Si)/s).

Note 2: 'Pass' indicates a sample that passes all post-irradiation SMD limits.

5.2 Variables data

The plots in Figures 2 through 57 show data at all downpoints. The plots report the response to total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased (Fig.1) case. The plots also show the response to the biased 168-hour 100°C high temperature anneal performed after low dose rate irradiation. We chose to plot the average for these parameters due to the relatively large sample sizes, and show the minimum and maximum values for each datapoint as well. Section 6 will provide individual discussion of the figures.

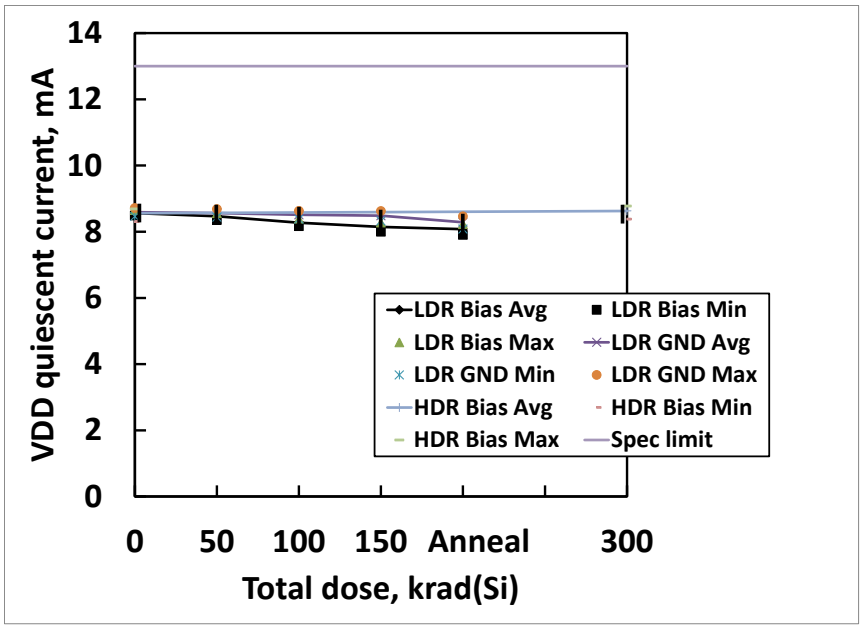

Fig. 2: HS-4080AEH lower gate driver ('VDD') quiescent power supply current as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100ºC for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 13.0mA maximum. (112)

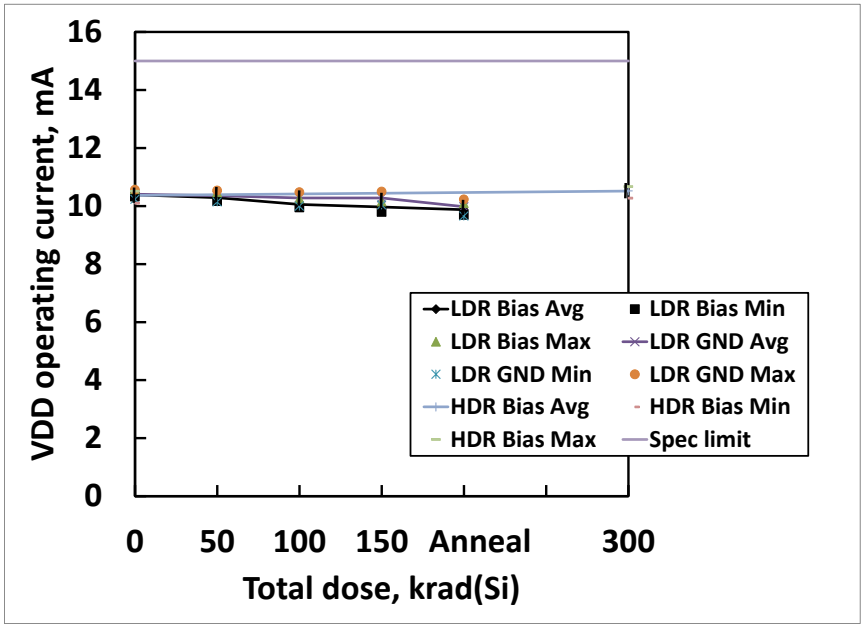

Fig. 3: HS-4080AEH lower gate driver ('VDD') operating power supply current as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100ºC for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 15.0mA maximum. (114)

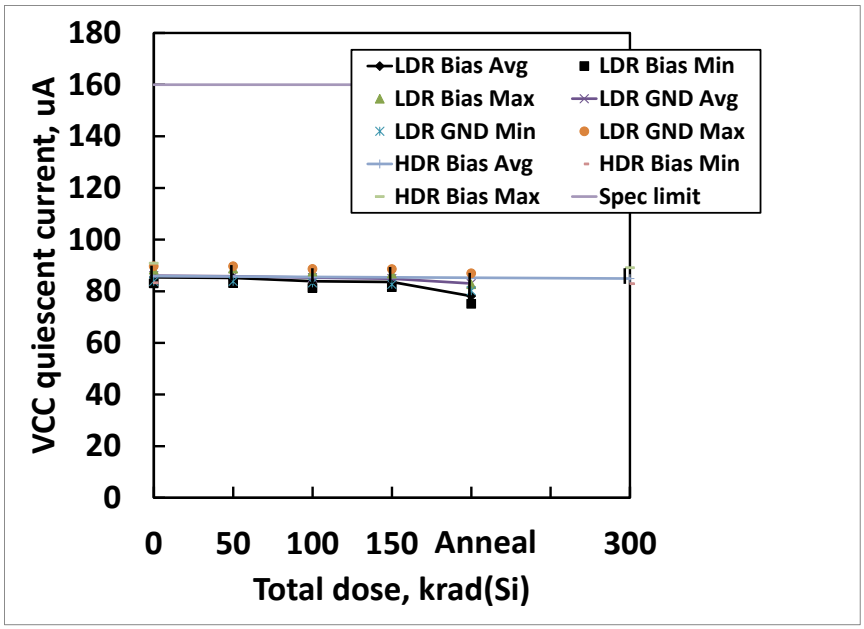

Fig. 4: HS-4080AEH upper gate driver ('VCC') quiescent power supply current as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 160.0uA maximum. (113)

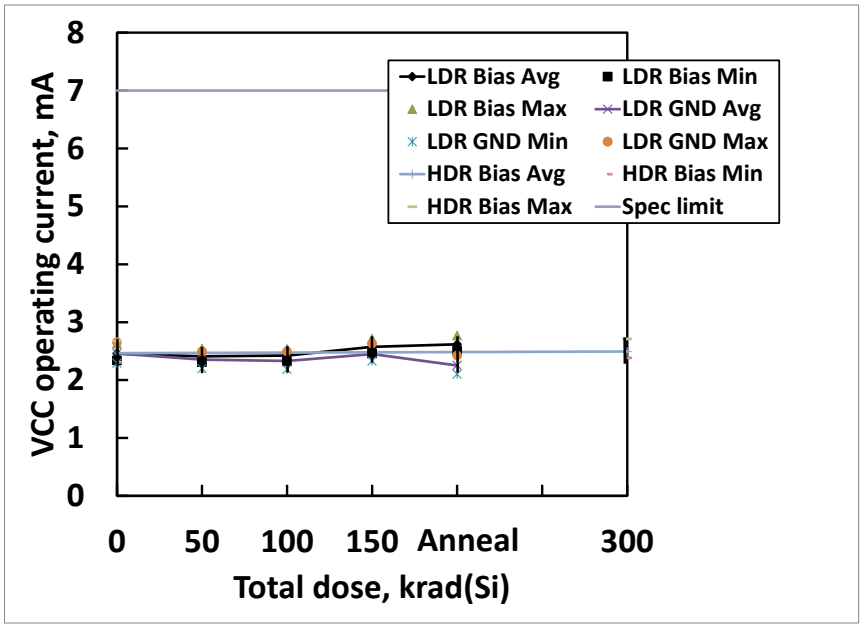

Fig. 5: HS-4080AEH upper gate driver ('VCC') operating power supply current as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 7.0mA maximum. (115)

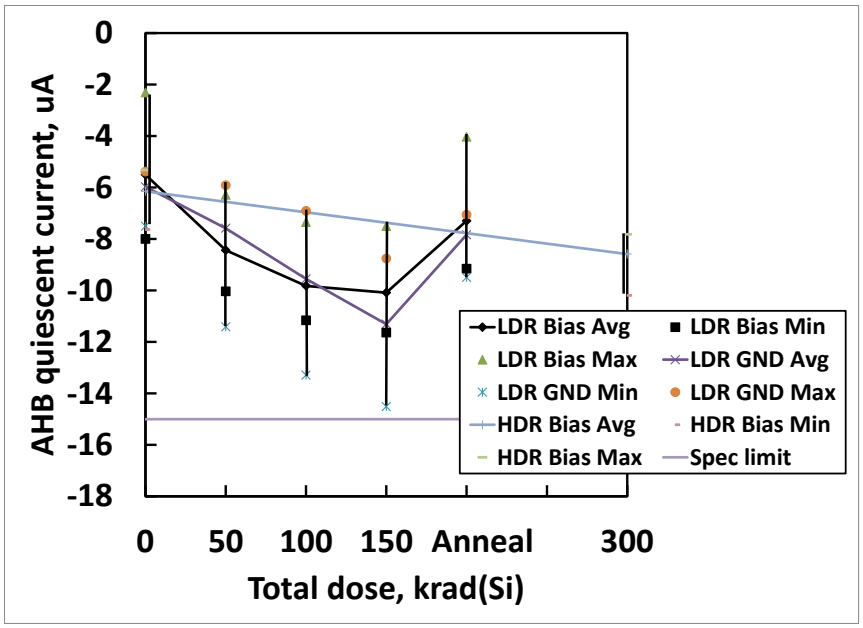

Fig. 6: HS-4080AEH A high side bootstrap supply quiescent current as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is -15.0uA maximum. (127)

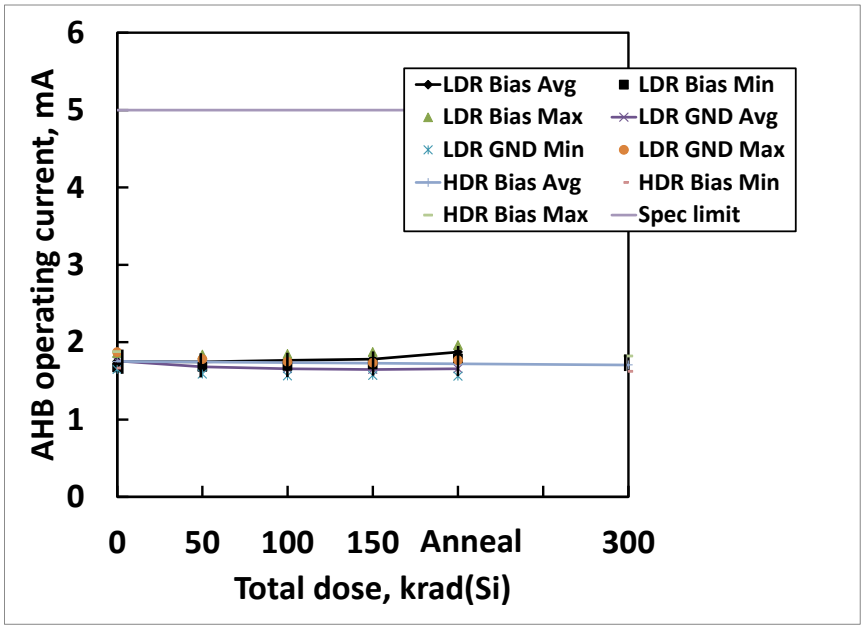

Fig. 7: HS-4080AEH A high side bootstrap supply operating current as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is -15.0uA maximum. (128)

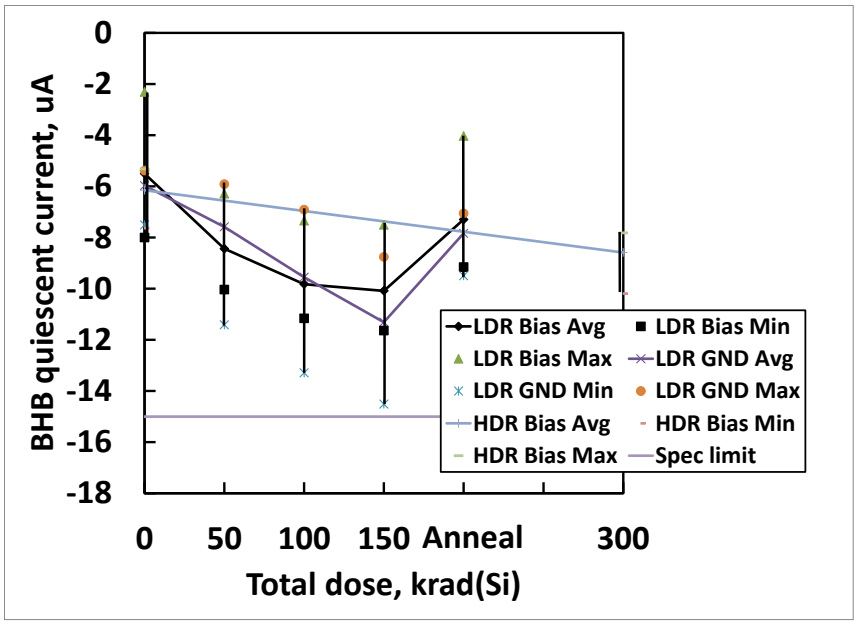

Fig. 8: HS-4080AEH B high side bootstrap supply quiescent current as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is -15.0uA maximum. (126)

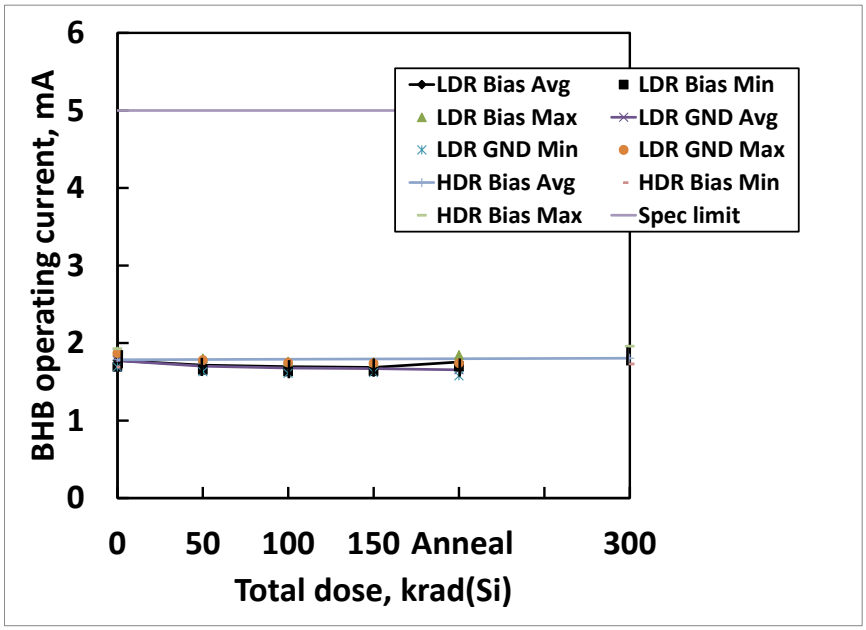

Fig. 9: HS-4080AEH B high side bootstrap supply operating current as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 5.0mA maximum. (129)

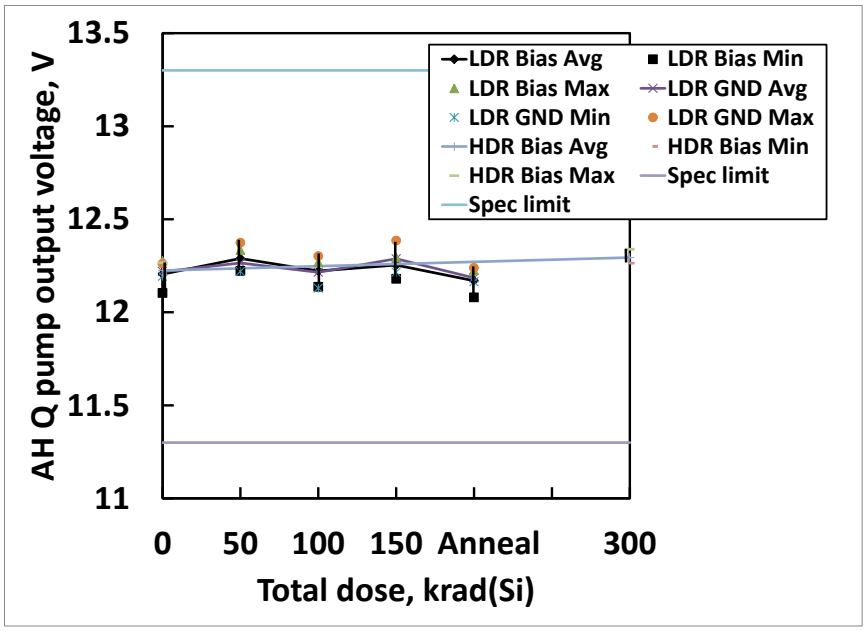

Fig. 10: HS-4080AEH A charge pump output voltage as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100ºC for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limits are 11.3V to 13.3V. (131)

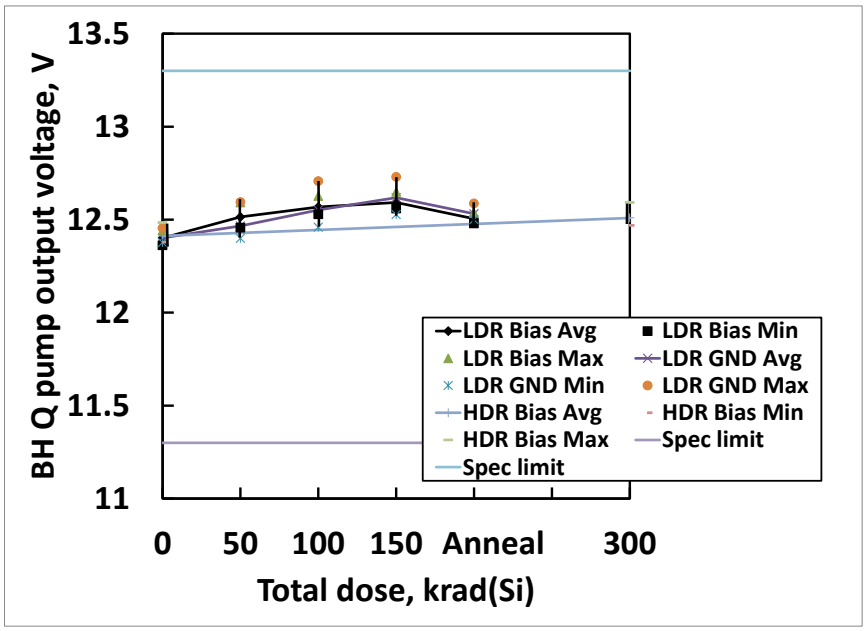

Fig. 11: HS-4080AEH B charge pump output voltage as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100ºC for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limits are 11.3V to 13.3V. (130)

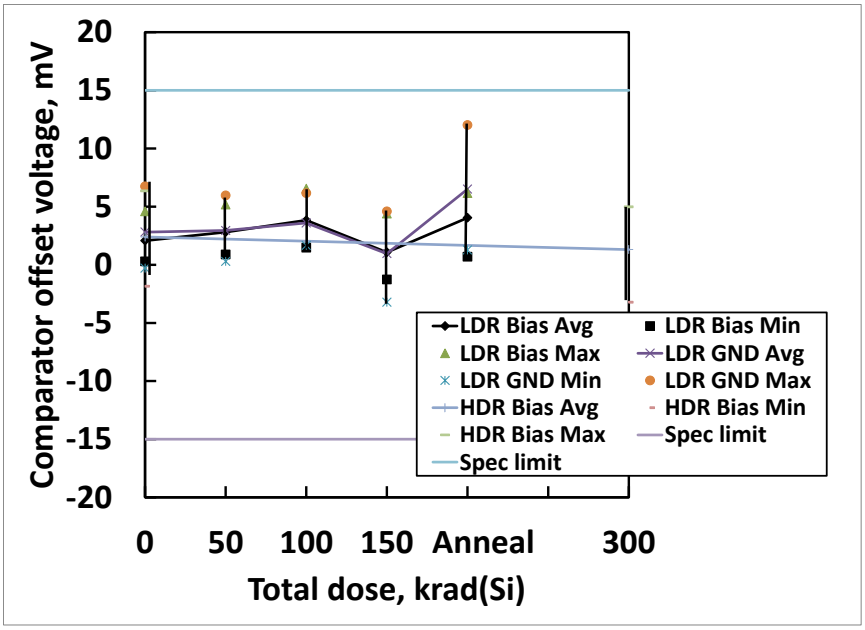

Fig. 12: HS-4080AEH comparator offset voltage as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100ºC for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limits are -15.0mV to +15.0mV. (155)

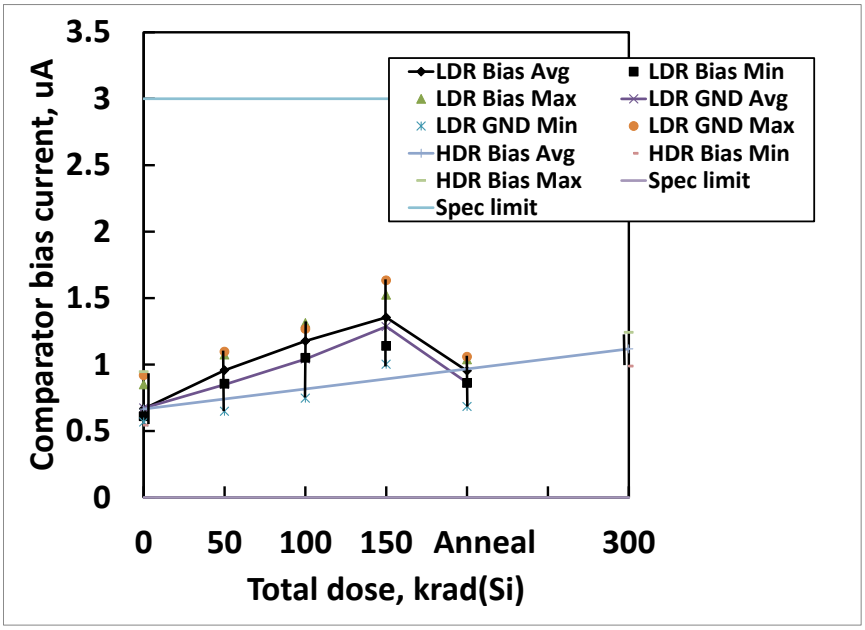

Fig. 13: HS-4080AEH comparator input bias current as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100ºC for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 3.0uA maximum. (156)

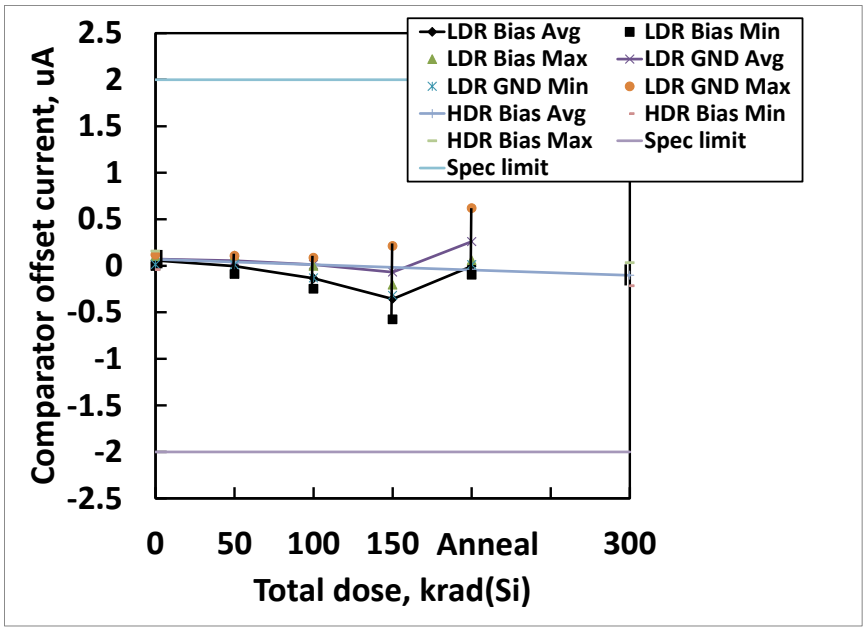

Fig. 14: HS-4080AEH comparator offset current as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limits are -2.0uA to +2.0uA. (157)

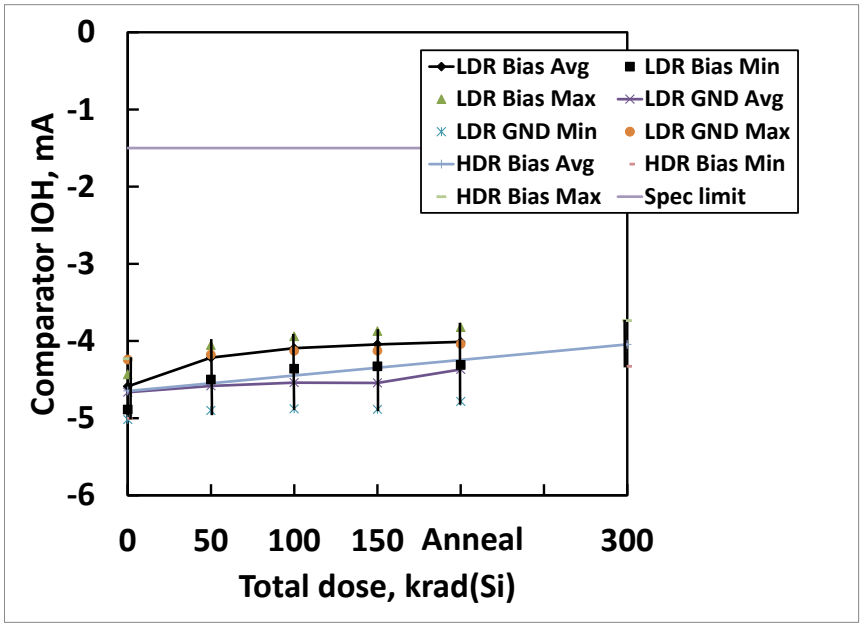

Fig. 15: HS-4080AEH comparator output HIGH current at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is -1.5mA minimum. (160)

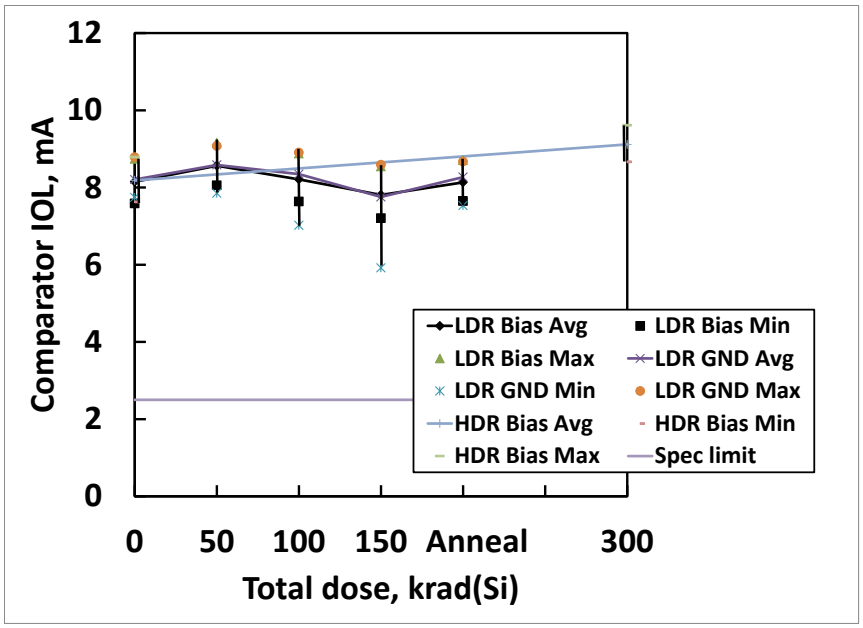

Fig. 16: HS-4080AEH comparator LOW input current as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 2.5mA minimum. (161)

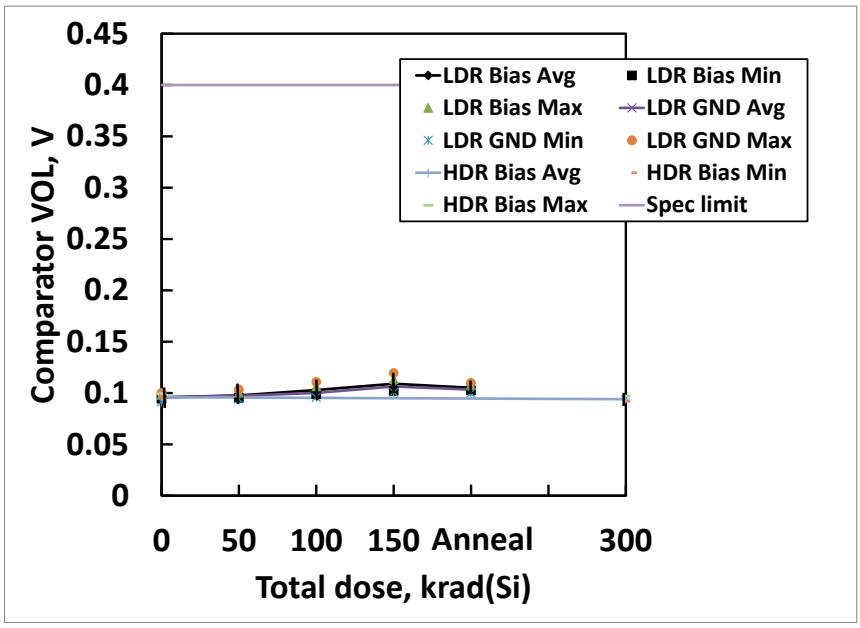

Fig. 17: HS-4080AEH comparator output LOW voltage as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 400.0mV maximum. (162)

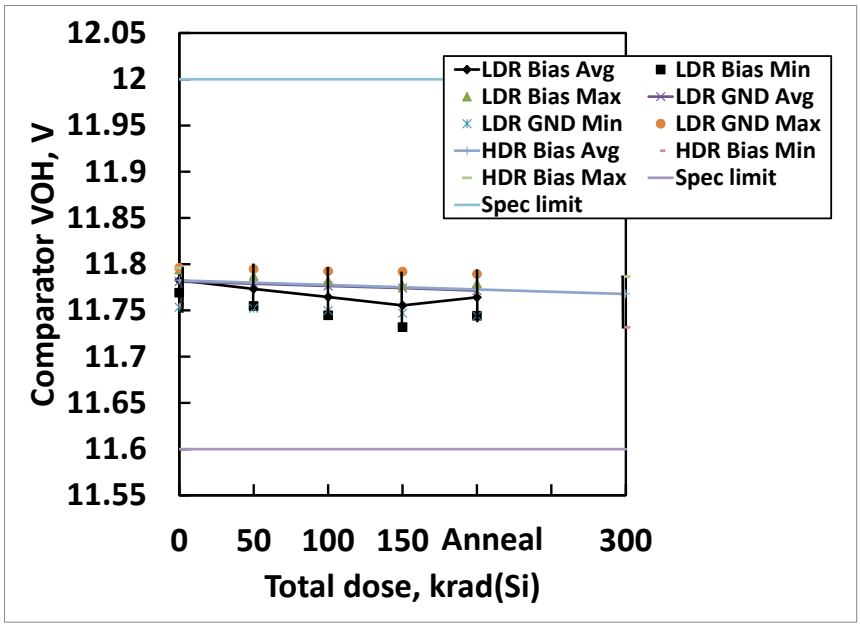

Fig. 18: HS-4080AEH comparator output HIGH voltage as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100ºC for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limits are 11.6V to 12.0V. (163)

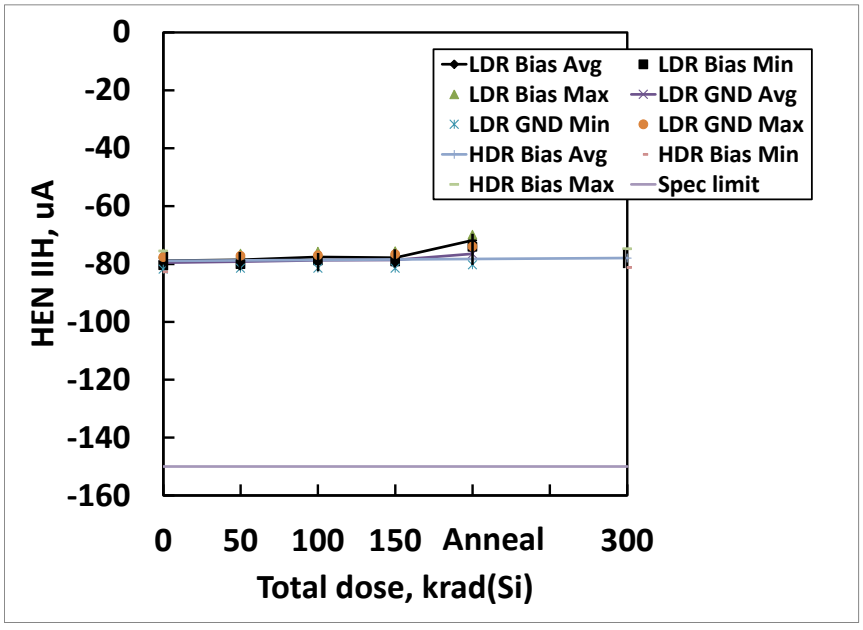

Figure 19: 120 HS-4080AEH high side enable (HEN) pin HIGH input current as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100ºC for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is -150.0uA maximum. (120)

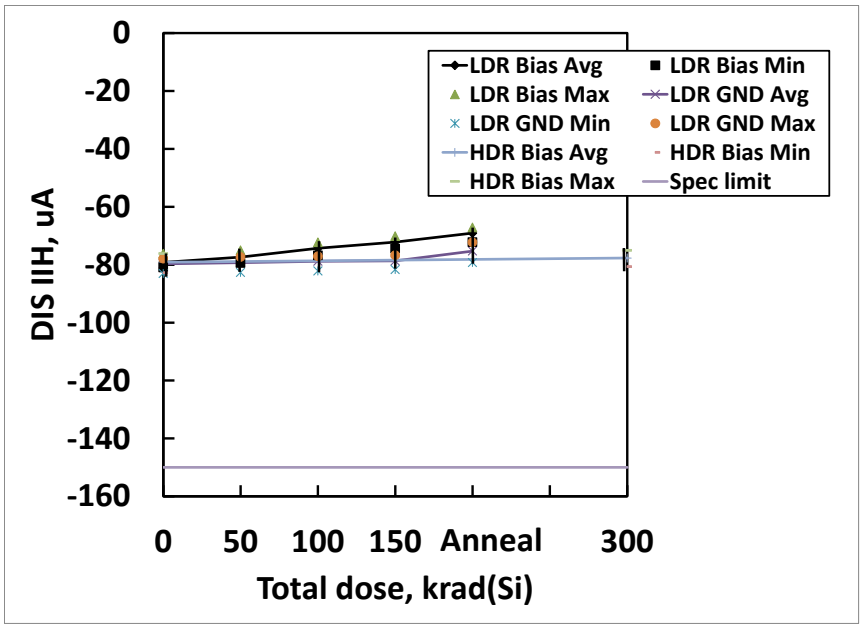

Fig. 20: HS-4080AEH disable (DIS) pin HIGH input current as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is -150.0uA maximum. (121)

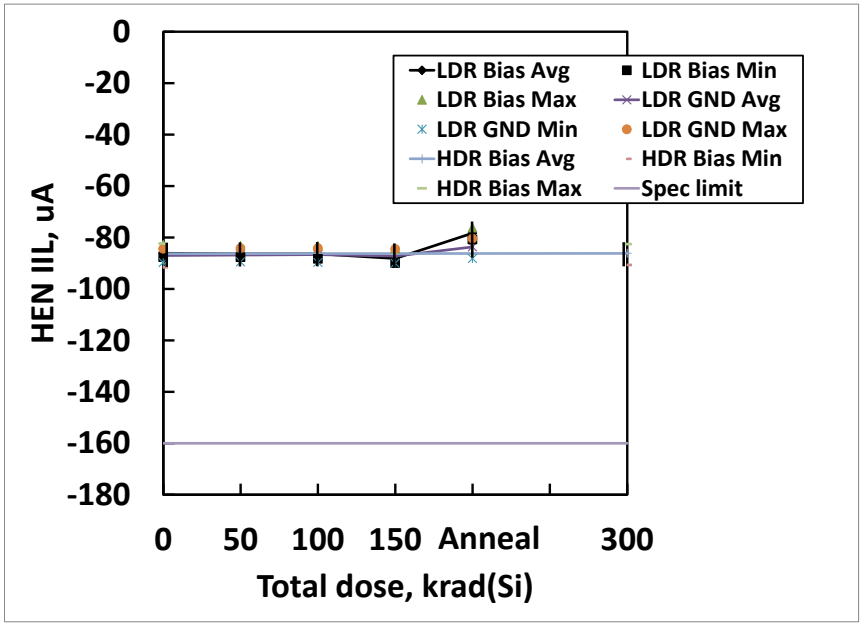

Fig. 21: HS-4080AEH high side enable (HEN) pin LOW input current as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is -160.0uA maximum. (122)

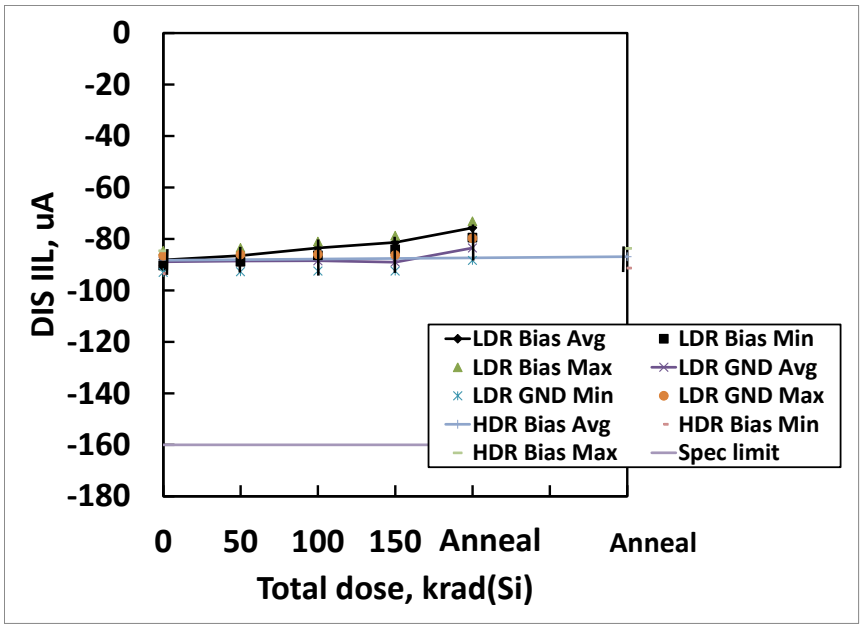

Fig. 22: HS-4080AEH disable (DIS) pin LOW input current as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is -160.0uA maximum. (123)

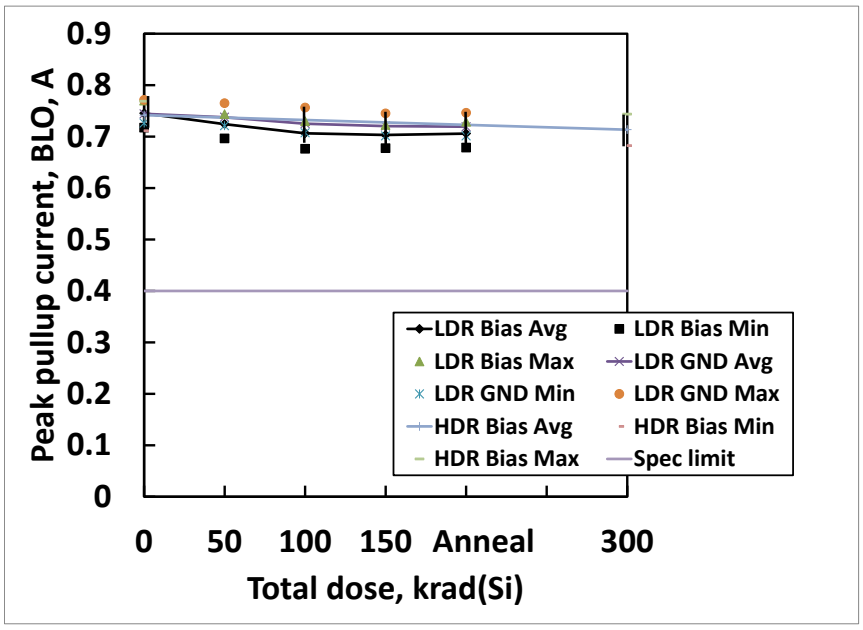

Fig. 23: HS-4080AEH B low side output peak pullup current as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 400.0mA minimum. The B high side, A low side and A high side pullup current responses (not shown) were closely similar. (133)

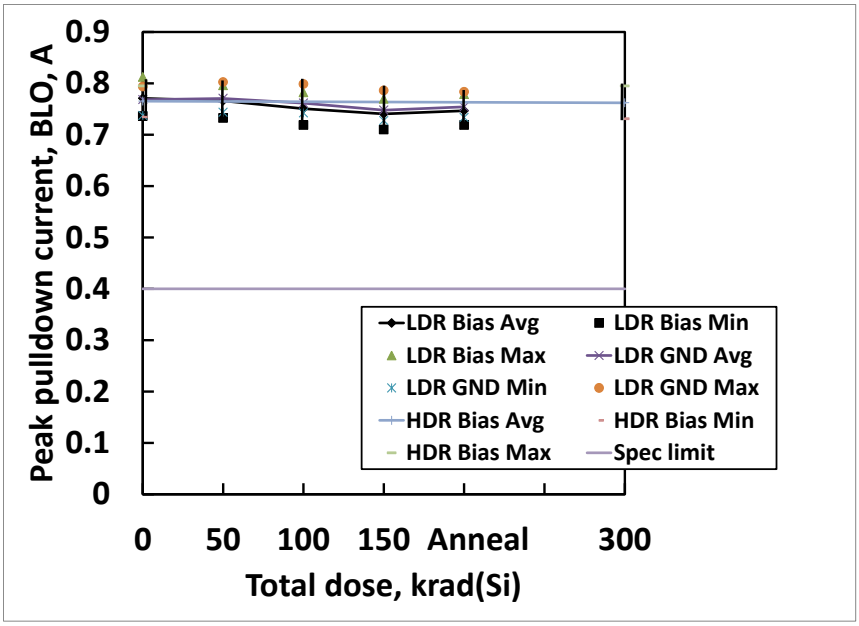

Fig. 24: HS-4080AEH B low side output peak pulldown current as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 400.0mA minimum. The B high side, A low side and A high side pulldown current responses (not shown) were closely similar. (135)

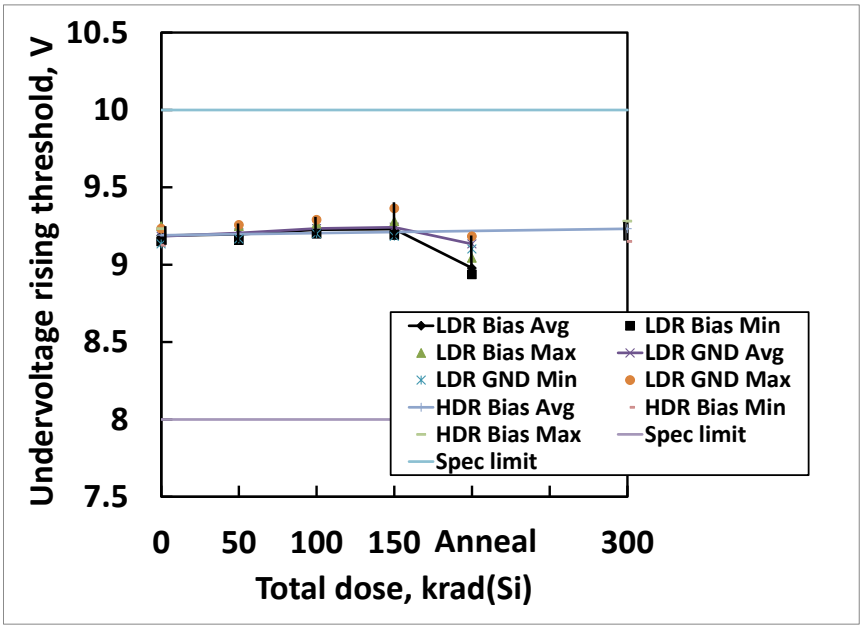

Fig. 25: HS-4080AEH undervoltage rising threshold voltage as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limits are 8.0V to 10.0V. (150)

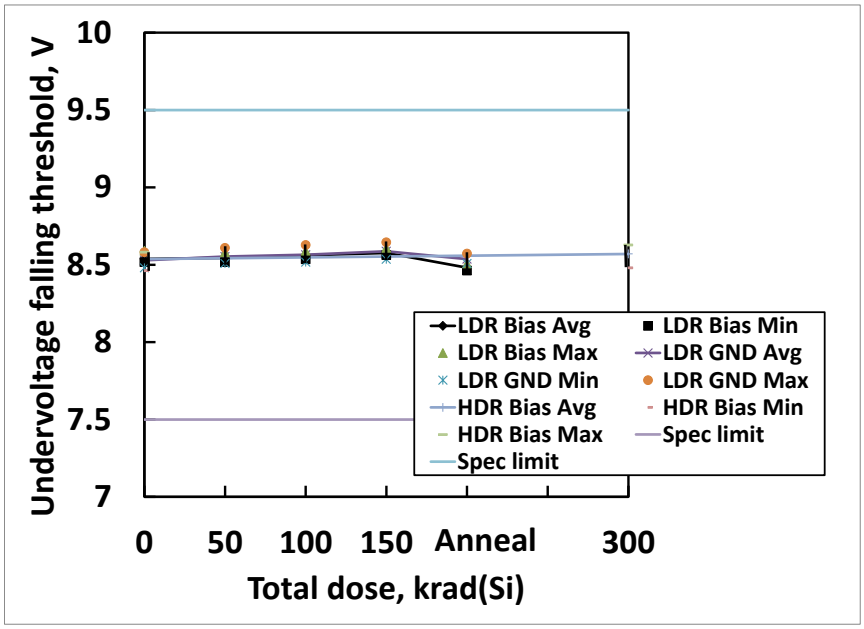

Fig. 26: HS-4080AEH undervoltage falling threshold voltage as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limits are 7.5V to 9.5V. (151)

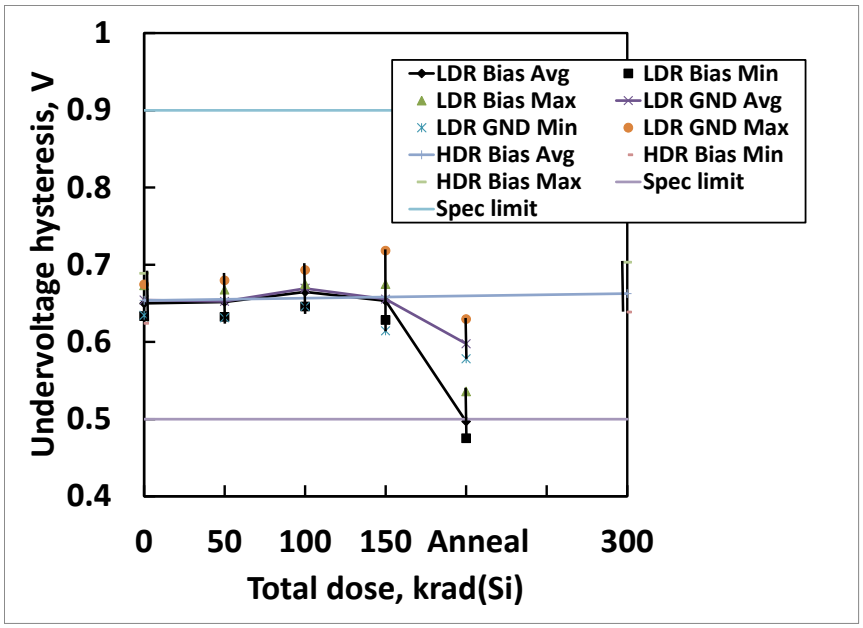

Fig. 27: HS-4080AEH undervoltage hysteresis voltage as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limits are 0.5V to 0.9V. (152)

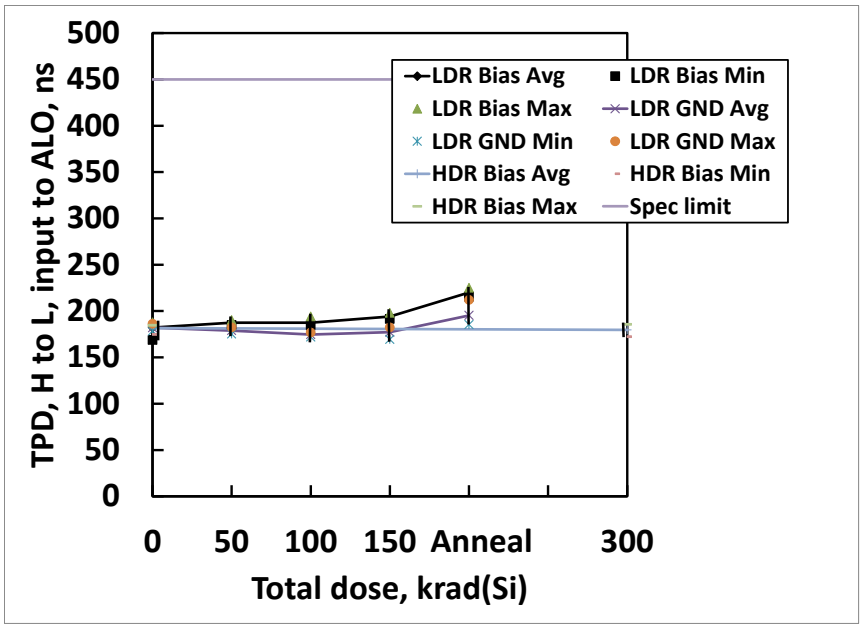

Fig. 28: HS-4080AEH input to A low side output high to low propagation delay as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 450ns maximum. The input to A high side, B low side and B high side high to low delay responses (not shown) were closely similar. (201)

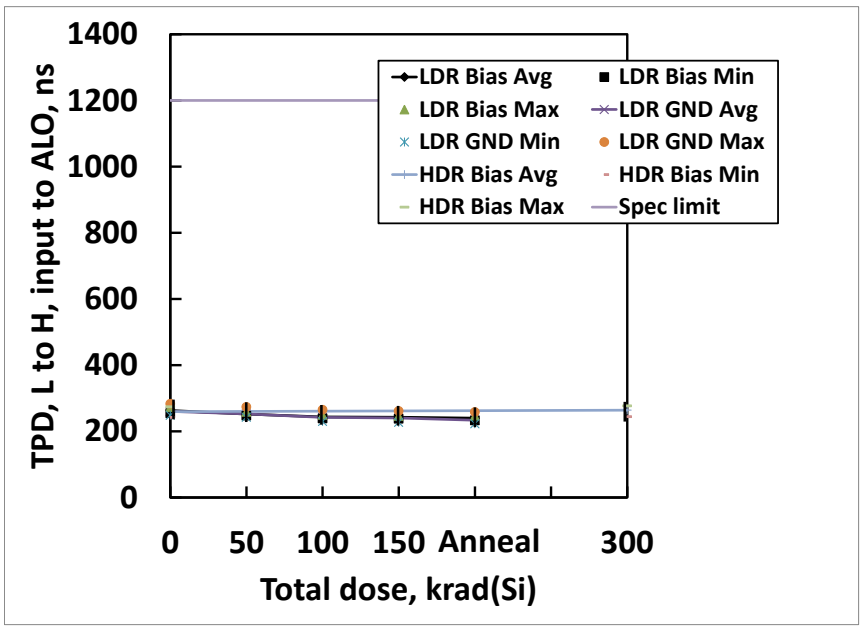

Fig. 29: HS-4080AEH input to A low side output low to high propagation delay as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 1200ns maximum. The input to A high side, B low side and B high side low to high delay responses (not shown) were closely similar. (200)

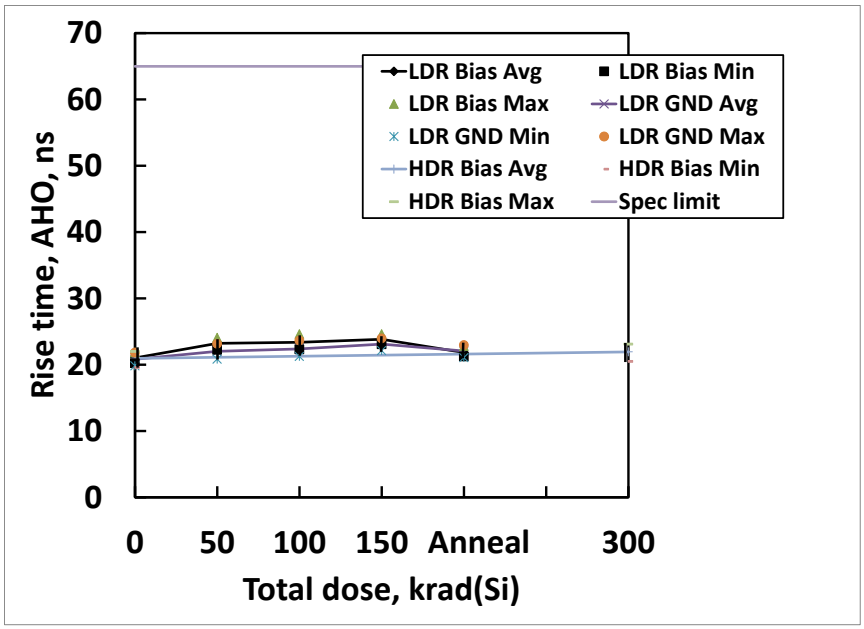

Fig. 30: HS-4080AEH A high side output rise time as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 65ns maximum. The A low side, B high side and B low side rise time responses (not shown) were closely similar. (216)

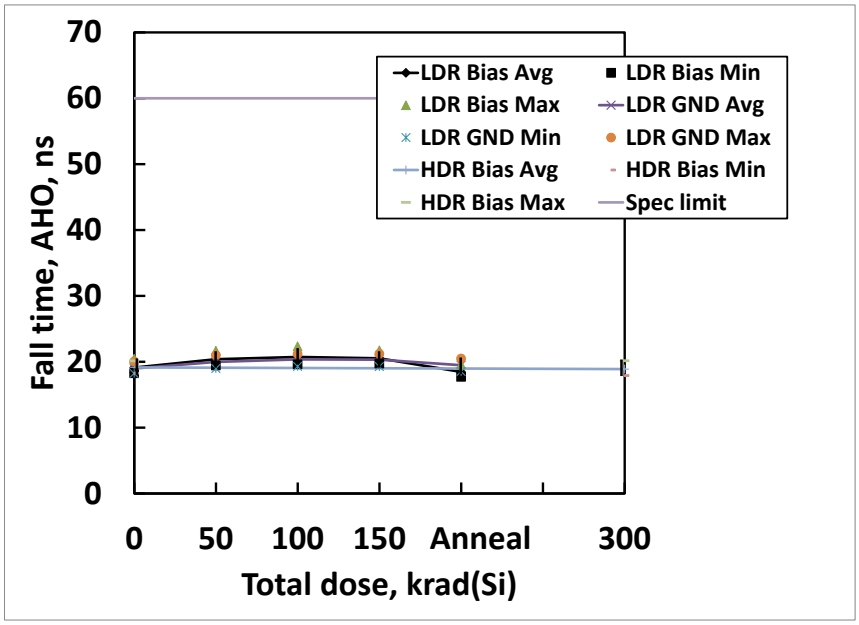

Fig. 31: HS-4080AEH A high side output fall time as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 60ns maximum. The A low side, B high side and B low side fall time responses (not shown) were closely similar. (217)

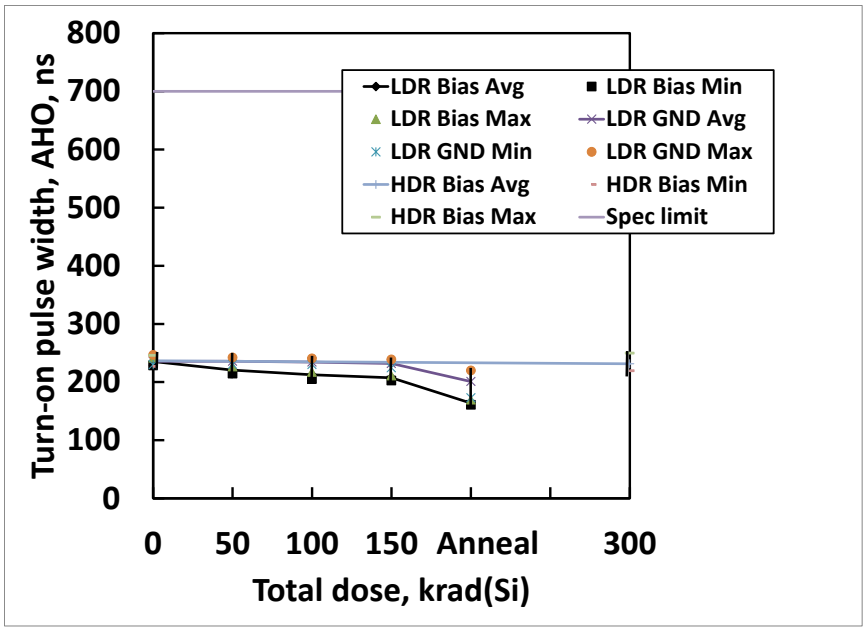

Fig. 32: HS-4080AEH A high side turnon input pulse width as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 700ns maximum. (230)

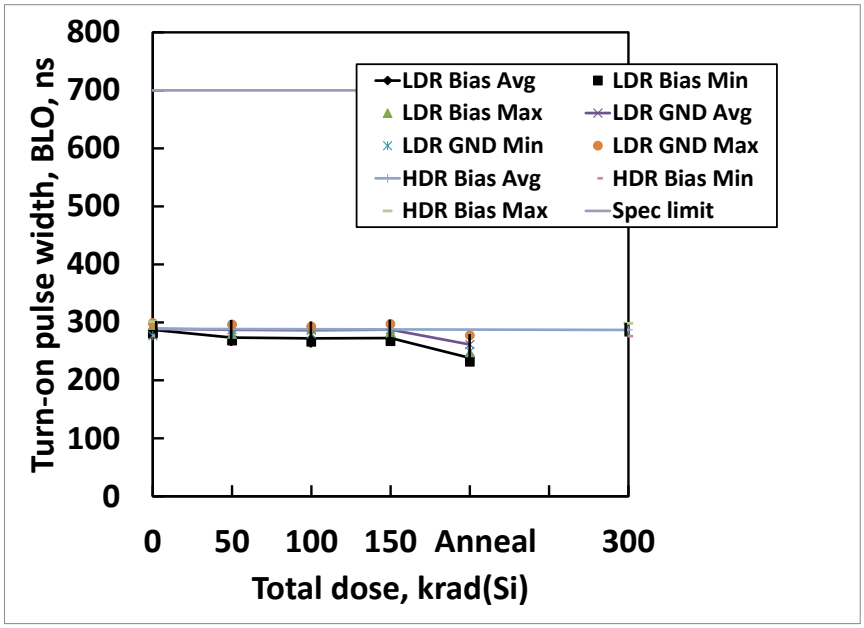

Fig. 33: HS-4080AEH B low side turnon input pulse width as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 700ns maximum. (232)

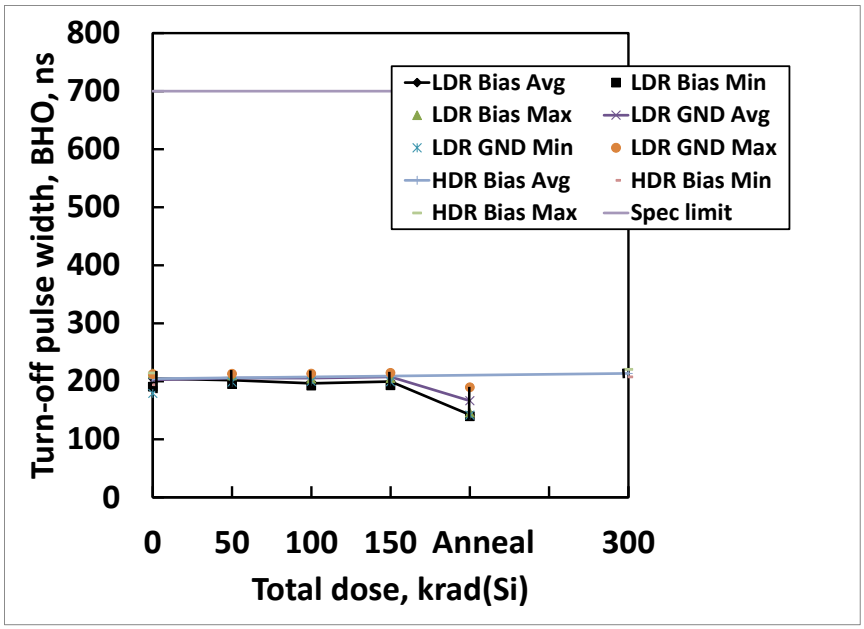

Fig. 34: HS-4080AEH B high side turnoff input pulse width as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 700ns maximum. (231)

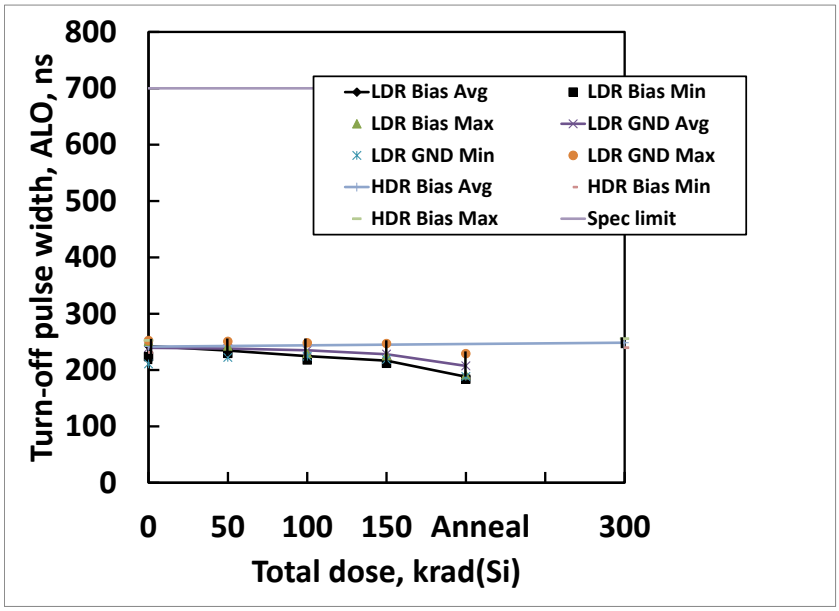

Fig. 35: HS-4080AEH A low side turnoff input pulse width as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 700ns maximum. (233)

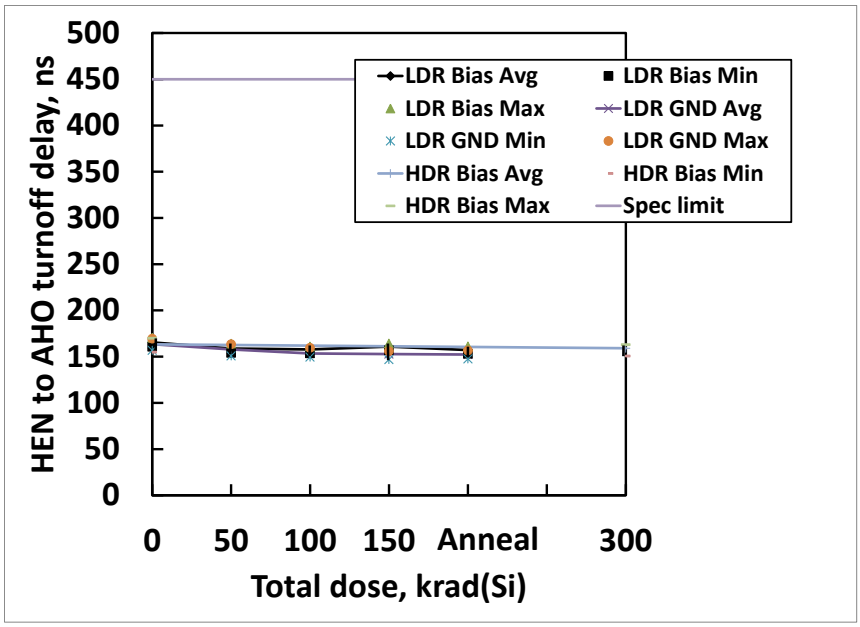

Fig. 36: HS-4080AEH high side enable (HEN) to A high side output turnoff delay as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100ºC for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 450ns maximum. (221)

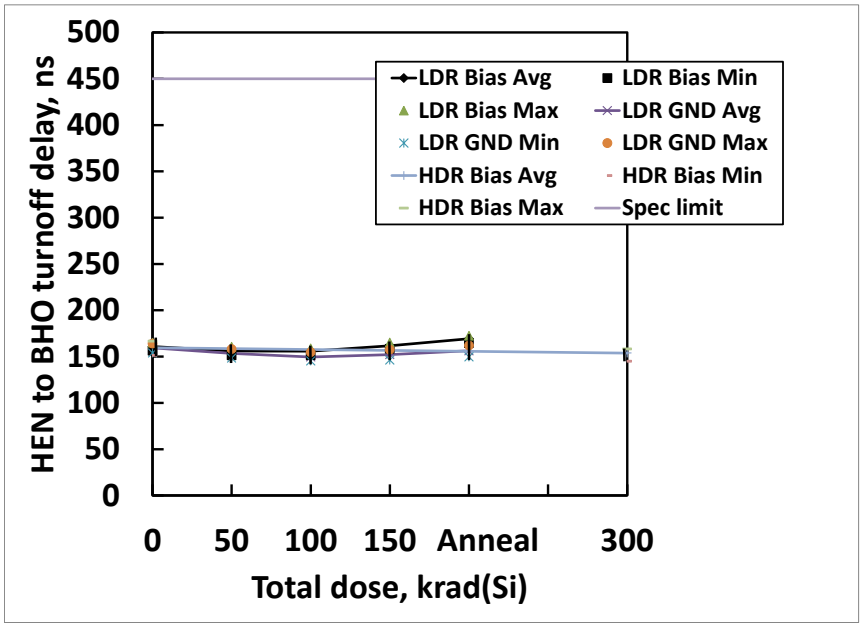

Fig. 37: HS-4080AEH high side enable (HEN) to B high side output turnoff delay as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100ºC for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 450ns maximum. (229)

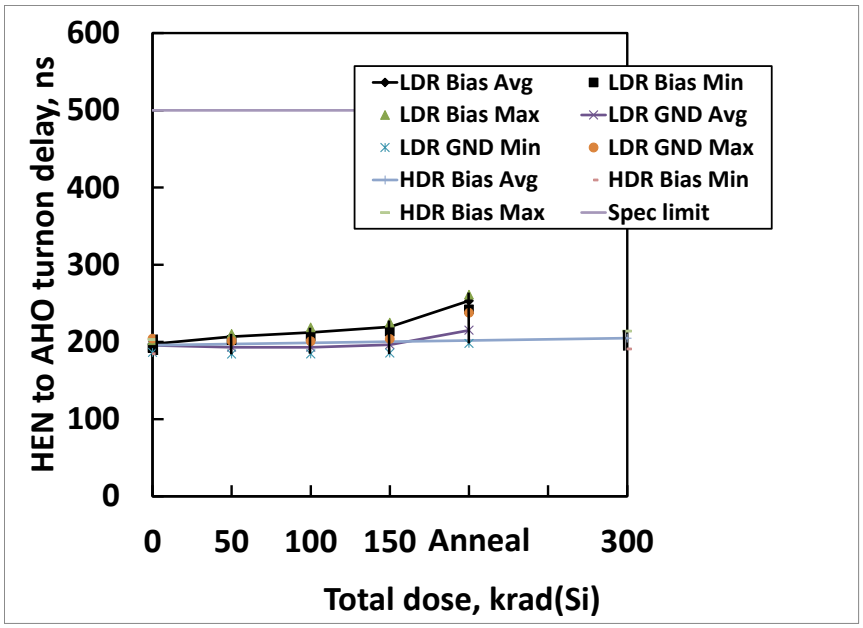

Fig. 38: HS-4080AEH high side enable (HEN) to A high side turnon delay as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 500ns maximum. (220)

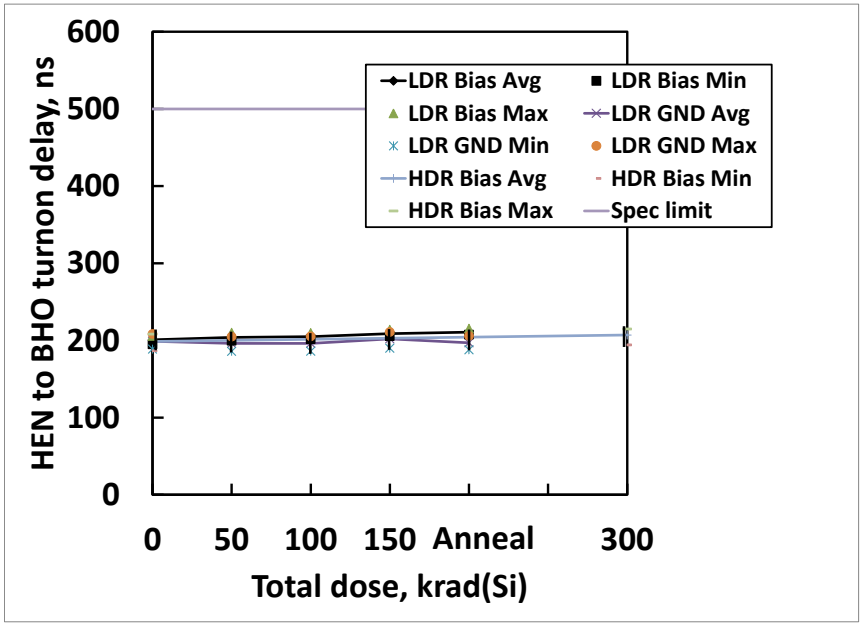

Fig. 39: HS-4080AEH high side enable (HEN) to B high side turnon delay as a function of total dose irradiation at low dose rate for the biased (per Figure 1) and unbiased (all pins grounded) cases and at high dose rate for the biased case. The dose rate was 0.01 rad(Si)/s for low dose rate irradiation and 68 rad(Si)/s for high dose rate irradiation. The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. Sample sizes were 10 at low dose rate under bias, 10 at low dose rate with all pins grounded and 20 samples at high dose rate under bias. The SMD post-irradiation specification limit is 500ns maximum. (228)

6: Discussion and conclusion

6.1 Discussion

This document reports the results of low and high dose rate testing of the HS-4080AEH full bridge N-channel power MOSFET driver. Samples were irradiated under bias and with all pins grounded at low dose rate (0.01 rad(Si)/s) and under bias at high dose rate (68 rad(Si)/s). The low dose rate irradiations were followed by a biased anneal at 100°C for 168 hours. The downpoints and attributes data for each test are given in Table 1, followed by curves of interest (5.2, figures 2 through 39). We will discuss each of the figures separately, grouped by parameter. This is a full bridge driver (sometimes called an H bridge driver) that has two halves, which we will call the A and B sides.

The lower gate drive and upper gate drive circuitry has separate supply pins, here called VDD (lower gates) and VCC (upper gates). Figs. 2 through 5 show the total dose response of the quiescent and operating currents for these pins. Little change was observed, and the low and high dose rate results were closely similar.

The high side bootstrap supply for the A and B sides (AHB and BHB) also has a separate pin for each side, and Figs. 6 through 9 show the quiescent (Figs. 6 and 8) and operating (Figs. 7 and 9) currents as a function of total dose. The operating current showed excellent stability and no dose rate sensitivity, but the quiescent current showed significant increase at low dose rate, both for the biased and grounded cases. The range of the parameter remained stable, but the low end of the range was close to the -15.0µA maximum. The parameter also showed a pronounced recovery over the high temperature post-irradiation anneal.

The part also features two charge pumps, which generate a gate bias voltage for the upper drivers. The charge pump output voltage (Figs. 10 and 11) was stable at low and high dose rate and showed only minor annealing response.

The input stage of the part uses a comparator. The comparator input offset voltage (Fig. 12) showed good stability and evidenced no dose rate sensitivity, but showed a broadening of the range after anneal. The comparator input bias current (Fig. 13) showed a gradual increase over total dose, with some dose rate sensitivity and a recovery over the post low dose rate anneal. The input offset current (Fig. 14) showed similar behavior as would be expected. The output HIGH and LOW currents (Figs. 15 and 16) and the output HIGH and LOW voltages (Figs. 17 and 18) all showed good stability.

There are two enable pins: the high side enable (HEN) and a chip disable function (DIS) that pulls all four output LOW when presented with a HIGH logic state. Figs. 19 through 22 show the HEN and DIS HIGH and LOW input currents, which were stable but showed a slight anneal recovery response.

As this part is designed to drive power MOSFET devices with substantial gate capacitance, the output drive current is a key parameter. We monitored both the pullup (sourcing) and pulldown (sinking) output current for each of the four outputs. These parameters showed a very closely similar response, with a slight (-5%) degradation over irradiation and no dose rate sensitivity. In the interest of saving space we have plotted only two (of eight) responses: the B low side pullup current (Fig. 23) and the B low side pulldown current (Fig. 24).

The part features undervoltage protection, and Figs. 25, 26 and 27 plot the UV rising threshold, the UV falling threshold and the UV hysteresis. The rising and falling thresholds (Figs. 25 and 26) showed good stability and no dose rate effects, but the UV hysteresis (Fig. 27) response showed a pronounced anneal response after showing good stability over irradiation. The post biased irradiation samples were at the 0.5V lower limit after anneal. These annealing responses disagree with conventional total dose testing wisdom. First, post-irradiation annealing is assumed to have an effect in CMOS devices only, and the HS-4080AEH is a BiCMOS design with many bipolar devices in most of its functional blocks. Also, anneals are assumed to lead to recovery of the affected parameter rather than to further degradation. Finally, anneals following low dose rate irradiation are assumed to be unnecessary as they will not produce any parametric change. These unconventional responses have been observed in RSG designs before, but a detailed understanding of the

physics involved will likely require more testing, with anneals after intermediate downpoints; this drives up the sample size requirements drastically.

We now come to the switching performance of the part, starting with the propagation delays from the input to each of the four outputs and looking at both the HIGH to LOW and LOW to HIGH responses. As in the output drive currents, these responses were closely similar and showed excellent stability and no dose rate or bias effects. In the interest of saving space we show only two (of eight) responses, the input to A low side HIGH to LOW delay (Fig. 28) and the input to A low side LOW to HIGH delay (Fig. 29).

The rise and fall times of each of the four outputs showed similar excellent stability over total dose and no dose rate or bias effects, and we show the A high side rise time (Fig. 30) and fall time (Fig. 31).

The input pulse width required to turn on any one of the four outputs is represented by the turnon input pulse width. Figs. 32 through 35 show the response of the parameter for the A high side, B low side, B high side and A low side outputs. The parameter showed excellent stability and no dose rate or bias sensitivity, with some shift following the anneal operation after low dose rate irradiation.

Finally, Figs. 36 through 39 show the high side enable (HEN) turnoff and turnon delay to the A and B side high side outputs. The parameter showed excellent stability and no dose rate sensitivity, with some shift following the anneal operation after low dose rate irradiation.

6.2 Conclusion

The high side bootstrap quiescent supply current (Figs. 6 and 8) showed significant dose rate sensitivity, both for the biased and grounded cases. The range of this parameter remained stable, but the low end of the range was close to the SMD maximum following 150 krad(Si) at low dose rate, biased and unbiased. This represents a 3x overtest over the part's 50 krad(Si) low dose rate specification. The parameter also showed a pronounced recovery over the high temperature post-irradiation anneal. Additionally the comparator input bias current showed a gradual increase over total dose, with some dose rate sensitivity and a recovery over the post low dose rate anneal. Based on this data the HS-4080AEH is considered moderately dose rate sensitive. The part is acceptance tested at both low and high dose rate on a wafer by wafer basis, providing additional hardness assurance.

The undervoltage (UV) hysteresis (Fig. 27) response showed a pronounced anneal response after showing good stability over irradiation. The post biased irradiation samples were at the 0.5V lower limit after anneal. These annealing responses disagree with conventional total dose testing wisdom. First, post-irradiation annealing is assumed to have an effect in CMOS devices only, and the HS-4080AEH is a BiCMOS design. Also, anneals are assumed to lead to recovery of the affected parameter rather than further degradation. Finally, anneals following low dose rate irradiation are assumed to be unnecessary as they will not produce any parametric change. These unconventional responses have been observed in RSG (and other) designs before, but a detailed understanding of the physics involved will likely require more testing, with anneals after intermediate downpoints; this drives up the samples size requirements drastically. Note again that these anneals were performed after a 3X overtest at low dose rate, and the data is presented for information only.

To summarize, the HS-4080AEH showed good performance over low and high dose rate irradiation. All samples passed the post-irradiation after the specified levels of 300 krad(Si) at high dose rate (50 – 300 rad(Si)/s) and of 50 krad(Si) at low dose rate (0.01 rad(Si)/s). Rejects were only encountered after biased low dose rate irradiation to 150 krad(Si), which represents a 3x overtest with respect to the rated 50krad(Si), and a subsequent high temperature biased anneal. The part is considered moderately dose rate sensitive, but is acceptance tested on a wafer by wafer basis at both low and high dose rate, insuring hardness to the specified level at both dose rates. We saw no bias sensitivity in the low dose rate results.

7: Appendices

7.1: Reported parameters, their post-irradiation limits and figure numbers for monitored parameters. Not all plots are shown in this report, see the Discussion section.

Fig.	Parameter	Limit, low	Limit, high	Units
2	VDD quiescent current	-	13	mA
3	VDD operating current	-	15	mA
4	VCC quiescent current	-	160	µA
5	VCC operating current	-	7	mA
6	A high side bootstrap supply quiescent current	-	-15.0	µA
7	A high side bootstrap supply operating current	-	-15.0	µA
8	B high side bootstrap supply quiescent current	-	-15.0	µA
9	B high side bootstrap supply operating current	-	-15.0	µA
10	A charge pump output voltage	11.3	13.3	V
11	B charge pump output voltage	11.3	13.3	V
12	Input comparator offset voltage	-15.0	15.0	mV
13	Input comparator bias current	-	3.0	µA
14	Input comparator offset current	-2.0	2.0	µA
15	Input comparator HIGH level output current	-1.5	-	mA
16	Input comparator LOW level output current	2.5	-	mA
17	Input comparator LOW level output voltage	-	0.4	V
18	Input comparator HIGH level output voltage	11.6	12.0	V
19	High side enable (HEN) pin HIGH input current	-150.0	-	µA
20	Disable (DIS) pin HIGH input current	-150.0	-	µA
21	High side enable (HEN) pin LOW input current	-160.0	-	µA
22	Disable (DIS) pin LOW input current	-160.0	-	µA
23	B low side output peak pullup current	400.0	-	mA
	A low side output peak pullup current	400.0	-	mA
	B high side output peak pullup current	400.0	-	mA
	A high side output peak pullup current	400.0	-	mA
24	B low side output peak pulldown current	400.0	-	mA
	A low side output peak pulldown current	400.0	-	mA
	B high side output peak pulldown current	400.0	-	mA
	A high side output peak pulldown current	400.0	-	mA
25	Undervoltage rising threshold voltage	8.0	10.0	V
26	Undervoltage falling threshold voltage	7.5	8.5	V
27	Undervoltage hysteresis voltage	0.5	0.9	V
28	Input to A low side output high to low propagation delay	-	450.0	ns
	Input to A high side output high to low propagation delay	-	1200.0	ns
	Input to B low side output high to low propagation delay	-	1200.0	ns
	Input to B high side output high to low propagation delay	-	500.0	ns
	Input to A low side output low to high propagation delay	-	650.0	ns
	Input to A high side output low to high propagation delay	-	1200.0	ns

29	Input to A low side output low to high propagation delay	-	1200.0	ns
	Input to B high side output low to high propagation delay	-	600.0	ns
	A low side output rise time	-	65.0	ns
	B low side output rise time	-	65.0	ns
30	A high side output rise time	-	65.0	ns
	B high side output rise time	-	65.0	ns
	A low side output fall time	-	60.0	ns
	B low side output fall time	-	60.0	ns
31	A high side output fall time	-	60.0	ns
	B high side output fall time	-	60.0	ns
32	A high side turnon input pulse width	-	700.0	ns
33	B low side turnon input pulse width	-	700.0	ns
34	B high side turnon input pulse width	-	700.0	ns
35	A low side turnon input pulse width	-	700.0	ns
36	High side enable (HEN) to A high side turnoff delay	-	450.0	ns
37	High side enable (HEN) to B high side turnoff delay	-	450.0	ns
38	High side enable (HEN) to A high side turnon delay	-	500.0	ns
39	High side enable (HEN) to B high side turnon delay	-	500.0	ns

8: Document revision history

Rev	Date	Pages	Comments
0	16 April 2014	All	Original issue