Final report

Total dose testing of the HS1840ARH 16-channel analog multiplexer

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Revision 0
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1. Introduction

This report provides interim results of a low and high dose rate total dose test of the HS1840ARH 16-channel analog multiplexer. The test was conducted in order to determine the sensitivity of the part to the total dose environment and to determine if any dose rate sensitivity exists.

2. Reference Documents

MIL-STD-883G test method 1019.7
HS1840ARH data sheet, Intersil document FN4355.2
DSCC Standard Microcircuit Drawing (SMD) 5962-95630

3: Part Description

The HS1840ARH is a radiation hardened 16 channel multiplexer constructed using the Intersil Rad-Hard Silicon Gate (RSG) dielectrically isolated process. It is designed to provide high input impedance to the analog source if device power fails (open), or the analog signal voltage exceeds the supply by up to ±35V, regardless of whether the device is powered on or off. This enables predictable operation in redundant or cold-spared applications, since the secondary device can be operated in a standby unpowered mode affording no additional power drain. More significantly, a very high impedance exists between the active and inactive devices preventing any interaction. One of sixteen channel selection is controlled by a 4-bit binary address plus an Enable/Inhibit input which may be used to control the ON/OFF operation of several multiplexers in a system. All inputs have electrostatic discharge protection. The HS1840ARH is processed and screened in full compliance with MIL-PRF-38535 (QML) standards. The device is available in a 28-lead SBDIP and a 28-lead ceramic flatpack.

As there have been two versions of the part a historical note is in order. The forerunner of the HS1840ARH was the HS1840RH. It was built in an early dielectrically isolated metal gate CMOS process. The key to hardening a metal gate process is the gate metal deposition, which must be done using a flash evaporator. In the 1995 time frame this equipment became difficult to maintain due to obsolescence, and the metal gate process was abandoned. As a result the HS1840RH was obsoleted.

The current RSG process was developed in order to continue supplying this very popular part, which was a key function in many space systems, and the HS-1840ARH is designed in that process. As part of the redesign the part gained some functionality made possible by the bipolar devices available in RSG. Accordingly the HS1840ARH design has several bipolar transistors (BJT), while the 1840RH did not; the metal gate process simply did not support them. Bipolar circuit blocks in the HS1840ARH include the on-chip voltage reference, the digital input ESD network and the VDD and VSS ESD nets.

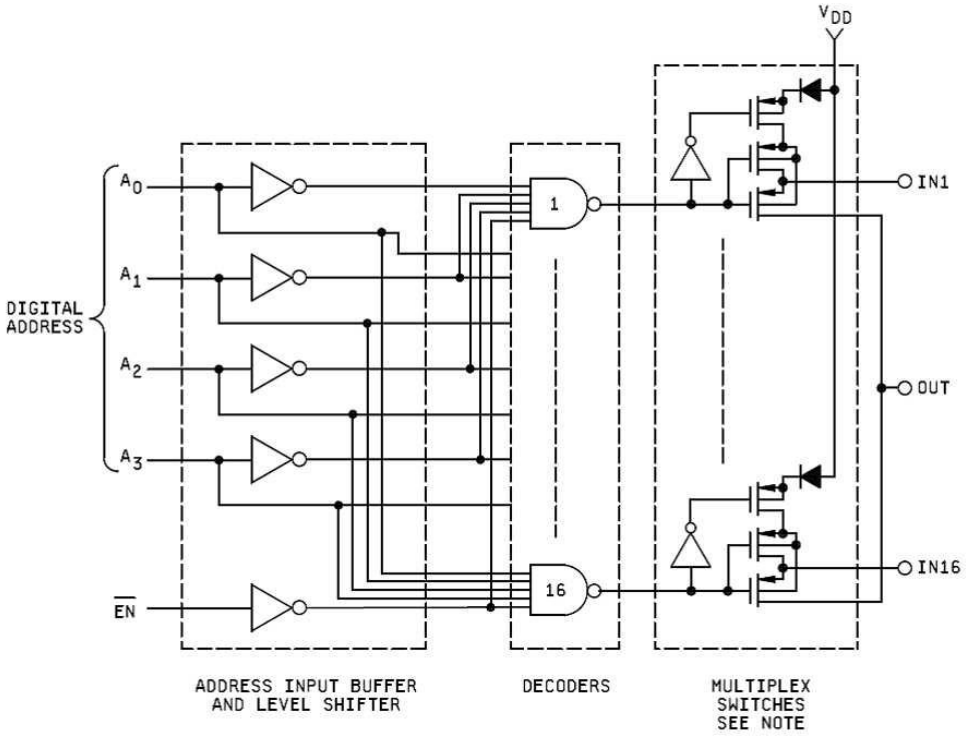

Figure 1: HS1840ARH block diagram.

4: Test Description

4.1 Irradiation Facilities

High dose rate testing was performed using a Gammacell 220 ^{60}Co irradiator located in the Palm Bay, Florida Intersil facility. Low dose rate testing was performed on a subcontract basis at White Sands Missile Range (WSMR) Survivability, Vulnerability and Assessment Directorate (SVAD), White Sands, NM. The high dose rate irradiations were done at 55rd(Si)/s and the low dose rate work was performed at .010rd(Si)/s, both per MIL-STD-883 Method 1019.7. Dosimetry for both tests was performed using Far West Technology radiochromic dosimeters and on-site readout equipment. A PbAl box was used to shield the test fixture and devices under test against low energy secondary gamma radiation.

4.2 Test Fixturing

Figure 2 shows the configuration used for biased irradiation in conformance with Standard Microcircuit Drawing (SMD) 5962-95630.

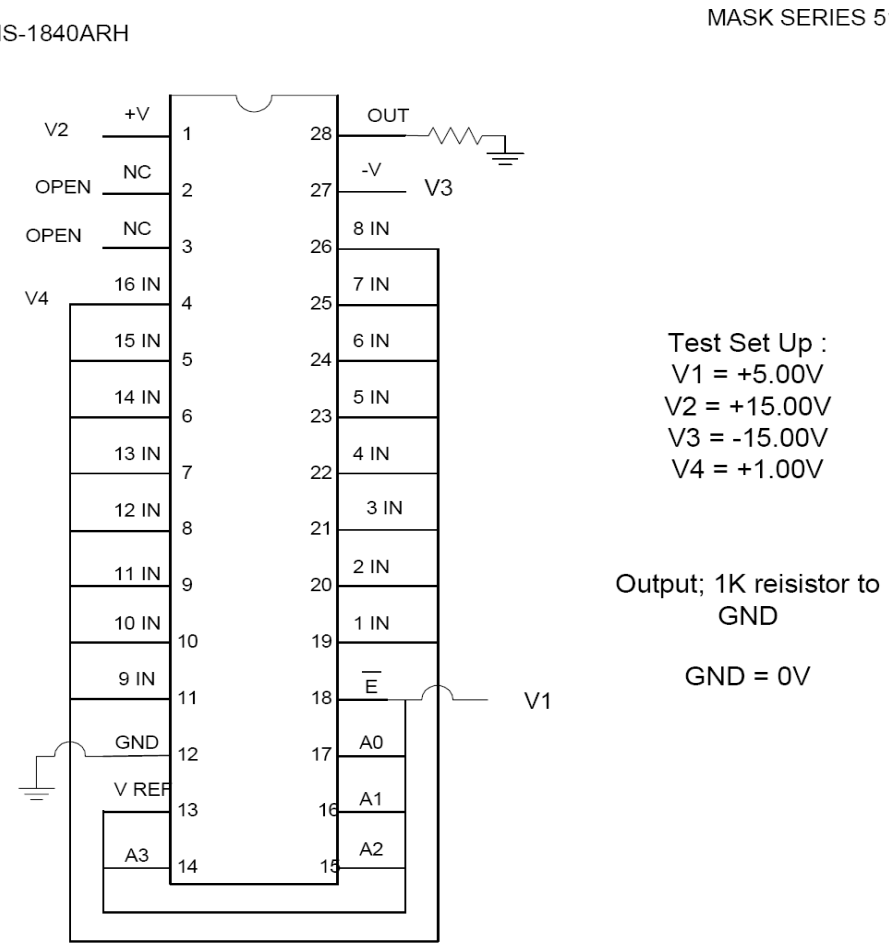

Figure 2: Irradiation bias configuration for the HS1840ARH per Standard Microcircuit Drawing (SMD) 5962-95630.

4.3 Characterization equipment and procedures

All electrical testing was performed outside the irradiator using the production automated test equipment (ATE) with datalogging at each downpoint. Downpoint electrical testing was performed at room temperature. The low dose rate testing at a remote site introduced some challenges, and shipping had to be done in a foam container with a frozen Gelpack™ along with a strip chart temperature recorder in order to remain well within the temperature limits imposed by MIL-STD-883 Test Method 1019.7.

4.4 Experimental matrix

Testing proceeded in accordance with the guidelines of MIL-STD-883 Test Method 1019.7. The experimental matrix consisted of five samples irradiated at high dose rate with all pins grounded, five samples irradiated at high dose rate under bias, five samples irradiated at low dose rate with all pins grounded and five samples irradiated at low dose rate under bias. One control unit was used.

Samples of the HS1-1840ARH-Q were drawn from wafer 15 of production lot DPH8HAC and were packaged in the standard hermetic 28-pin ceramic solder-sealed side brazed dual in-line (DIP) production package. Samples were processed through the standard burnin cycle before irradiation, as required by MIL-STD-883, and were screened to the SMD 5962-95630 limits at room, low and high temperatures.

4.5 Downpoints

Downpoints for low and high dose rate tests were zero, 10krad(Si), 25krad(Si), 50krad(Si), 100krad(Si) and 150krad(Si).

5: Results

5.1 Test results

Testing at both dose rates to 150krad(Si) of the HS1840ARH is complete and showed no reject devices after irradiation to 150krad(Si), screening to the SMD post-irradiation limits.

5.2 Variables data

The plots in Figures 3 through 40 show data at all downpoints. The plots show the median of key parameters as a function of total dose for each of the four irradiation conditions. All parts showed excellent stability over irradiation, with no observed low dose rate sensitivity.

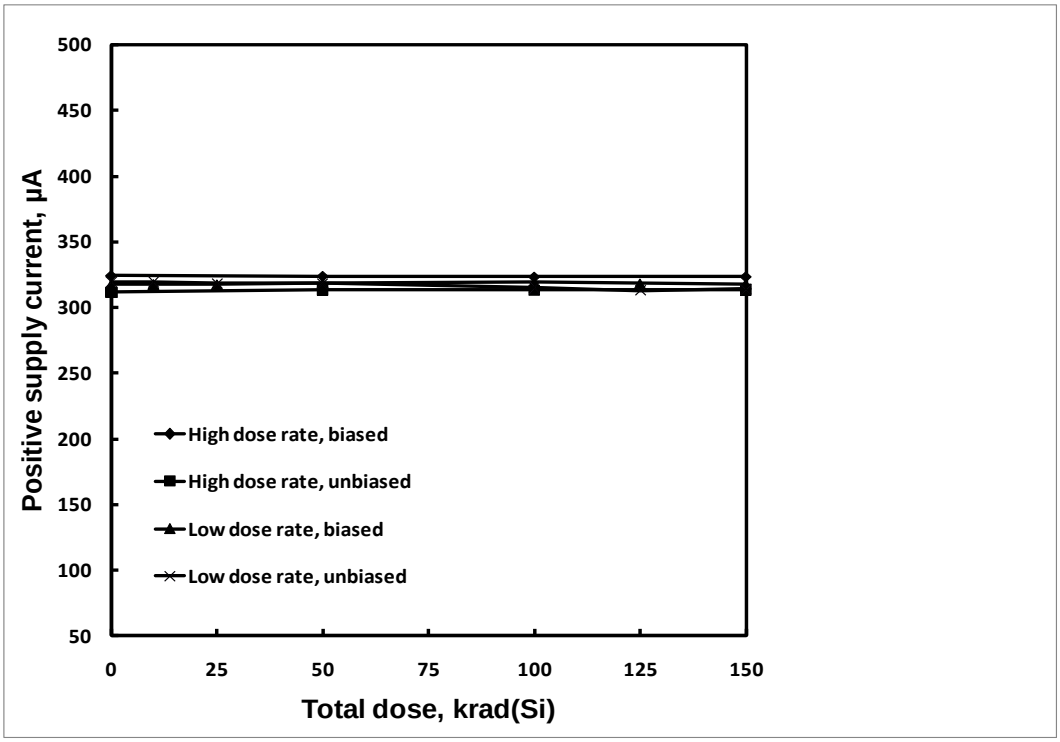

Figure 3: HS1840ARH positive supply current as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Figure 2) cases. The low dose rate was .01rad(Si)/s and the high dose rate was 55rad(Si)/s. Sample size for each cell was 5. The SMD limit is 500µA.

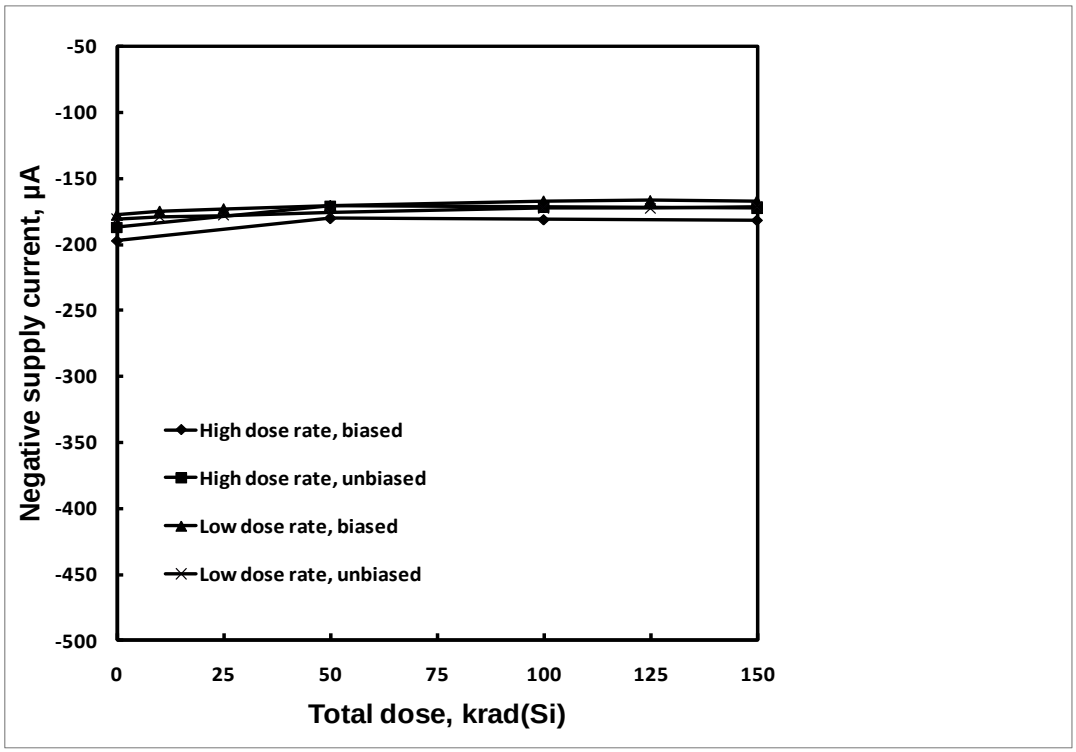

Figure 4: HS1840ARH negative supply current as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The SMD limit is 500µA.

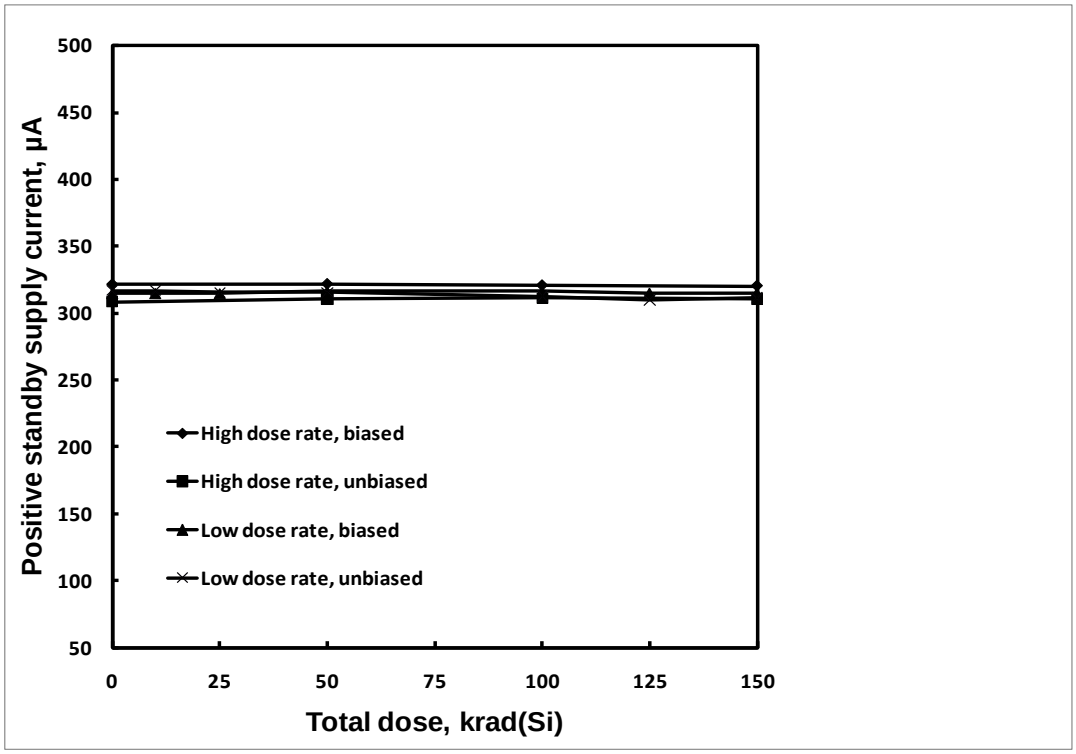

Figure 5: HS1840ARH positive standby current as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 500µA.

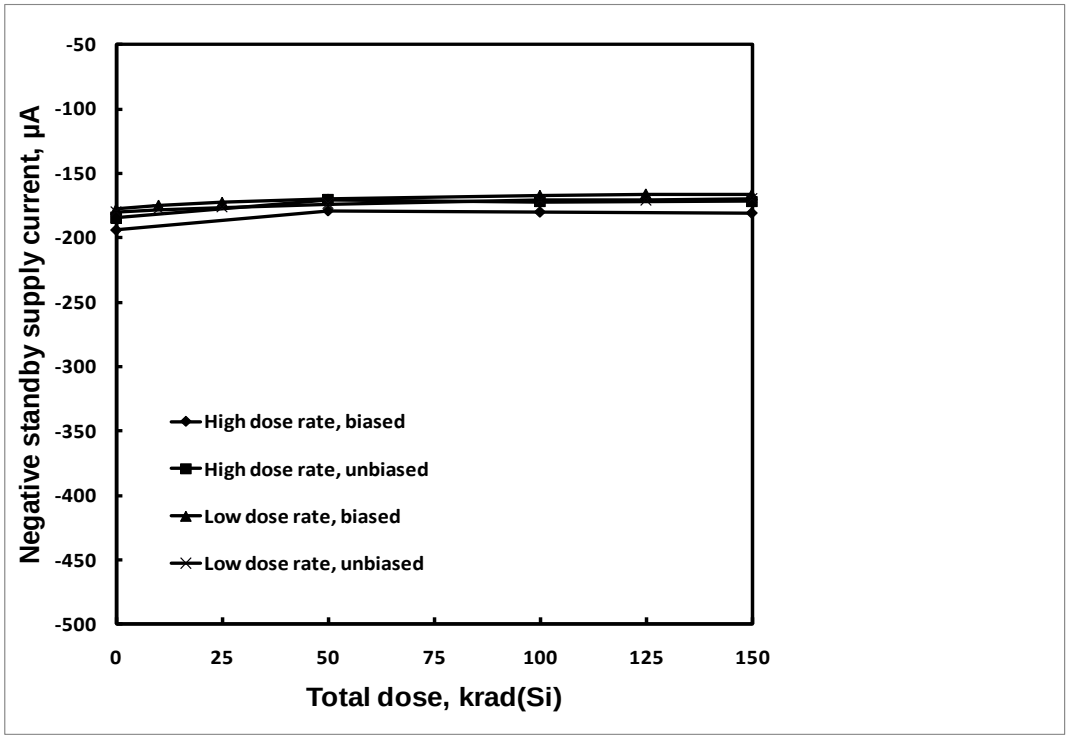

Figure 6: HS1840ARH negative standby current as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 500µA.

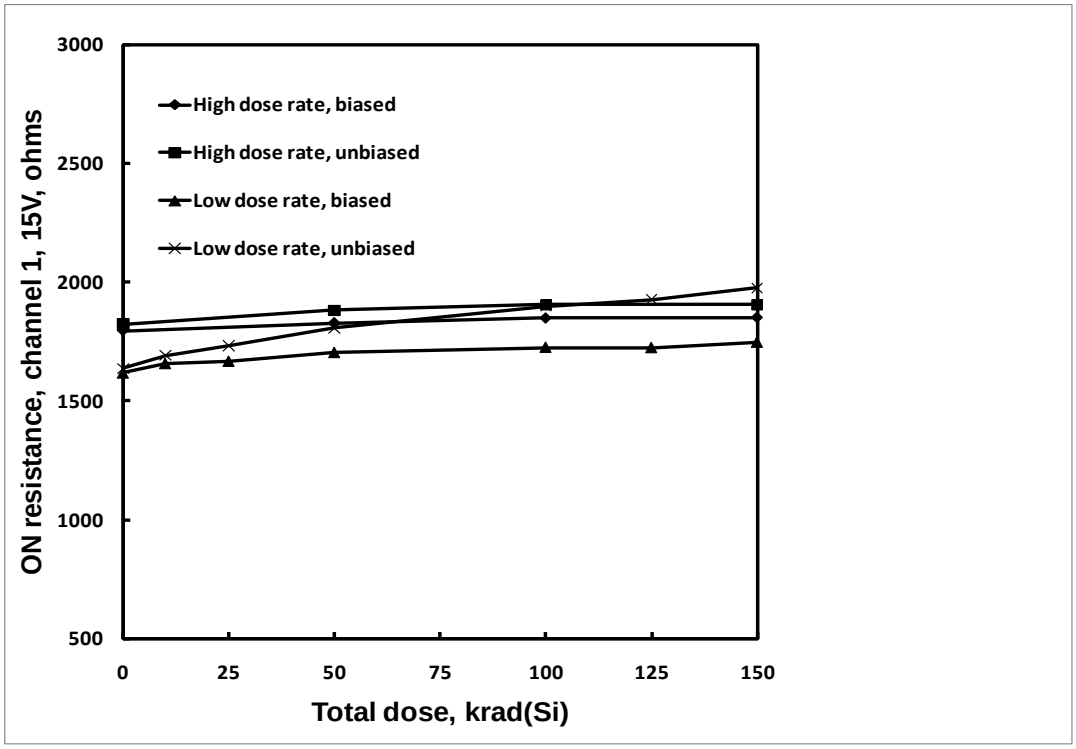

Figure 7: HS1840ARH switch ON resistance (1mA drain current, 15V source voltage, channel 1) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 500-3000 ohms.

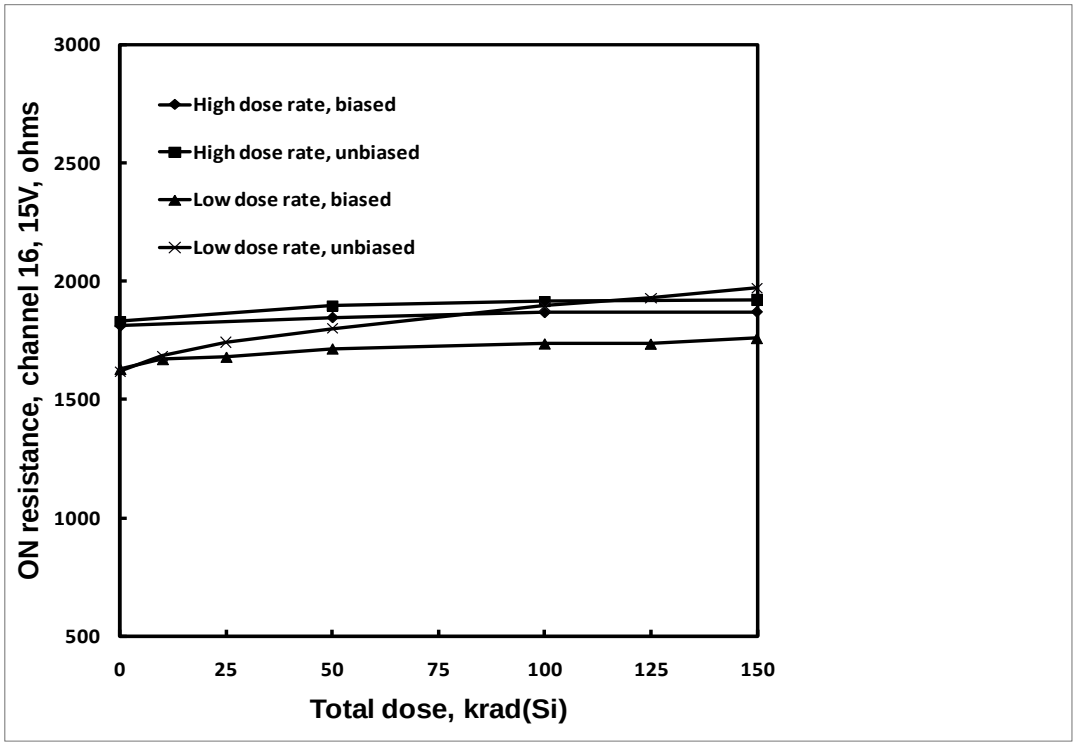

Figure 8: HS1840ARH switch ON resistance (1mA drain current, 15V source voltage, channel 16) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 500-3000 ohms.

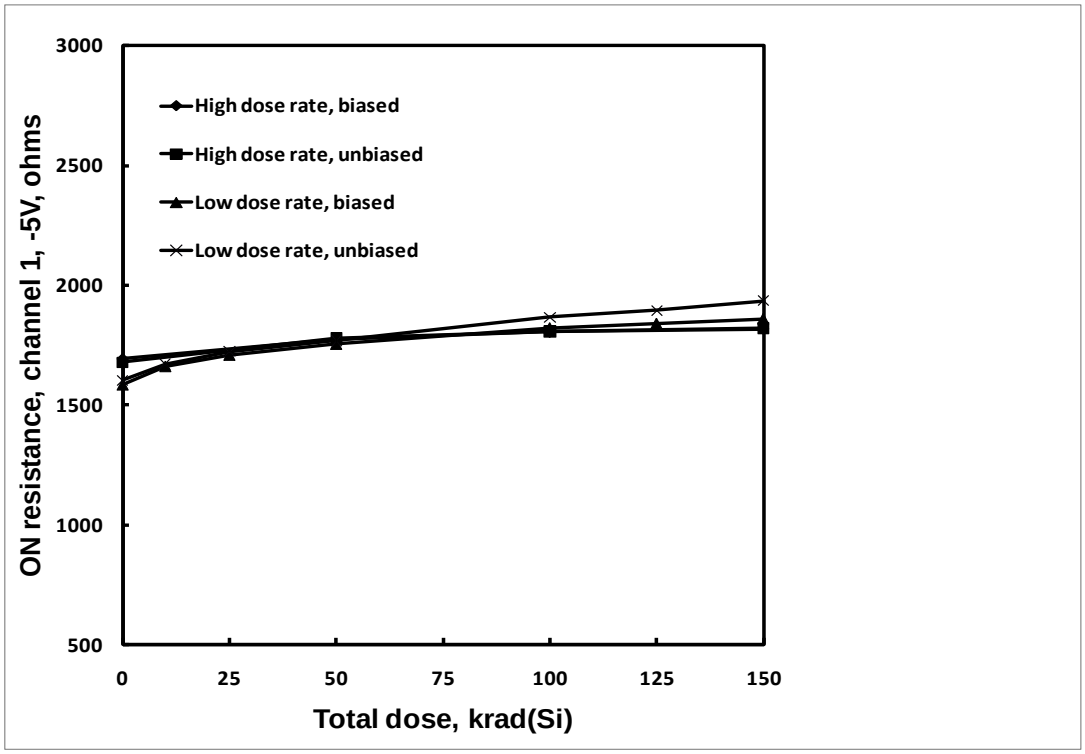

Figure 9: HS1840ARH switch ON resistance (1mA drain current, -5V source voltage, channel 1) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 500-3000 ohms.

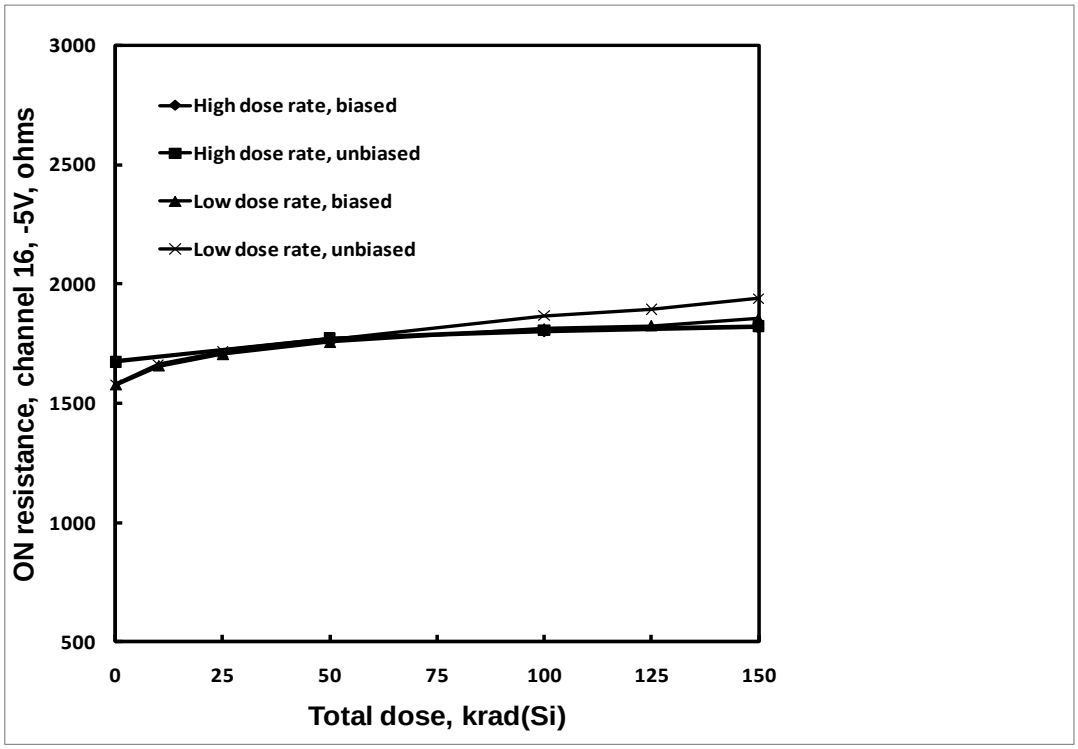

Figure 10: HS1840ARH switch ON resistance (1mA drain current, -5V source voltage, channel 16) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 500-3000 ohms.

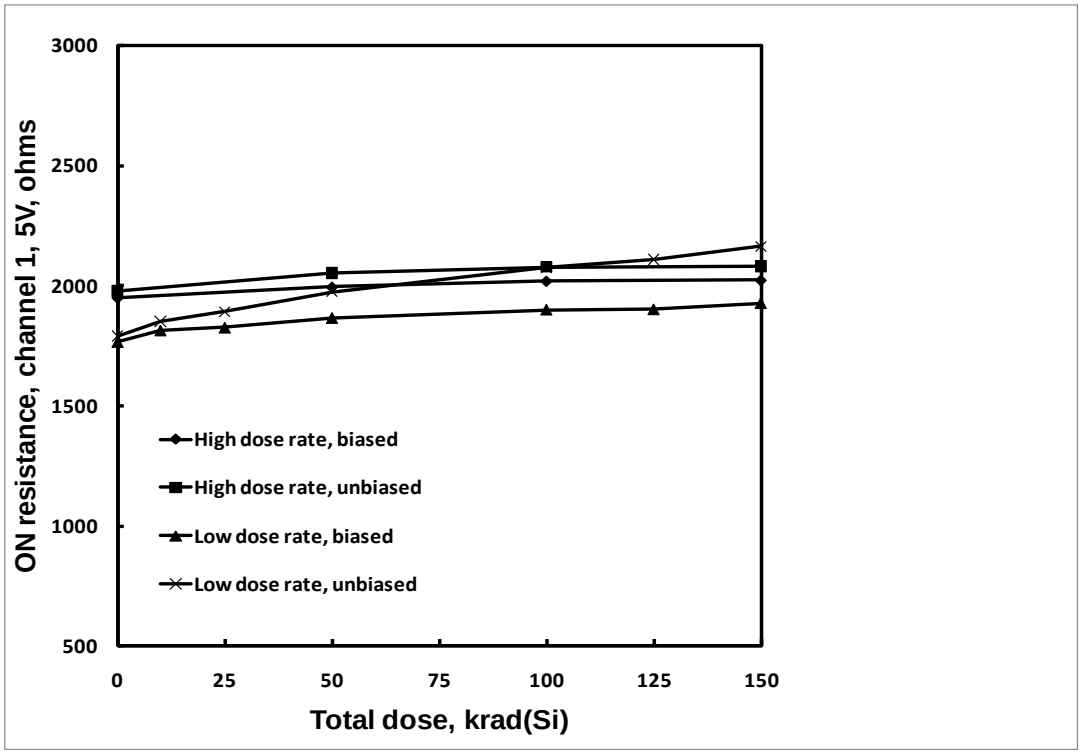

Figure 11: HS1840ARH switch ON resistance (1mA drain current, 5V source voltage, channel 1) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 500-3000 ohms.

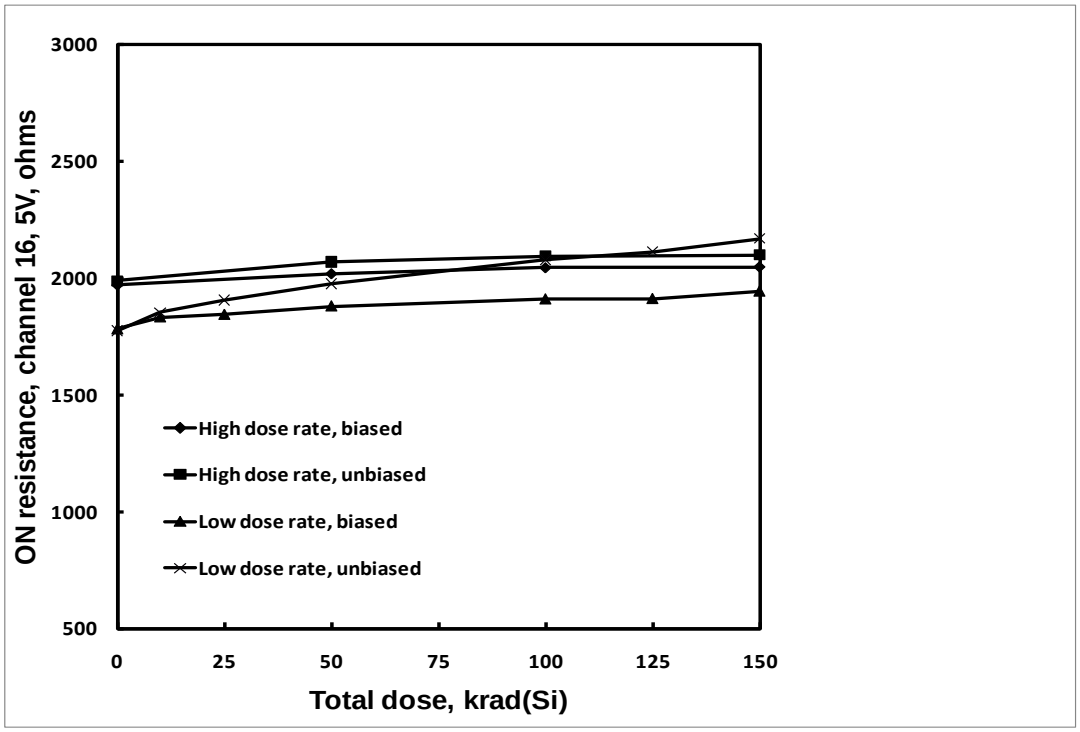

Figure 12: HS1840ARH switch ON resistance (1mA drain current, 5V source voltage, channel 16) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 500-3000 ohms.

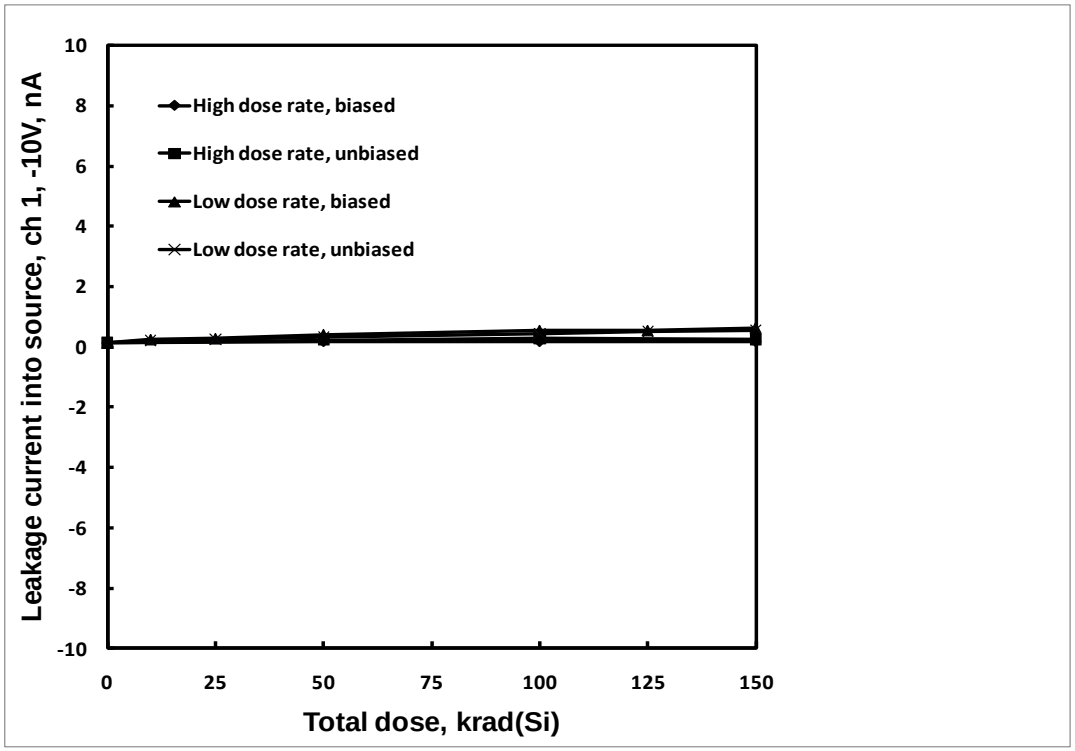

Figure 13: HS1840ARH leakage current into source (-10V source voltage, channel 1) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -100 to 100nA.

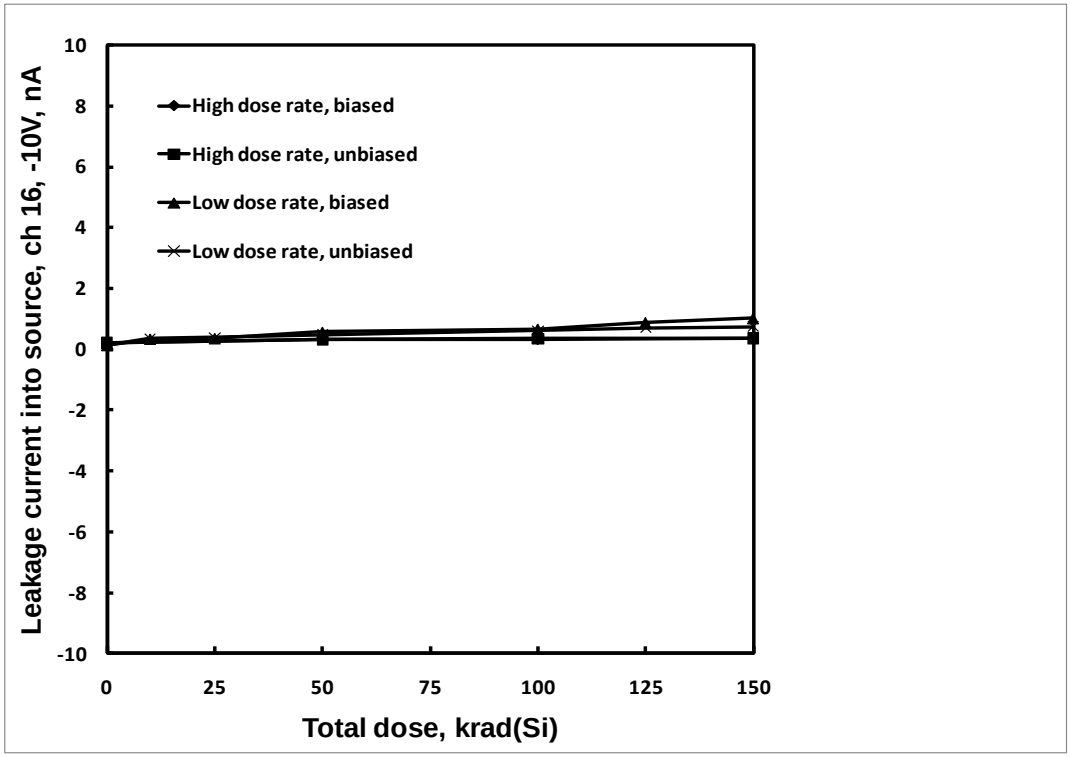

Figure 14: HS1840ARH leakage current into source (-10V source voltage, channel 16) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is -100 to 100nA.

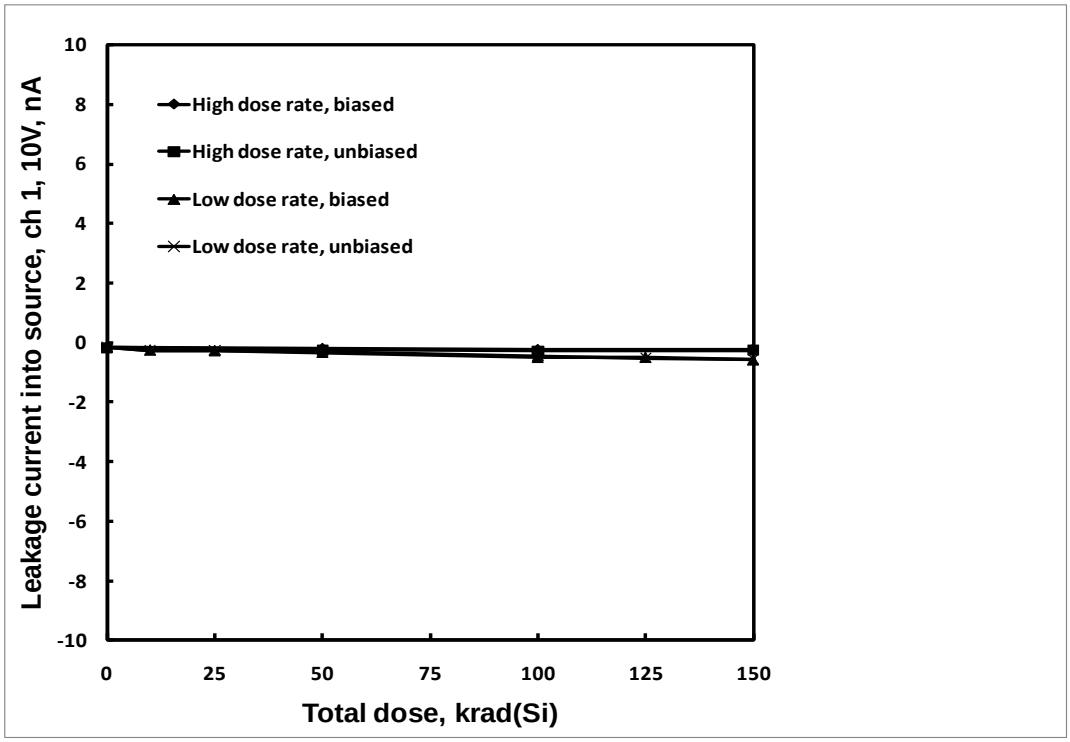

Figure 15: HS1840ARH leakage current into source (10V source voltage, channel 1) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -100 to 100nA.

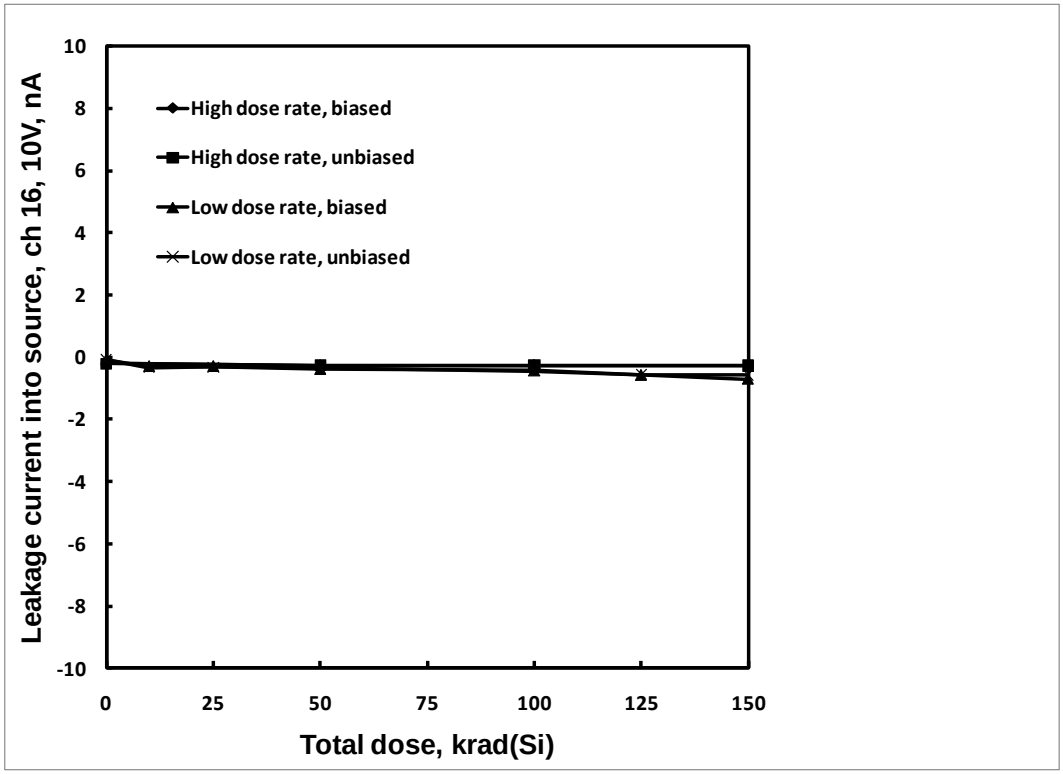

Figure 16: HS1840ARH leakage current into source (10V source voltage, channel 16) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -100 to 100nA.

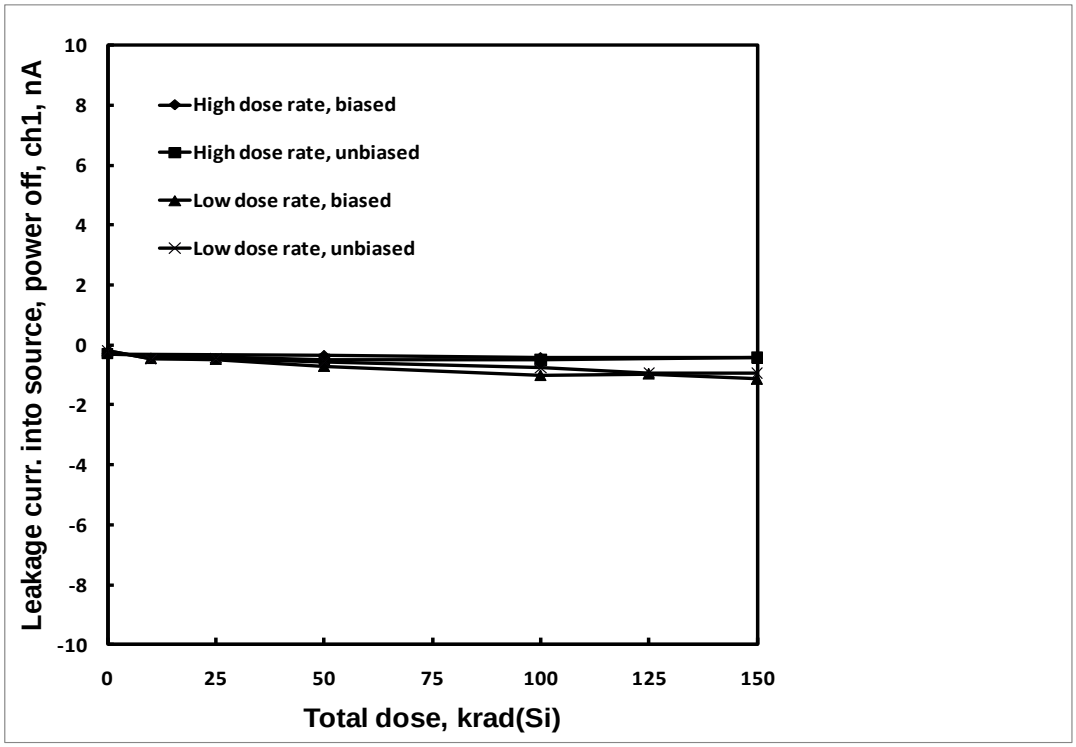

Figure 17: HS1840ARH leakage current into source (power OFF, channel 1) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -100 to 100nA.

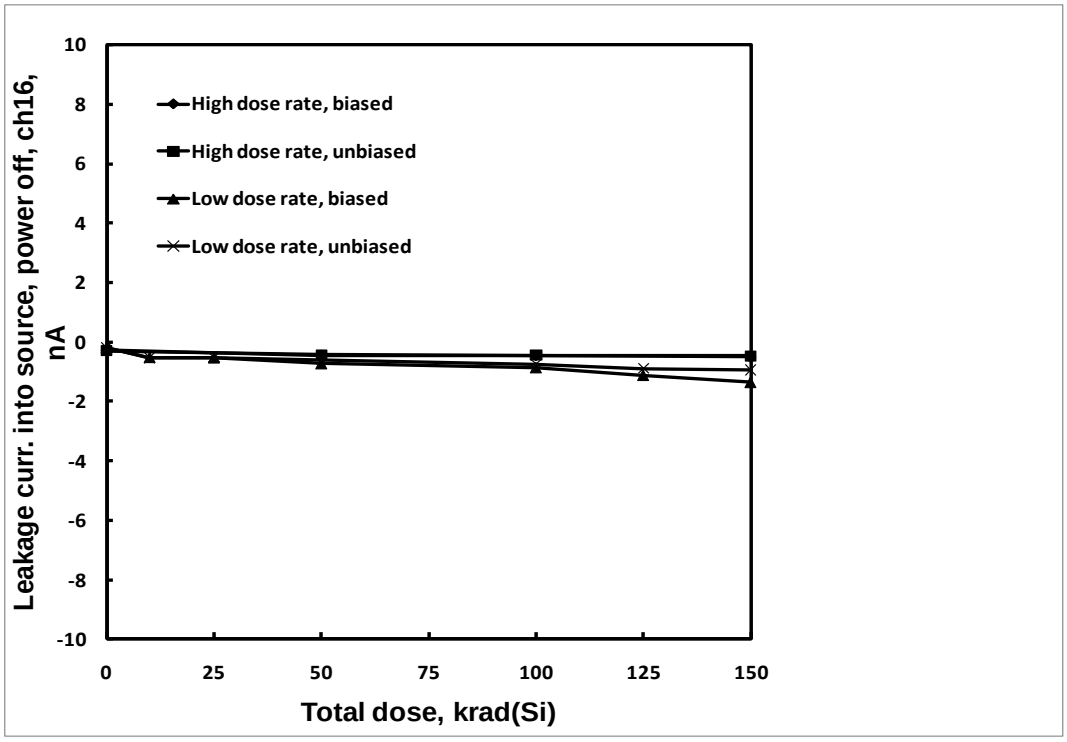

Figure 18: HS1840ARH leakage current into source (power OFF, channel 16) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -100 to 100nA.

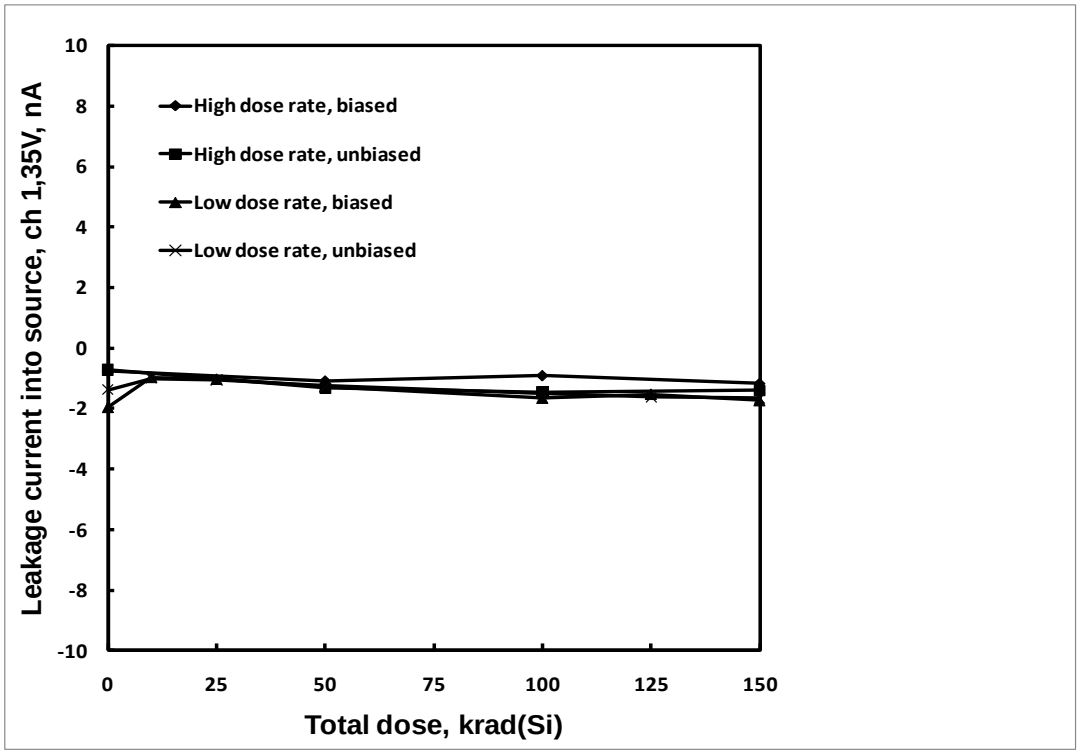

Figure 19: HS1840ARH leakage current into source (35V overvoltage, channel 1) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -1.5 to 1.5µA.

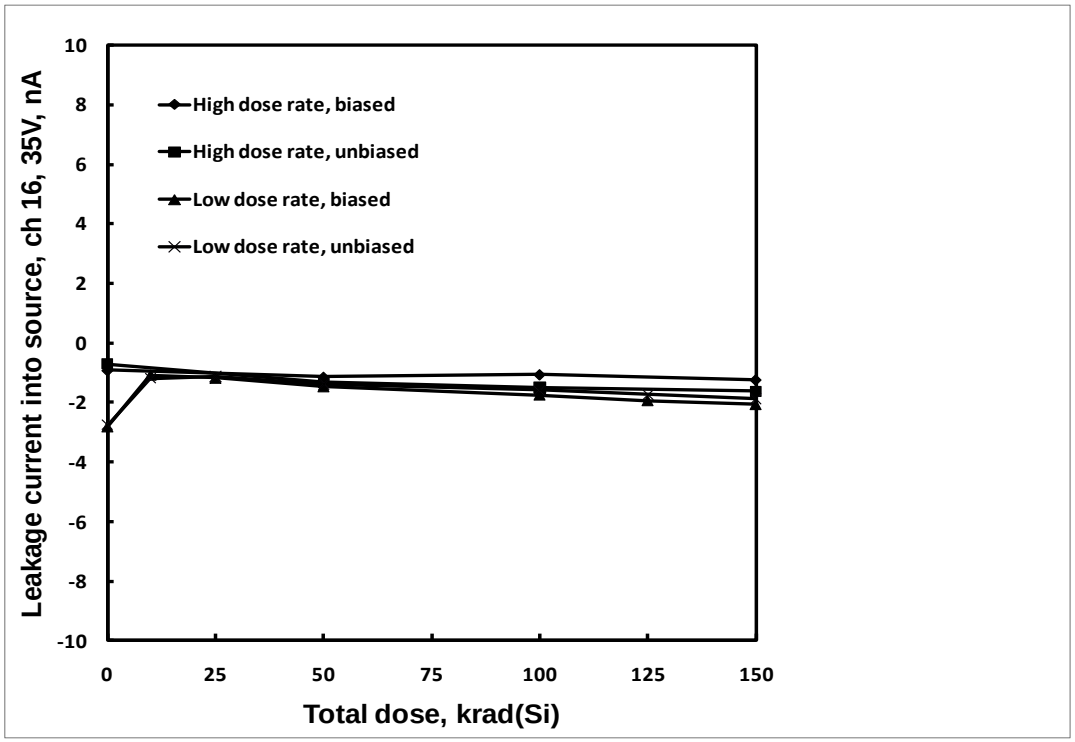

Figure 20: HS1840ARH leakage current into source (35V overvoltage, channel 16) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -1.5 to 1.5µA.

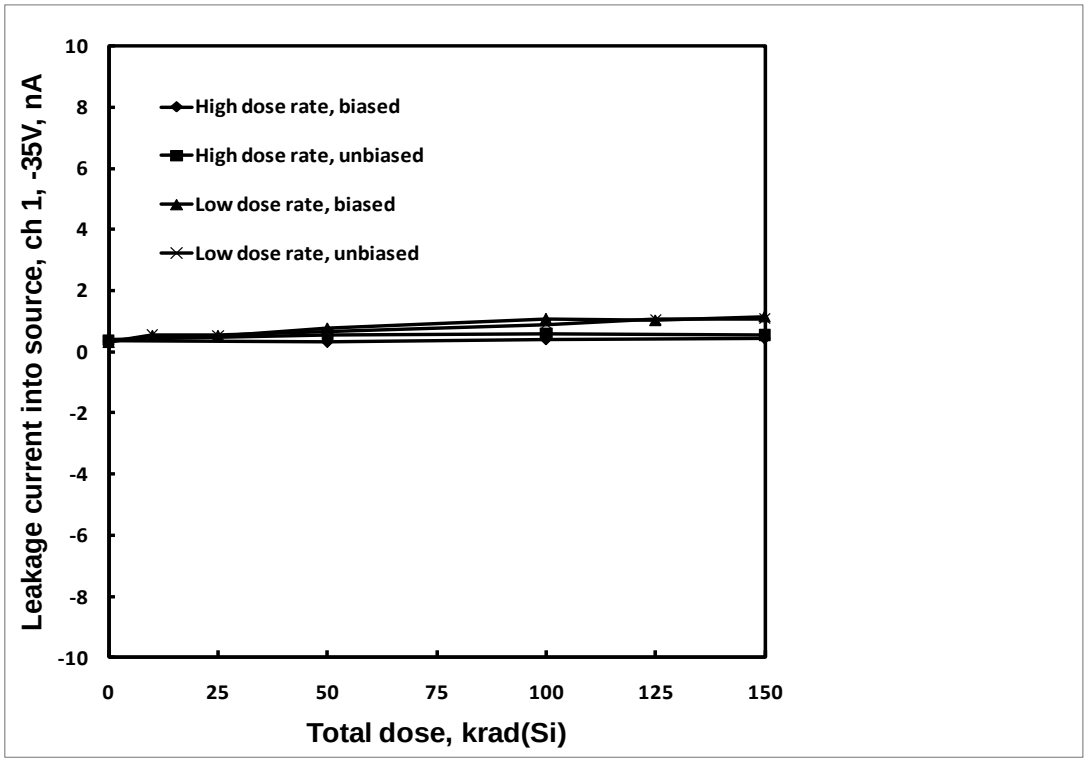

Figure 21: HS1840ARH leakage current into source (-35V overvoltage, channel 1) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -1.5 to 1.5µA.

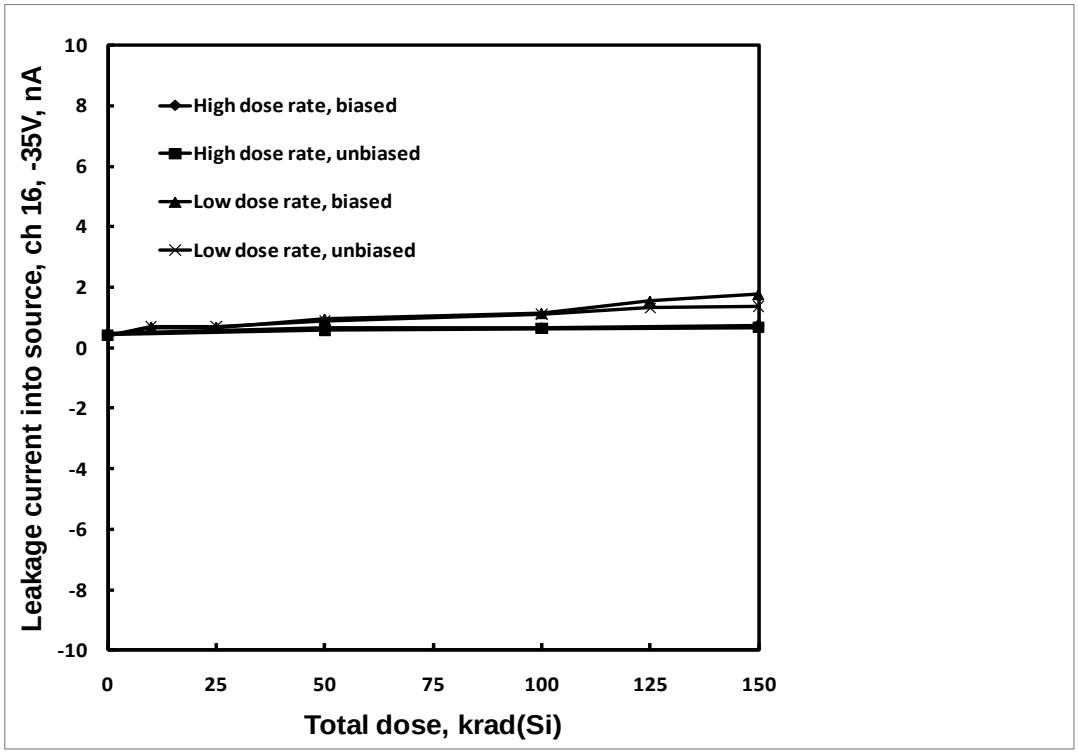

Figure 22: HS1840ARH leakage current into source (-35V overvoltage, channel 16) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -1.5 to 1.5µA.

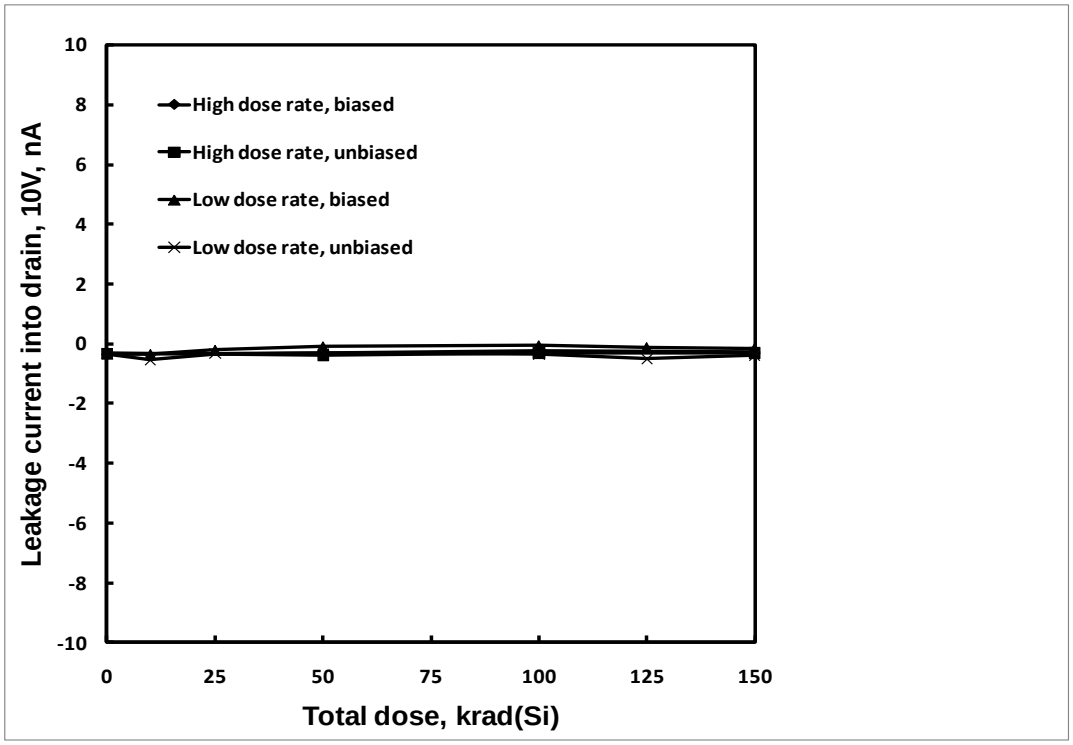

Figure 23: HS1840ARH leakage current into drain (10V) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -100 to 100nA.

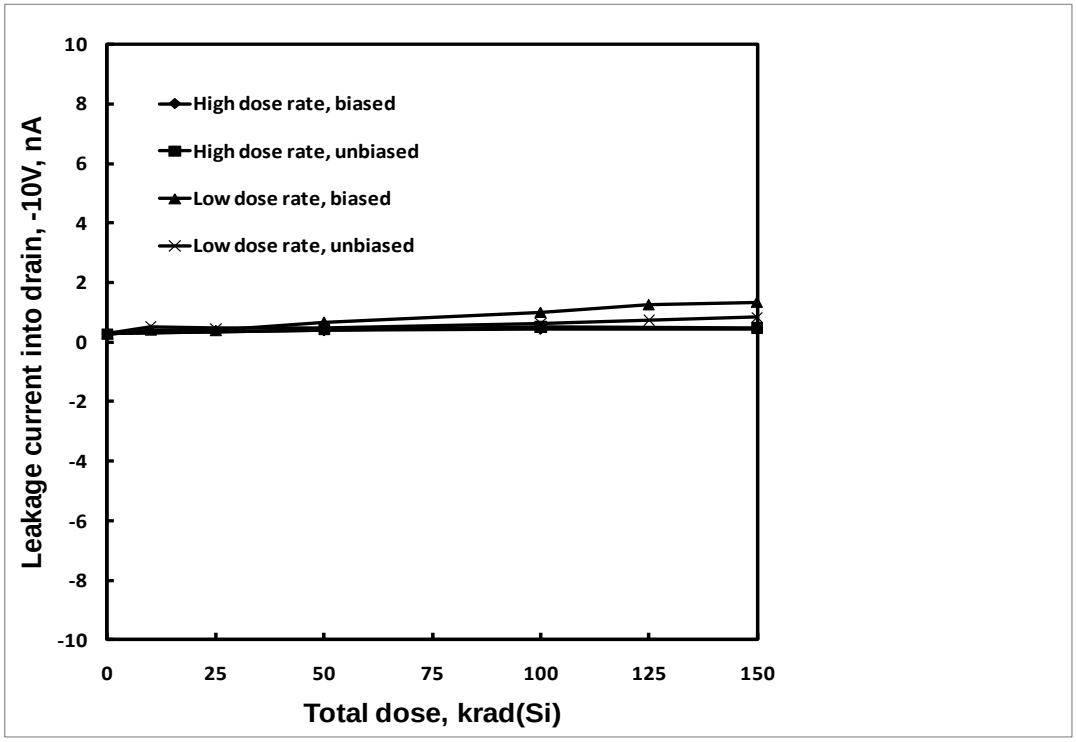

Figure 24: HS1840ARH leakage current into drain (-10V) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -100 to 100nA.

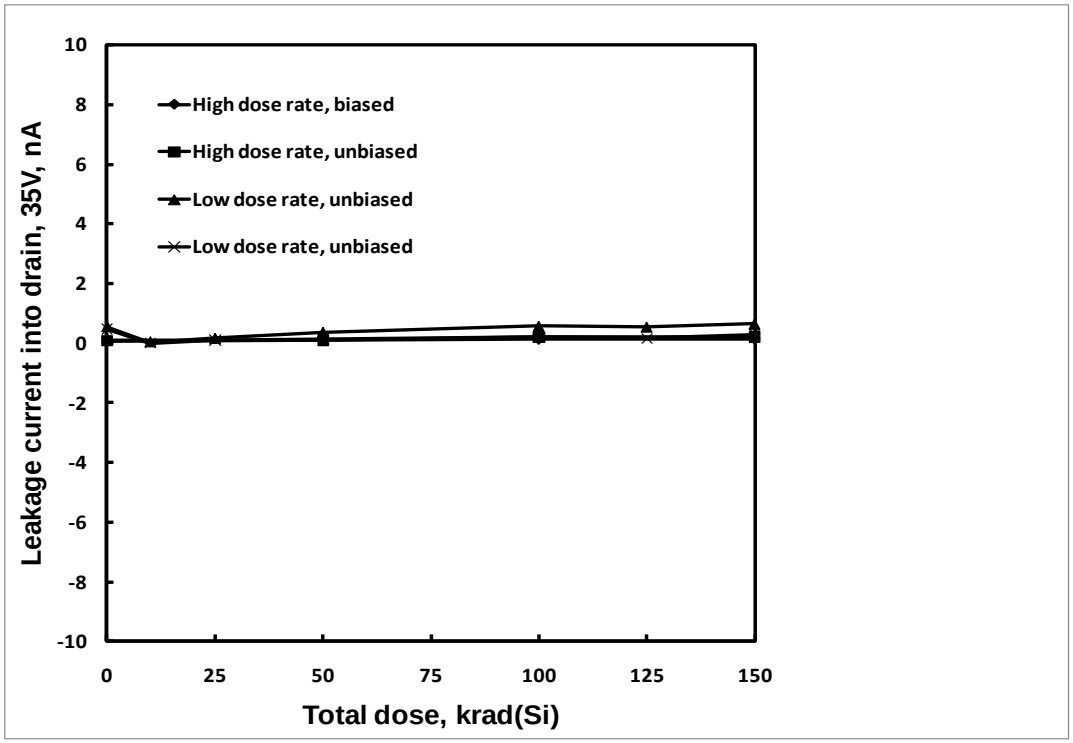

Figure 25: HS1840ARH leakage current into drain (35V overvoltage) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -1 to 1µA.

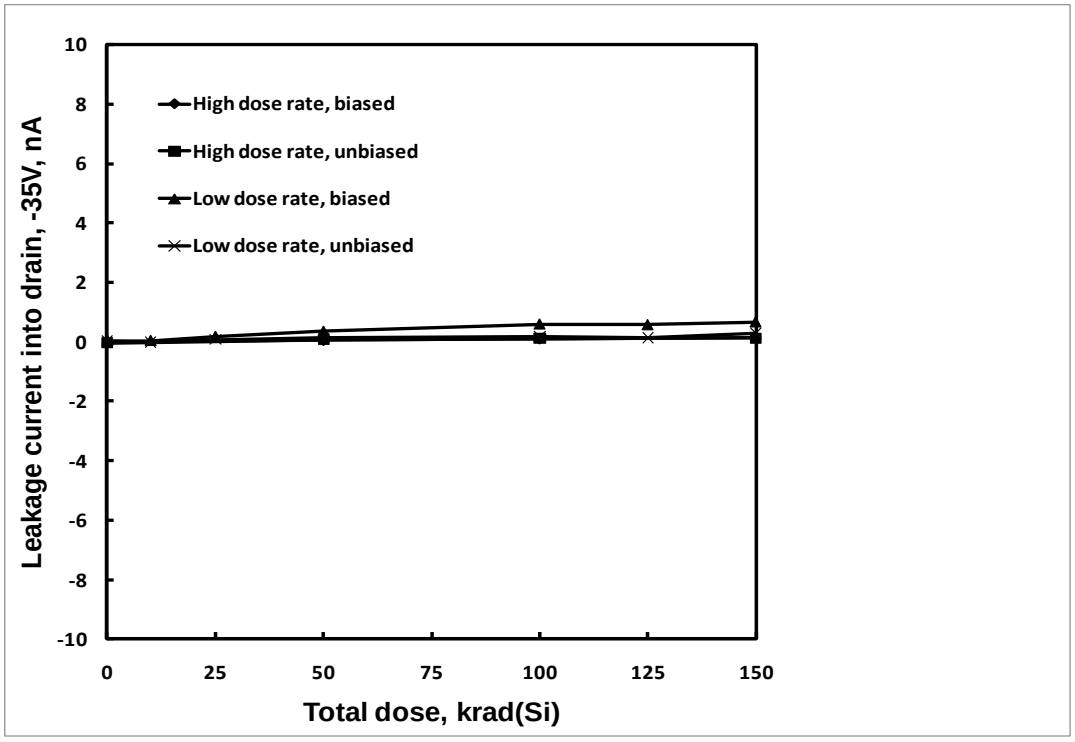

Figure 26: HS1840ARH leakage current into drain (-35V overvoltage) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -1 to 1µA.

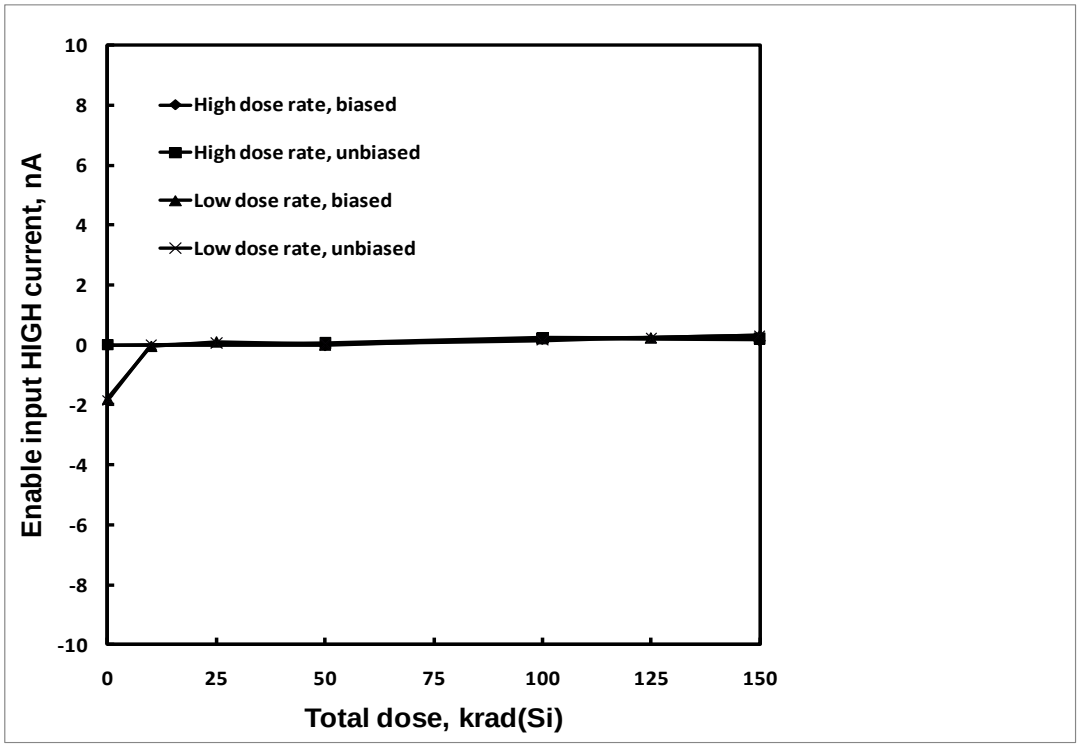

Figure 27: HS1840ARH enable input HIGH current as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -1 to 1µA.

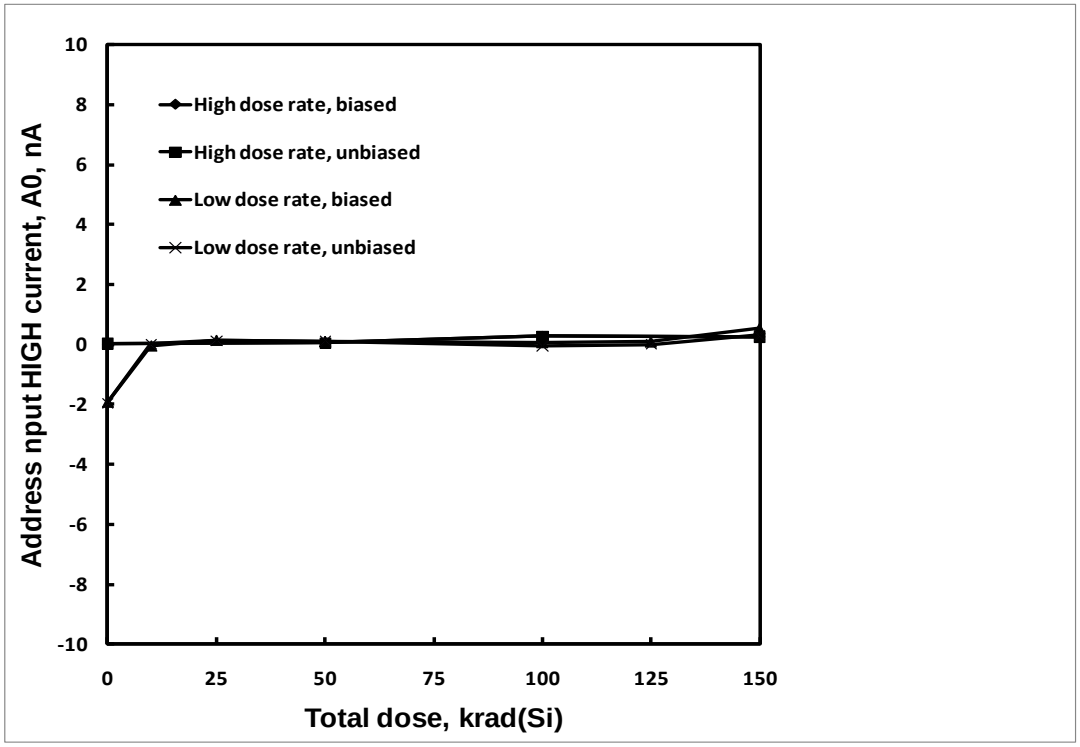

Figure 28: HS1840ARH address input HIGH current, address A0, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -1 to 1µA.

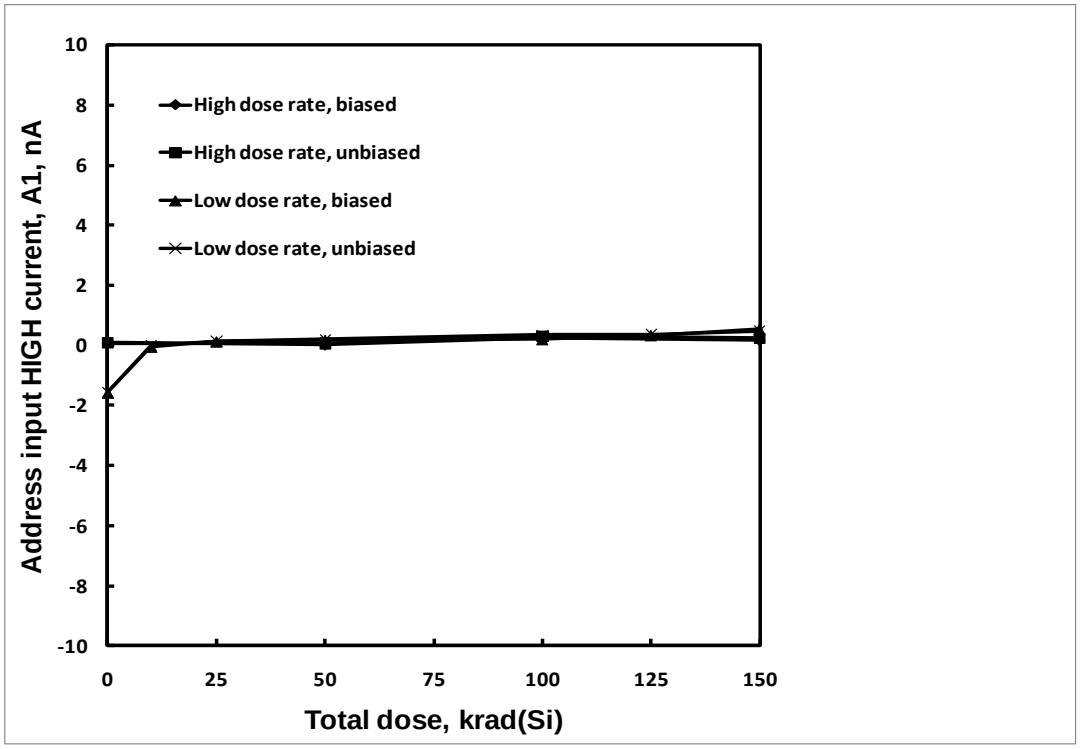

Figure 29: HS1840ARH address input HIGH current, address A1, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -1 to 1µA.

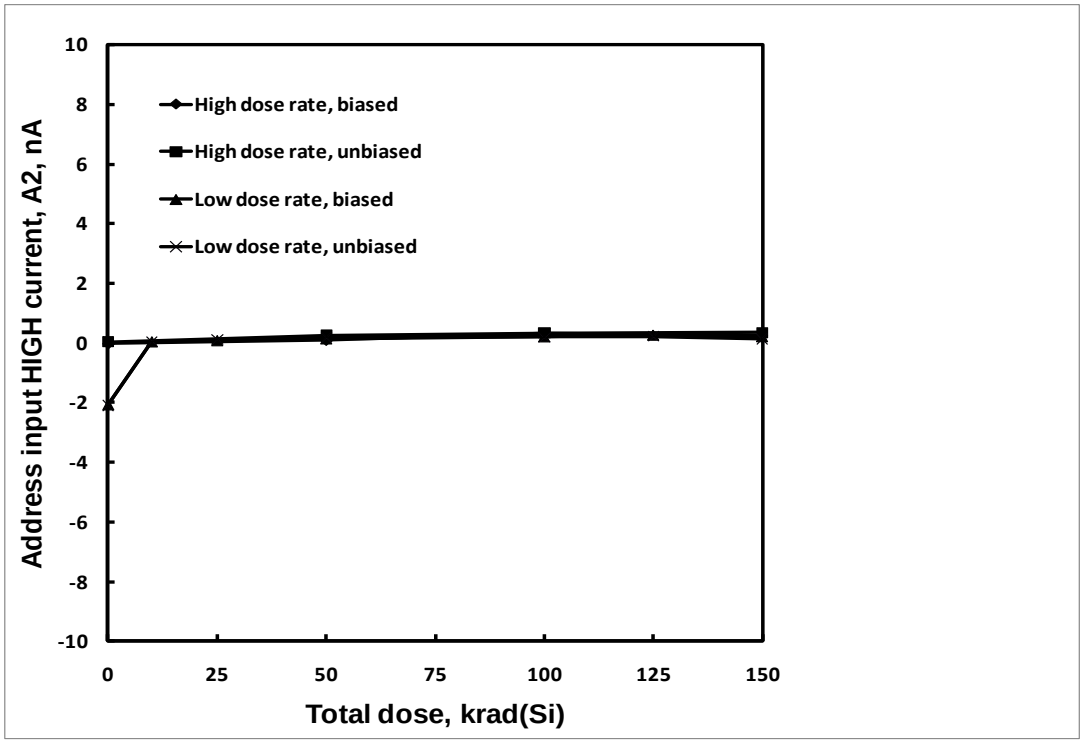

Figure 30: HS1840ARH address input HIGH current, address A2, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -1 to 1µA.

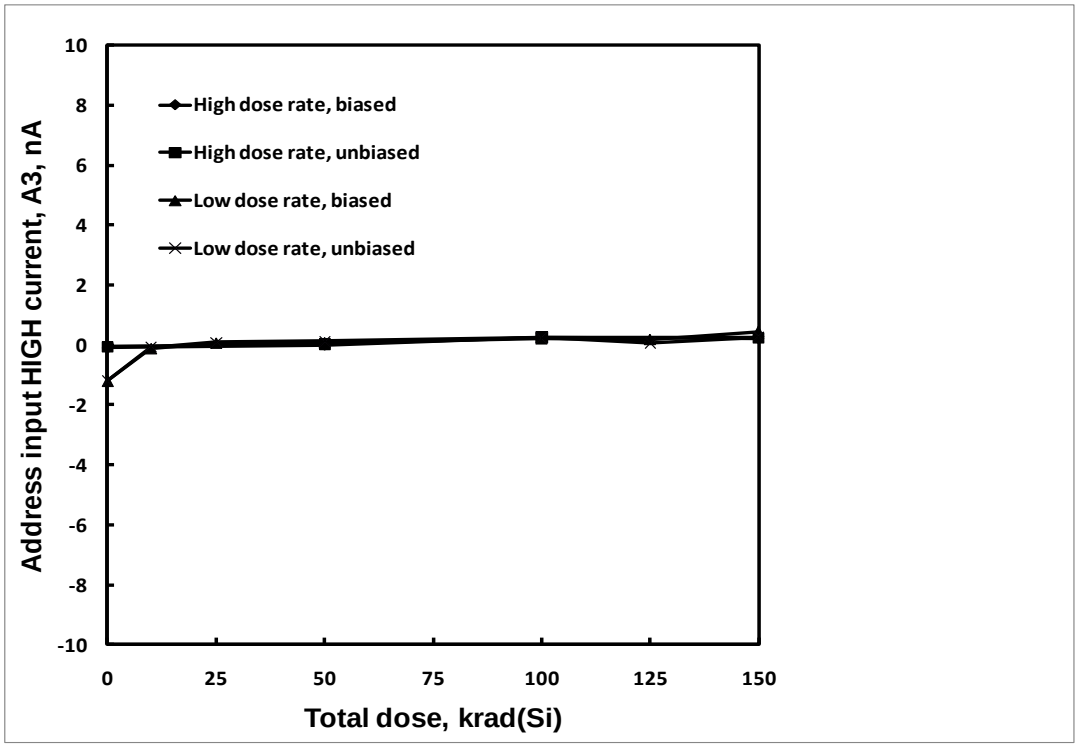

Figure 31: HS1840ARH address input HIGH current, address A3, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -1 to 1µA.

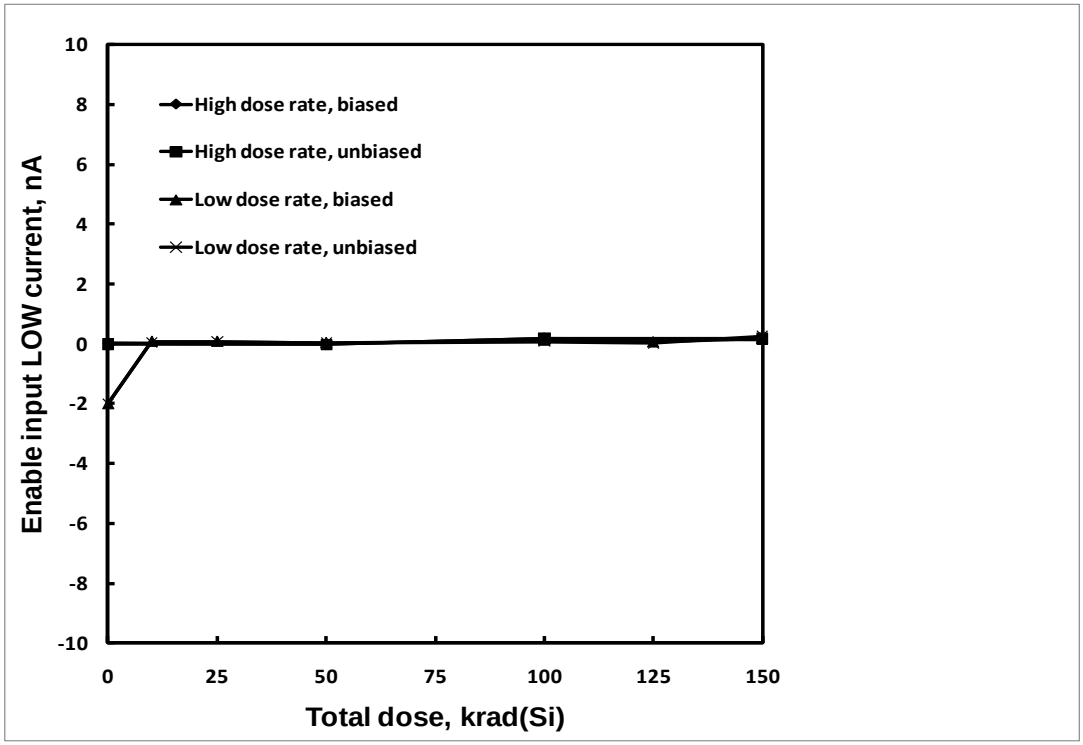

Figure 32: HS1840ARH enable input LOW current as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -1 to 1µA.

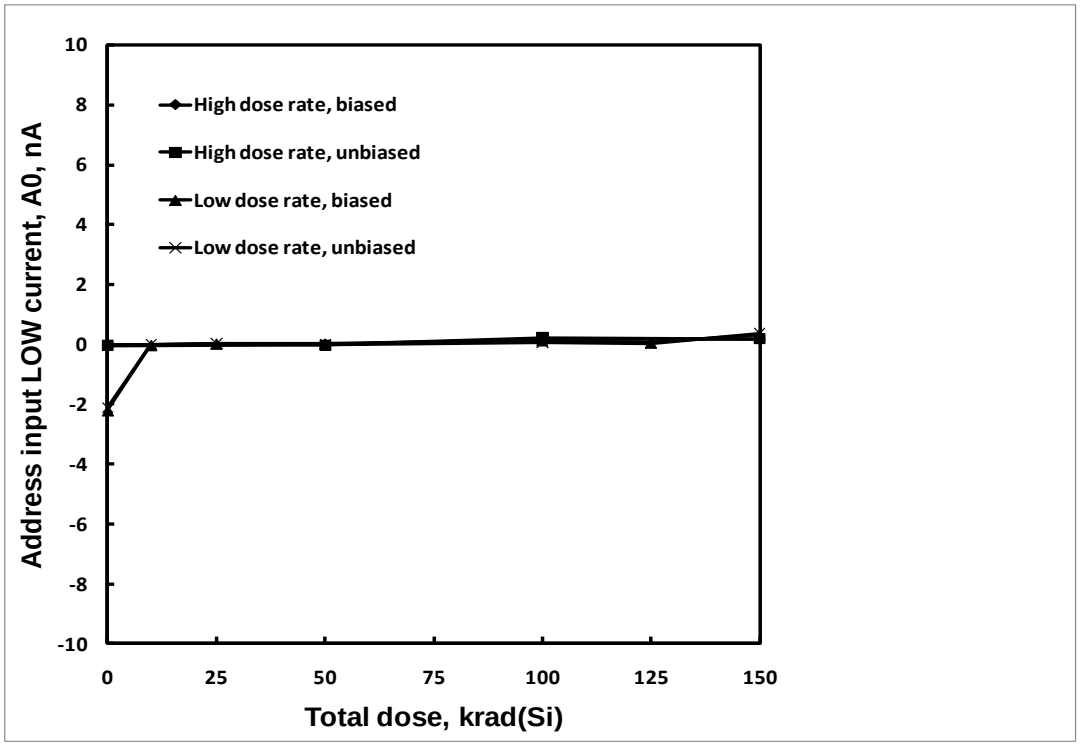

Figure 33: HS1840ARH address input LOW current, address A0, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -1 to 1µA.

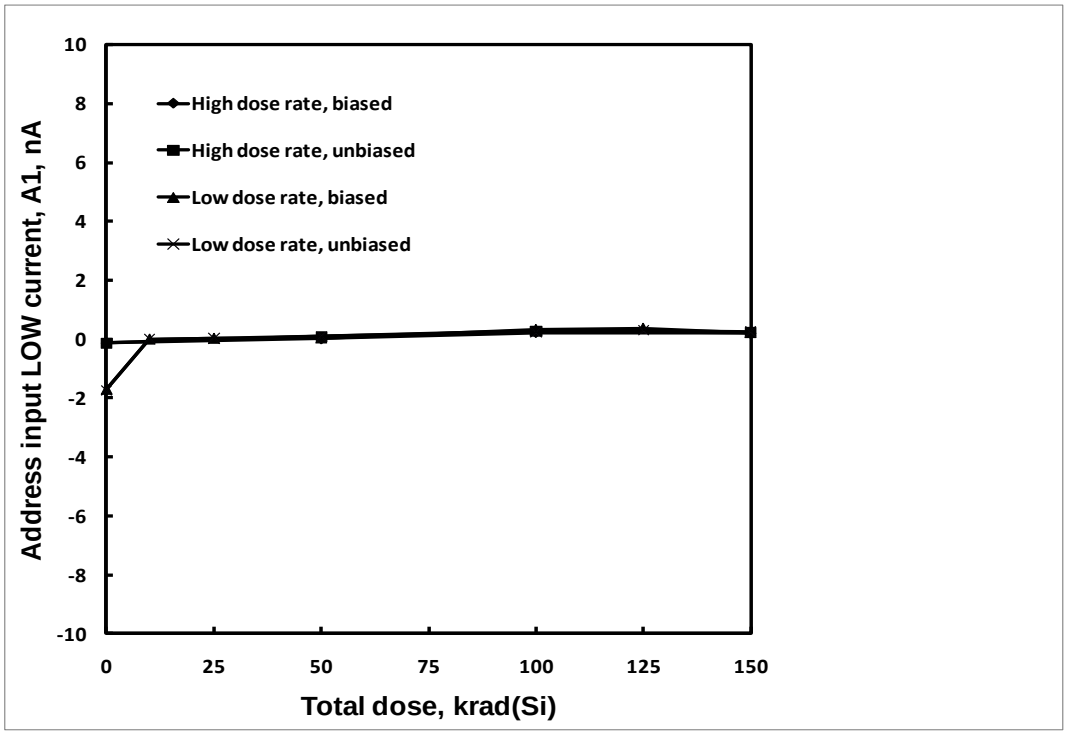

Figure 34 HS1840ARH address input LOW current, address A1, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -1 to 1µA.

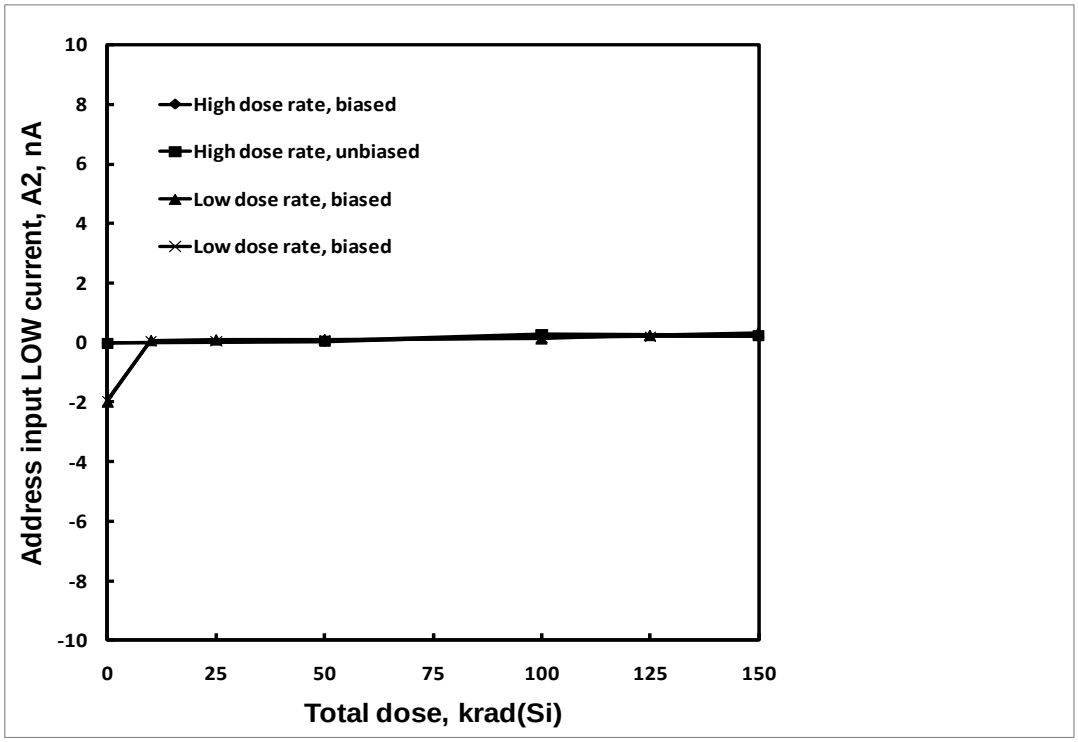

Figure 35: HS1840ARH address input LOW current, address A2, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -1 to 1µA.

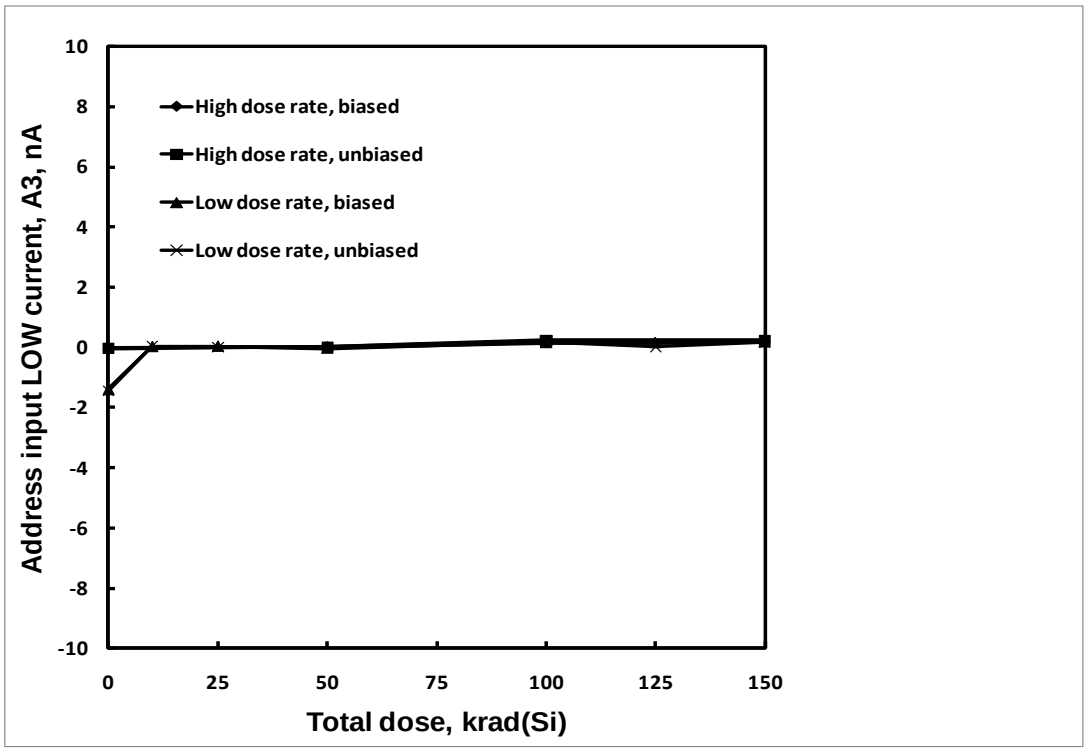

Figure 36: HS1840ARH address input LOW current, address A3, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -1 to 1µA.

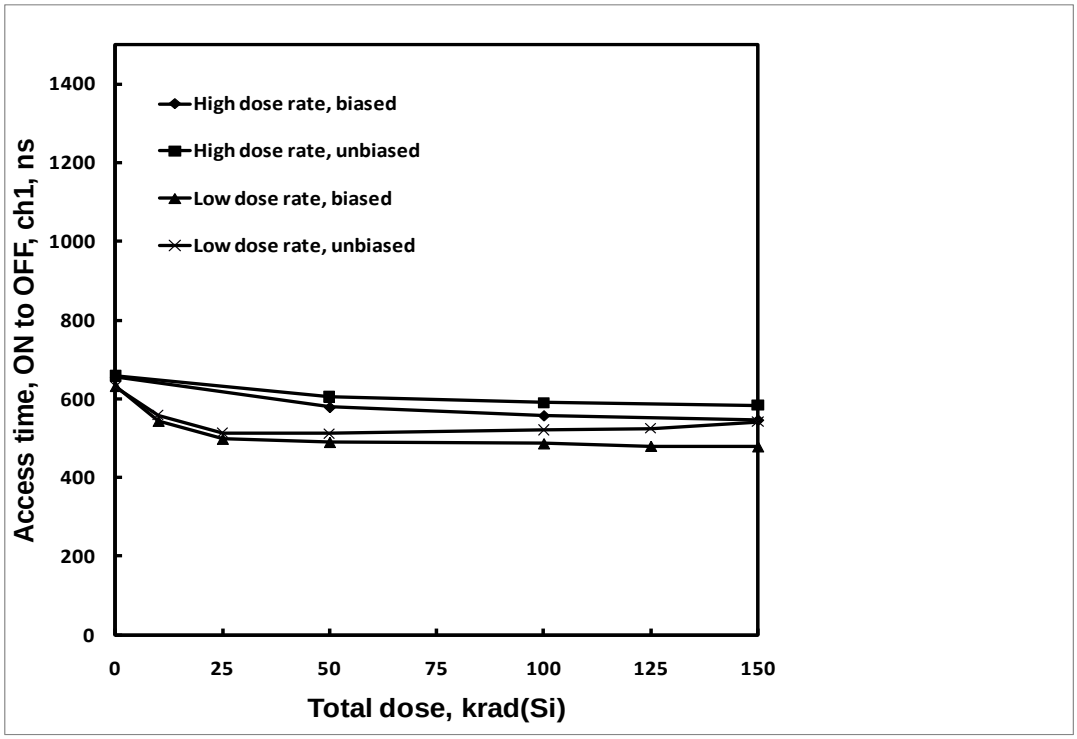

Figure 37: HS1840ARH access time, ON to OFF, channel 1, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 1.5µs.

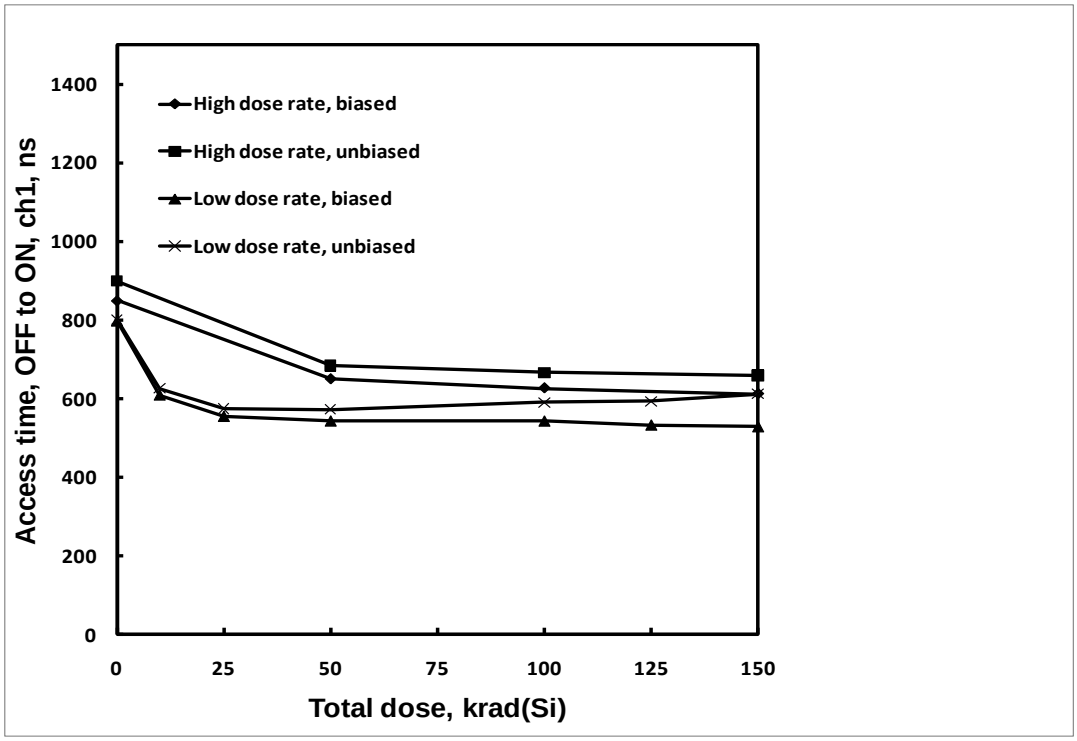

Figure 38: HS1840ARH access time, OFF to ON, channel 1, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 1.5µs.

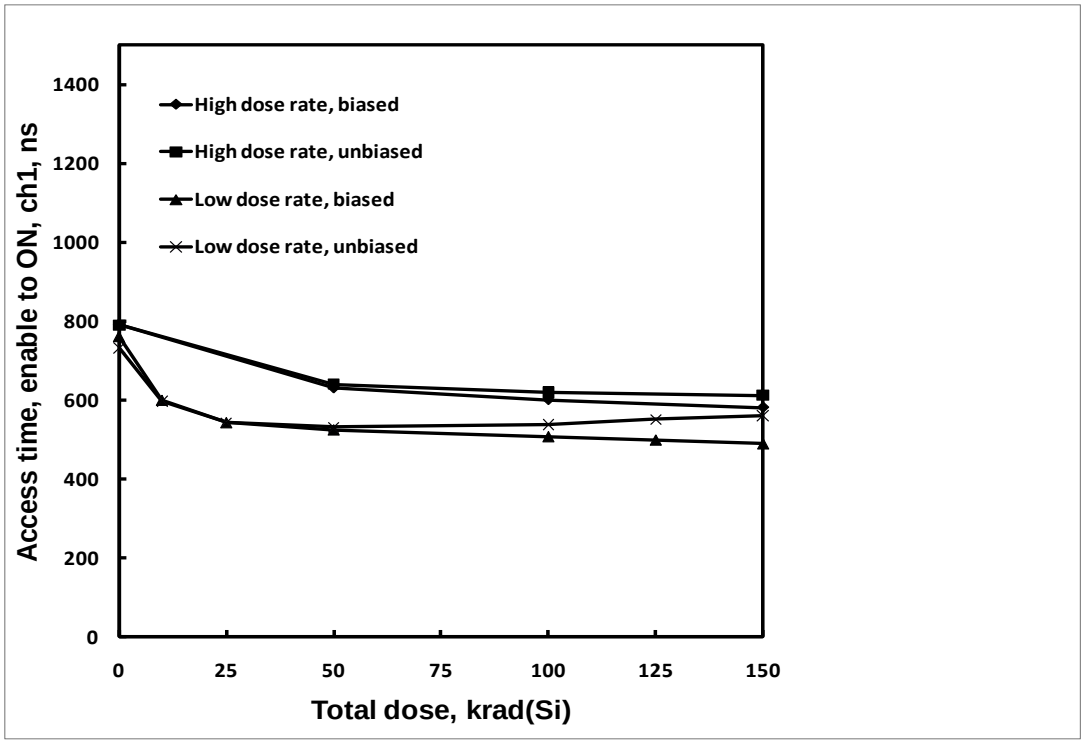

Figure 39: HS1840ARH access time, enable to ON, channel 1, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 1.5µs.

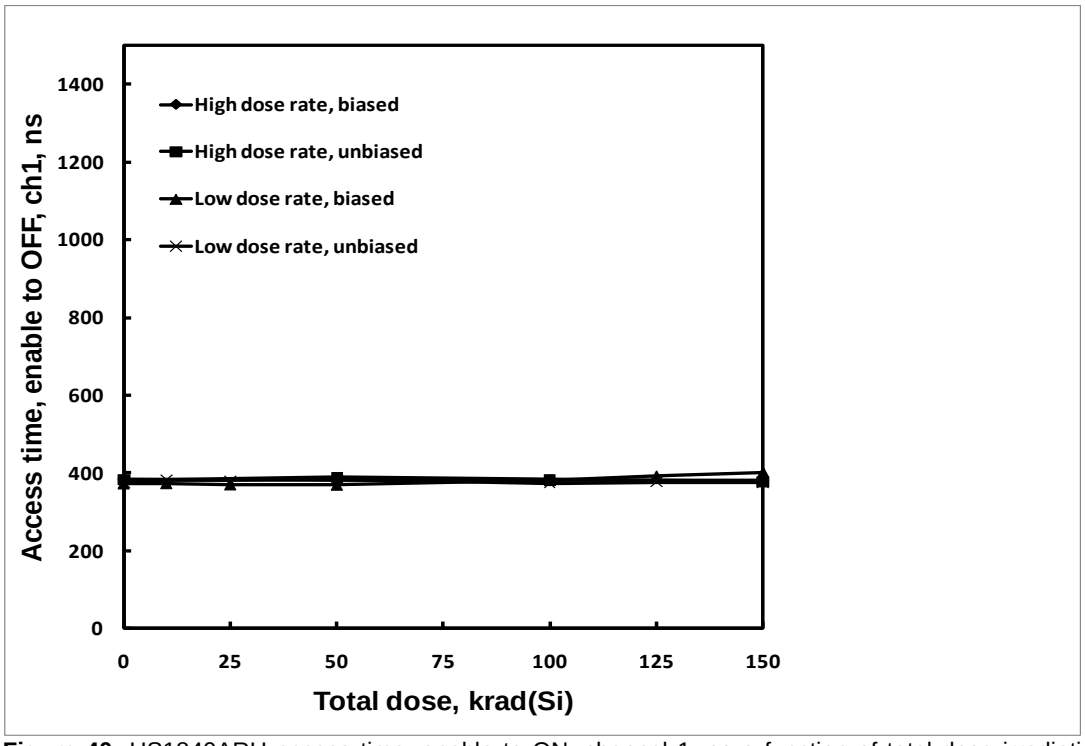

Figure 40: HS1840ARH access time, enable to ON, channel 1, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 1.5µs.

6: Conclusion

This document reports interim results of a total dose test of the HS1840ARH 16-channel analog multiplexer. Parts were tested at low and high dose rate under biased and unbiased conditions as outlined in MIL-STD-883 Test Method 1019.7, to a maximum total dose of 150krad(Si).

ATE characterization testing at downpoints showed no rejects to the SMD Group A limits. Variables data for selected parameters is presented in Figures 3 through 49.

As a determinant of low dose rate sensitivity, MIL-STD-883 Test Method 1019.7 specifies that a delta_parameter calculation be performed for any parameters that exceed the Group A limits. These calculations were not required as there were no rejects against the Group A limits. Accordingly, the part is considered ELDRS insensitive up to 150krad(Si).

Similarly, no differences between biased and unbiased irradiation were noted, and the part is not considered bias sensitive.

7: Appendices

7.1: Reported parameters.

Figure	Parameter	Limit, low	Limit, high	Units	Notes
3	Positive supply current		500	µA	
4	Negative supply current		500	µA	
5	Positive standby supply current		500	µA	
6	Negative standby supply current		500	µA	
7	Switch ON resistance	500	3000	ohms	Channel 1
8	Switch ON resistance	500	3000	ohms	Channel 16
9	Switch ON resistance	500	3000	ohms	Channel 1
10	Switch ON resistance	500	3000	ohms	Channel 16
11	Switch ON resistance	500	3000	ohms	Channel 1
12	Switch ON resistance	500	3000	ohms	Channel 16
13	OFF source leakage	-100	100	nA	-10V
14	OFF source leakage	-100	100	nA	-10V
15	OFF source leakage	-100	100	nA	+10V
16	OFF source leakage	-100	100	nA	+10V
17	OFF source leakage	-100	100	nA	Power OFF
18	OFF source leakage	-100	100	nA	Power OFF
19	OFF source leakage	-1.5	1.5	µA	Overvoltage, 35V
20	OFF source leakage	-1.5	1.5	µA	Overvoltage, 35V
21	OFF source leakage	-1.5	1.5	µA	Overvoltage, -35V
22	OFF source leakage	-1.5	1.5	µA	Overvoltage, -35V

23	ON source leakage	-100	100	nA	10V
24	ON source leakage	-100	100	nA	-10V
25	ON source leakage	-1	1	µA	Overvoltage, 35V
26	ON source leakage	-1	1	µA	Overvoltage, -35V
27	Input HIGH current	-1	1	µA	Enable
28	Input HIGH current	-1	1	µA	Address A0
29	Input HIGH current	-1	1	µA	Address A1
30	Input HIGH current	-1	1	µA	Address A2
31	Input HIGH current	-1	1	µA	Address A3
32	Input LOW current	-1	1	µA	Enable
33	Input LOW current	-1	1	µA	Address A0
34	Input LOW current	-1	1	µA	Address A1
35	Input LOW current	-1	1	µA	Address A2
36	Input LOW current	-1	1	µA	Address A3
37	Access time, ON to OFF		1.5	µs	Channel 1
38	Access time, OFF to ON		1.5	µs	Channel 16
39	Access time, enable to ON		1.5	µs	Channel 1
40	Access time, enable to ON		1.5	µs	Channel 16

Note 1: Limits are taken from Standard Microcircuit Drawing (SMD) 5962-95630.

8: Document revision history

Revision	Date	Pages	Comments
0	23 March 2010	All	Original issue