

# Evaluation of Subsystem Clock Oscillation Circuit

[HD64F38124H-80A] QFP(14x14) 0.65mm pitch

Measurement conditions : 5.0V , 3.3V

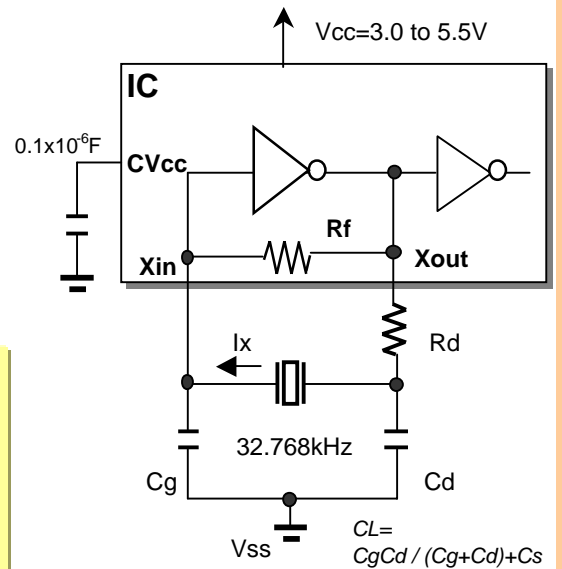
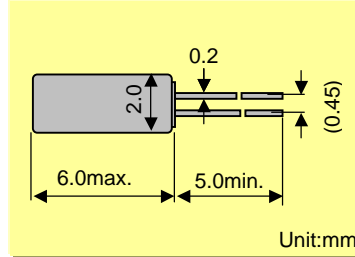


Model :VT-200  
 Frequency :Fo=32.768kHz  
 Frequency tolerance :dF/Fo= +/-20x10<sup>6</sup>  
 Load capacitance :CL=12.5pF  
 Equivalent series resistance :R1=50kohm max  
 Max. Drive level :DL=1x10<sup>6</sup>W max  
 Recommended drive level :DL=0.1x10<sup>6</sup>W typ

### FEATURES

- 1.Compact tubular package
- 2.Photolithographic process
- 3.Excellent shock resistance and environmental characteristics.
- 4.Real time clocks, Timers, Portable applications

### DIMENSIONS(VT-200)



Remark) I<sub>x</sub> : current through crystal

When the internal power supply Step-Down circuit is not used, please connect the external power supply to the CVcc pin and Vcc pin.

The permissible range for the power supply voltage is 3.0V to 3.6V.

MODEL:VT-200 12.5pF with HD64F38124H at 25°C

| Key specifications                        | Vcc=3.3V | Vcc=5.0V | Remarks                                   |
|---|----------|----------|---|
| Current control resistance : Rd ( k ohm ) | 0        | 0        | Control drive level & secure phase margin |
| Capacitance at gate : Cg ( pF )           | 20       | 20       | Optimal capacity in response to CL        |
| Capacitance at drain : Cd ( pF )          | 20       | 20       | ( CL = Cd // Cg + stray capacitance )     |

| Circuit characteristics ( at 25°C )                   | Vcc=3.3V | Vcc=5.0V | Remarks   |
|---|----------|----------|---|
| Matching Accuracy : df / f ( x10 <sup>-6</sup> )      | -3.6     | -3.2     | Frequency offset volume at specified Vdd  |
| Voltage Fluctuation : +/-df / V ( x10 <sup>-6</sup> ) | 0.0      | 0.0      | Vdd +/-10% ( Standard operating voltage range )   |
| Drive Level : DL ( x10 <sup>-6</sup> W )              | 0.30     | 0.30     | DL=I <sub>x</sub> <sup>2</sup> Re < 1x10 <sup>-6</sup> W, Re=R1( 1 + Co / CL ) <sup>2</sup> |
| Negative resistance :   - RL   ( kohm )               | 944      | 944      | 5 times larger than R <sub>1MAX</sub>   |
| Oscillation allowance : M ( times )                   | 18.9     | 18.9     | Judgemental standard of oscillation stability   |
| Oscillation start up time : Ts ( sec )                | 0.56     | 0.54     | Time to reach 90% of output level   |

| Temperature characteristics of circuit            | Vcc=3.3V | Vcc=5.0V | Remarks   |
|---|----------|----------|---|
| at -40°C Variation : df / T ( x10 <sup>-6</sup> ) | -142     | -142     | Typ.Tp=25°C ( K = -3.5x10 <sup>-8</sup> / °C <sup>2</sup> ) |
| at +85°C Variation : df / T ( x10 <sup>-6</sup> ) | -129     | -128     | Typ.Tp=25°C ( K = -3.5x10 <sup>-8</sup> / °C <sup>2</sup> ) |

The mention value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

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We value the "takumi" spirit.

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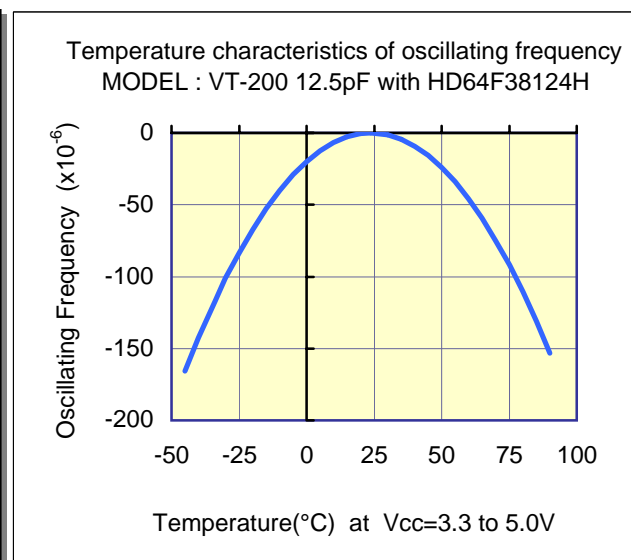
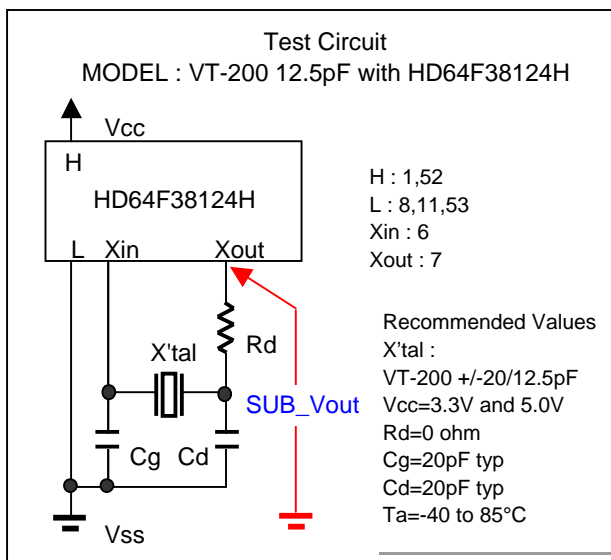
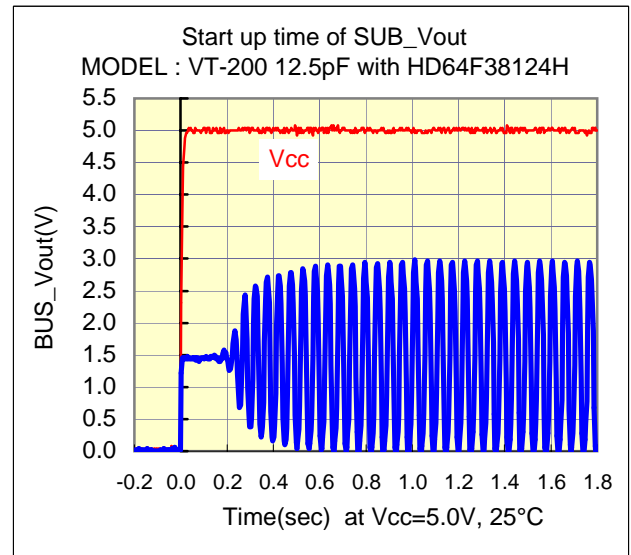
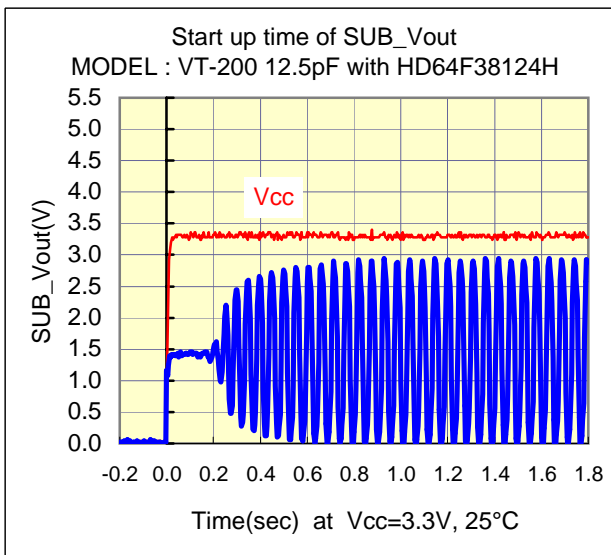
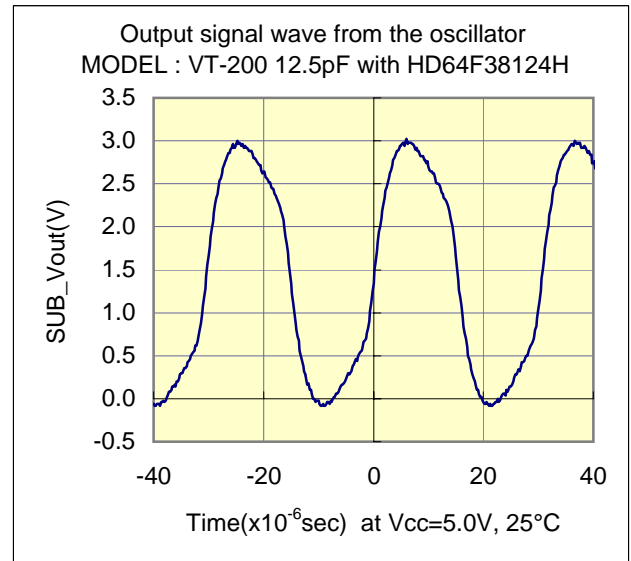
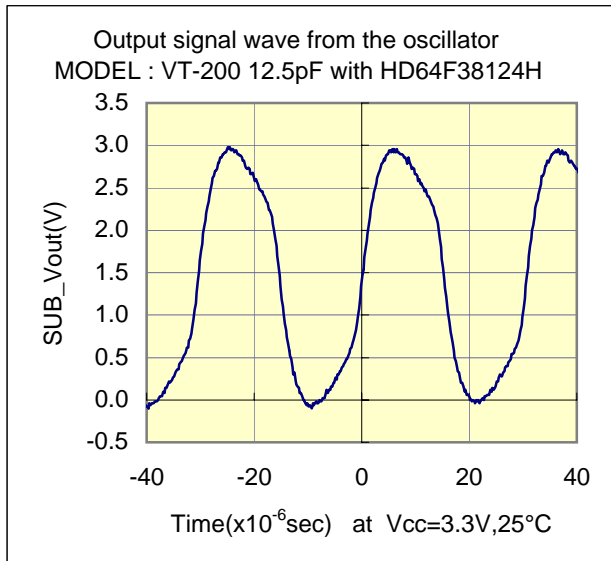
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## Test Data



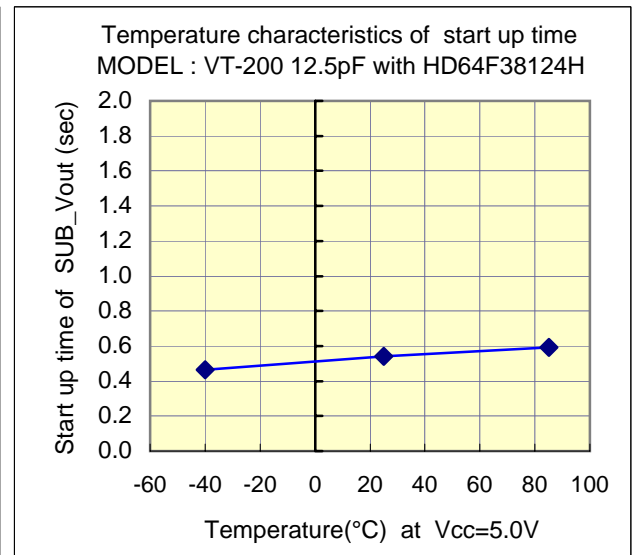
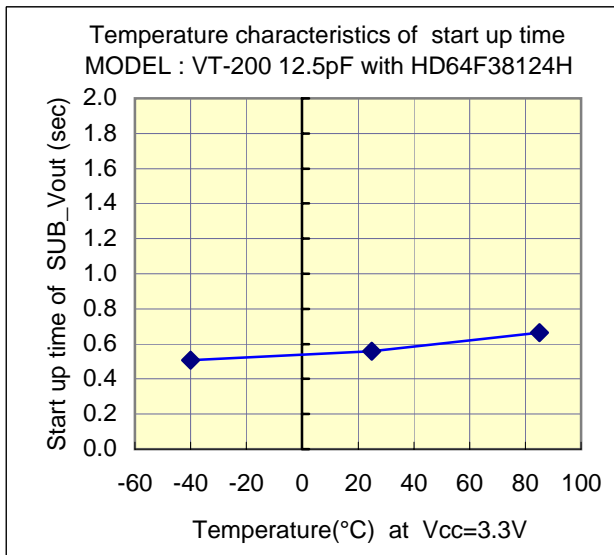
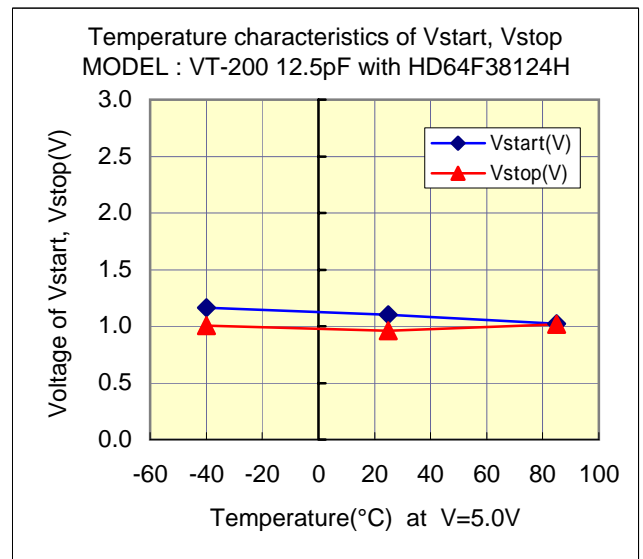
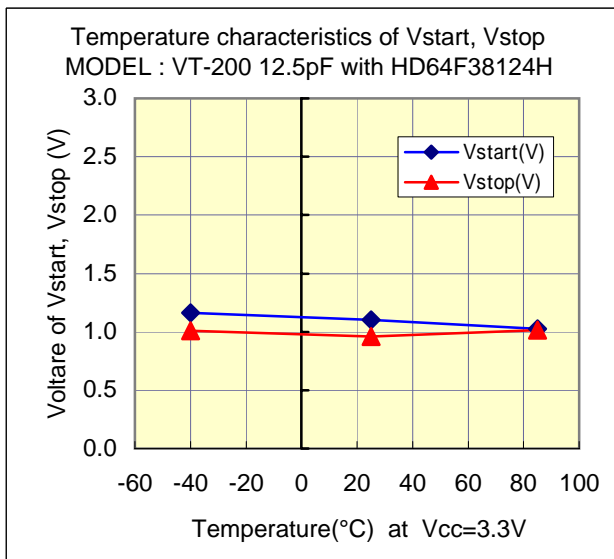
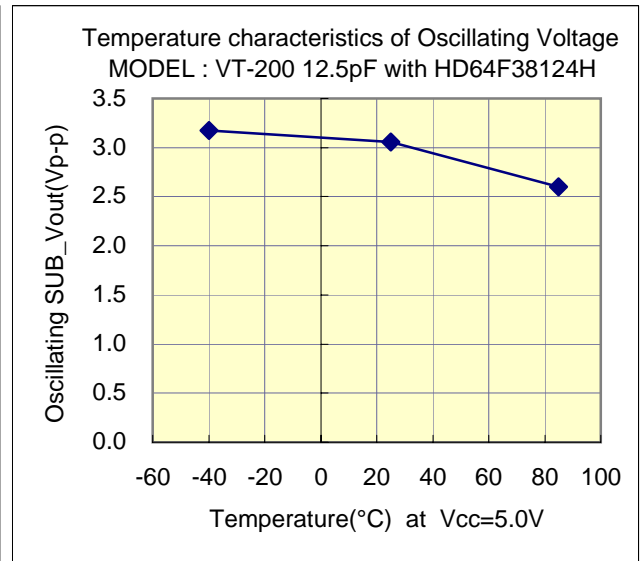
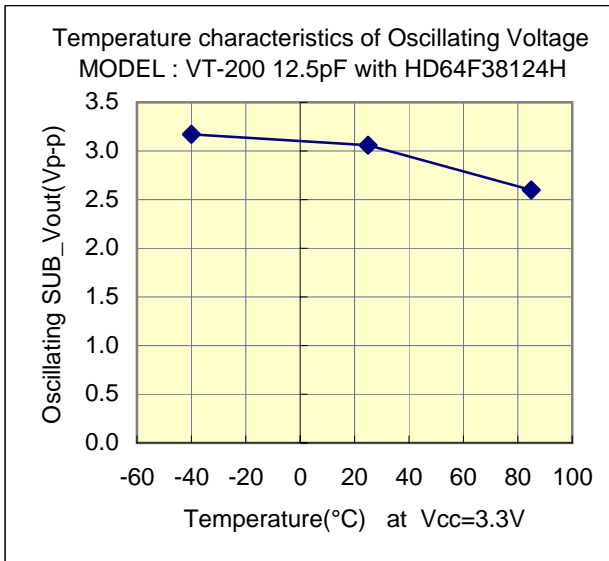
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## Test Data : Temperature characteristics



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## Referencial components layout(see Figure 1)

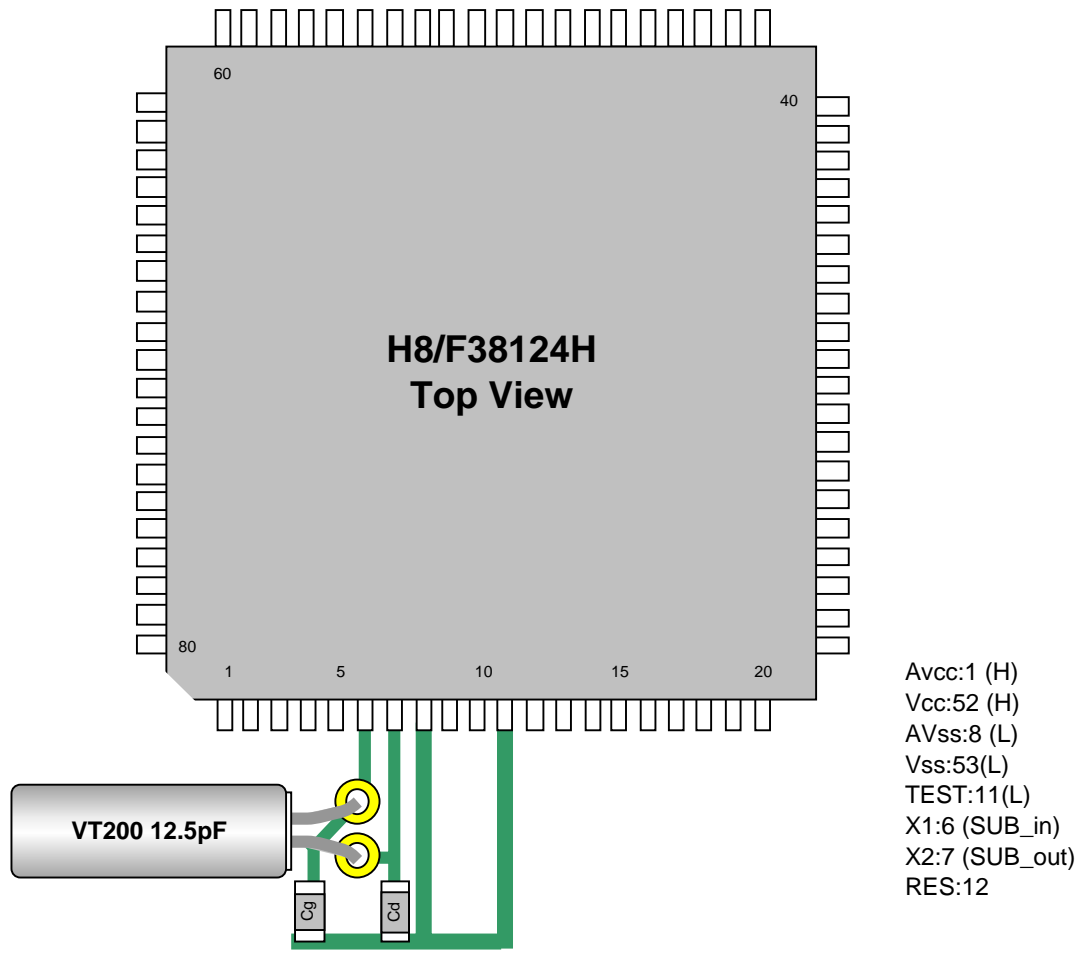


Figure 1 Referencial components layout

## Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB\_in and SUB\_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

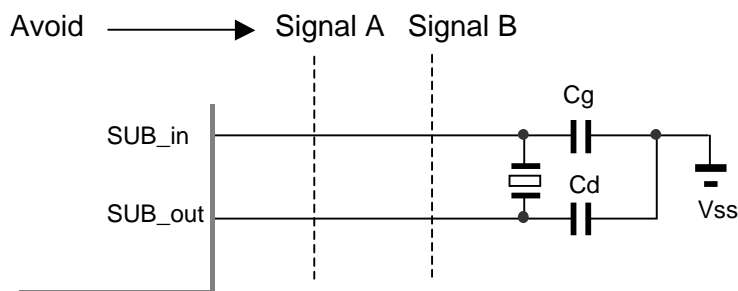


Figure 2 Example of Incorrect Board Design

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## [Evaluation Sample : VT-200 12.5pF at 25°C]

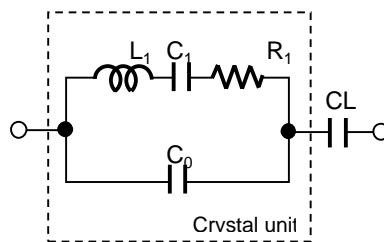
| SAMPLE           | No. | CL( pF ) | Fo( Hz ) | fr( Hz ) | R1( kohm ) | Co( pF ) | C1( fF ) | Q( k ) |
|------------------|-----|----------|----------|----------|------------|----------|----------|--------|
| VT-200<br>12.5pF | 1   | 12.5     | 32768.11 | 32765.28 | 27.4       | 0.91     | 2.319    | 76.5   |
|                  | 2   | 12.5     | 32768.09 | 32765.24 | 26.9       | 0.89     | 2.333    | 77.4   |
|                  | 3   | 12.5     | 32768.34 | 32765.45 | 29.9       | 0.93     | 2.368    | 68.6   |

## [IC Test Data : IC samples Rd=0 ohm,Cg=20pF,Cd=20pF at 25°C]

| Vcc( V ) | IC samples | Fosc( Hz ) | df / f( x10 <sup>-6</sup> ) | DL(x10 <sup>-6</sup> W) | -RL  ( kohm ) | Vstart( V ) | Ts(sec) |
|----------|------------|------------|-----------------------------|-------------------------|---------------|-------------|---------|
| 5.0      | TYP        | 32768.24   | -3.18                       | 0.30                    | 944           | 1.10        | 0.54    |
|          | W#02-049   | 32768.24   | -3.03                       | 0.35                    | 944           | 1.18        | 0.47    |
|          | W#04-044   | 32768.24   | -3.09                       | 0.32                    | 944           | 1.02        | 0.47    |
|          | W#07-048   | 32768.24   | -3.12                       | 0.34                    | 944           | 1.12        | 0.54    |
|          | W#13-047   | 32768.24   | -3.03                       | 0.34                    | 944           | 1.19        | 0.50    |
| 3.3      | TYP        | 32768.22   | -3.58                       | 0.30                    | 944           | 1.10        | 0.56    |
|          | W#02-049   | 32768.22   | -3.64                       | 0.35                    | 944           | 1.18        | 0.50    |
|          | W#04-044   | 32768.23   | -3.33                       | 0.32                    | 944           | 1.02        | 0.57    |
|          | W#07-048   | 32768.23   | -3.48                       | 0.34                    | 944           | 1.12        | 0.56    |
|          | W#13-047   | 32768.23   | -3.33                       | 0.34                    | 944           | 1.19        | 0.56    |

Remak ( see figure 3 )

$$F_o = f_r \times \{ C_1 / ( 2 \times ( C_o + C_L ) + 1 ) \} \text{ ( Hz )}$$



- Fo : Load resonance frequency
- fr : Resonance frequency
- R1 : Motional resistance
- C1 : Motional capacitance
- Co : Shunt capacitance
- CL : Load Capacitance

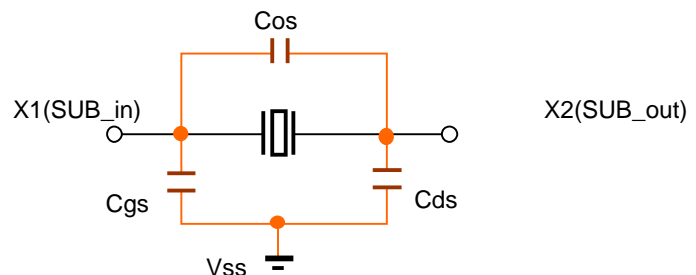
Figure 3 Equivalent circuit of crystal unit, and CL

Remak ( see figure 4 )

Approximate formula of the load capacitance of the circuit CL.

$$C_L = C_g \times C_d / ( C_g + C_d ) + C_s \text{ ( pF )}$$

Where Cs Stands for stray capacity of the circuit.



- Cos : X1\_X2 Stray capacitance
- Cgs : X1\_Vss Stray capacitance
- Cds : X2\_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.