

Introduction

The intense heavy ion environment encountered in space applications can cause a variety of transient and destructive effects in analog circuits, including single-event latchup (SEL), single-event transient (SET) and single-event breakdown (SEB). These effects can lead to system-level failures including disruption and permanent damage. For predictable, reliable space system operation these components have to be formally designed and fabricated for SEE hardness, followed by detailed SEE testing to validate the design. This report discusses the results of SEE testing of the Intersil IS-1845ASRH Pulse Width Modulator.

Product Description

Pulse width modulation (PWM) controllers are commonly used in various switching mode power supplies. These devices offer special features designed to optimize the controller while minimizing the need for external circuitry. The devices generally have an error amplifier, an oscillator circuit, an output circuit and an internal reference circuit. In the IS-1845ASRH there is also a current limit comparator and an under voltage lockout (UVLO). The current limit comparator is used to limit the duty cycle if an overcurrent condition arises. The UVLO circuit is used to bring the PWM into regulation after it has reached a designated threshold value.

The IS-1845ASRH is fabricated using the Intersil Corporation dielectrically isolated hardened silicon gate (RSG) process. This is a BiCMOS flow optimized for power management functions and features complementary high-voltage MOS and bipolar devices as well as various passive components. The IS-1845ASRH is SEL immune by construction and is hardened to a total ionizing dose level of 300krad(Si). The DI process enables vertical PNP and NPN bipolar devices, resulting in greatly enhanced low dose rate (ELDRS) performance.

SEE Test Objectives

Non-hardened SEU PWMs have been tested previously under SEE conditions. The effective LET of commercial 1845A components has been demonstrated to be 15 MeV/mg/cm². The Intersil's IS1845ASRH was designed for an effective LET of 45 MeV/mg/cm². Single-event effects were

simulated by the injection of charge corresponding to the 45MeV/mg/cm^2 objective LET into critical nodes of the circuit and then monitoring upset levels. If a simulated upset occurred in the CMOS section of the design, device sizes were increased appropriately to minimize the effect; simulations were then rerun. In parts of the bipolar section where an upset occurred (such as the error amp, voltage regulator and comparator), redundant paths were used to negate the effects of a transient pulse.

SEE Test Procedure

The goal of this work was to determine the vulnerability of the IS-1845ASRH in a radiation environment. The PWM was tested for single event effects at the Cyclotron Institute at Texas A&M University using Au ions ($\text{LET}=89.1\text{MeV/mg/cm}^2$) and Kr ions ($\text{LET}=35.0\text{MeV/mg/cm}^2$).

At the TAMU facility, all SEE testing is done outside the chamber. The device under test was mounted in the beam line and bombarded with heavy ions of the appropriate species. The parts were assembled in dual in-line packages with the metal lid removed for beam exposure. The beam was directed on to the exposed die and the beam flux, beam fluence and errors in the device outputs were measured. The outputs measured were the output of the device, the RT/CT pin, the error amplifier output and the voltage reference output. The devices were configured such that they are functioning with a steady state output, with the inputs to the controller biased at a fixed value so that the device puts out typical waveforms at a single frequency.

The tests were controlled remotely from the control room. All input power was supplied from portable power supplies connected via cable to the DUT. The supply currents were monitored along with the device outputs. All currents were measured with digital ammeters while all the output waveforms were monitored on a digital oscilloscope for ease of identifying the different types of SEE which the part displayed. Events were captured by triggering on changes in the output pulses in time such as changes in duty cycle or phase shifts.

The test circuit consisted of a 10k (RT) resistor tied from the RT/CT pin to VREF, a 470pF (CT) capacitor from RT/CT pin to GND, a 1nF load capacitor on the OUTPUT pin, the COMP pin tied to VFB, and a 4.7k/1k resistor divider network across ISENSE from the OUTPUT pin. This resistor divider network reduced the free-running duty cycle down from 50% to 20%, while the RT/CT combination gave a 310kHz ramp waveform.

SEE Test Results

Using Au ($\text{LET}=89.1\text{MeV/mg/cm}^2$) as a first ion at a fluence of 1×10^6 ions/ cm^2 , the total number of upsets that occurred was 5, giving a capture cross-section of $5 \times 10^{-6} \text{ cm}^2$. This capture cross-section is approximately 2.5 orders of magnitude smaller than the equivalent commercial part.

In testing of the IS-1845ASRH several different SEE phenomena were observed, including clock upsets in which the ramp would upset, discharge and start a new cycle. This also was related to a phase shift on the output. Additionally, a second condition was observed that resulted in a dropped pulse on the output without a disturbance on the clock. Most likely this was caused in the CMOS digital circuitry. The last case was an observed 'stretched pulse', which would be considered a change in duty cycle. As none of these events lasted longer than a single clock cycle, effects on the system would be minimal.

There were no observed upsets using Kr ($\text{LET}=35\text{MeV/mg/cm}^2$) at a fluence of 1×10^6 ions/ cm^2 .

None of the tests resulted in any permanent damage or parametric degradation, and no latchup effects were observed.

Conclusions

As expected, we observed upsets at the higher LET value ($\text{LET}=89.1\text{MeV/mg/cm}^2$) using Au as an ion source. These upsets resulted in perturbations in oscillator frequency, phase shift and duty cycle changes. The calculated capture cross section was $5 \times 10^{-6} \text{ cm}^2$. None of these upsets lasted longer than a clock cycle before recovery and hence would not cause system-level effects. These findings were similar to what has occurred in the competitor part at substantially lower LET values. There were no indications of upset using Kr at $\text{LET}=35\text{MeV/mg/cm}^2$ as an ion source.

No destructive single-event effects or latchup were observed using Au at the maximum LET of 89.1MeV/mg/cm^2 .