9DBL0242 Evaluation Board

This document provides an overview of the 9DBL0242 evaluation board's (EVB) connections/functions and describes how to use the PCIe Clock/Buffer SMBus Register Tool to read and write register values to the device.

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1. Evaluation Board (EVB) Overview

Note: For screen captures or images denoting IDT: IDT was acquired by Renesas.

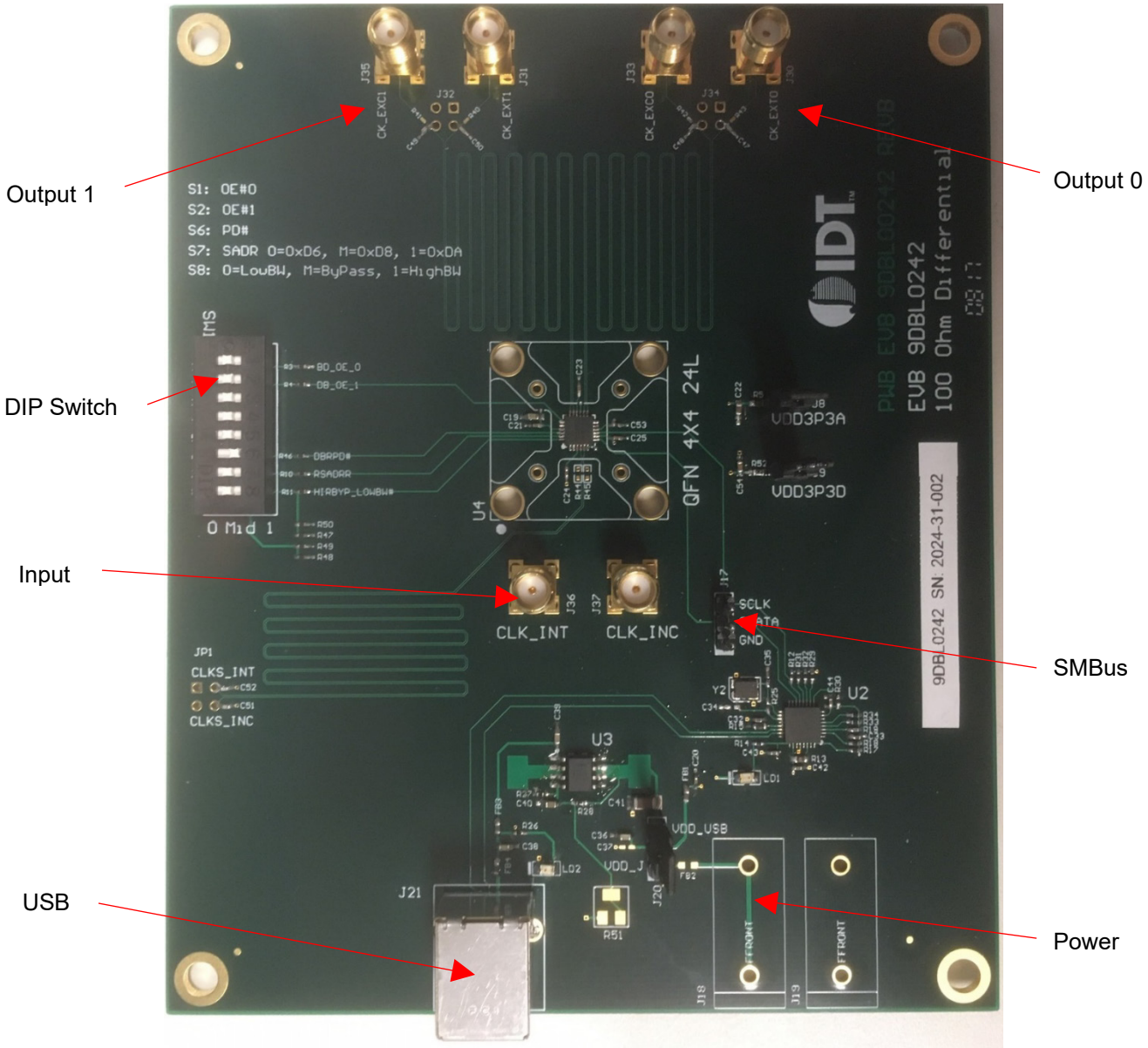

Figure 1. 9DBL0242 Evaluation Board (EVB)

1.1 EVB Connector Descriptions

Refer to Figure 1 and Table 1 for the 9DBL0242 EVB connectors and their descriptions.

Table 1. EVB Connectors and Descriptions

Label	Description
Output 0/Output 1	Differential output clock SMA connectors. Terminate into high impedance (preferred for LP-HCSL) or 50Ω for 9DBL0242 (42.5Ω for 9DBL0252) for double-terminated, with half the voltage swing.
DIP Switch	Having all switches in the default “Mid” position: **SW1**: OE#0 – Output Enable (active-low) for clock output 0; “-“ for on, “+” for off. **SW2**: OE#1 – Output Enable (active-low) for clock output 1; “-“ for on, “+” for off. **SW6**: PD# – Power Down (active-low); “-“ for off, “+” for on. Refer to the Power Management section of the 9DBL02x2/9DBL04x2/9DBL06x1/9DBL08x1C datasheet. **SW7**: S_ADR_tri – SMBus address selection; “-“ for 0xD6 (0x6B), “Mid” for 0xD8 (0x6C), “+” for 0xDA (0x6D). Refer to Table 20 “SMBus Address Selection” of the datasheet. **SW8**: ZDB (PLL) operating mode – “-“ for low bandwidth PLL mode, “Mid” for bypass (fan-out buffer) mode, “+” for high bandwidth PLL mode. Refer to Table 17 “ZDB (PLL) Operating Mode” of the datasheet.
Input	Differential input clock SMA connectors, LP-HCSL levels. For bench testing, use a 100MHz differential square wave, 0V to 1.0V from a signal generator with a 50Ω output impedance.
USB	A USB 2.0 type A to type B cable connecting to the computer. This supplies power to the board and allows SMBus connectivity to the 9DBL0242 device via the FT4222 USB-to-SMBus .
SMBus	Use this header to connect directly to the SMBus from a bus master or bus spying tool. For normal operation with a USB connection, J17 can be left unconnected.
Power	Jumper J20 is set to the VDD_USB side to power the board from USB 5V through the on-board 3.3V regulator. Jumpers J38 and J39 must be installed to power the 9DBL0242 device.

2. Using the ClockCtl Tool

1. Prior to running the ClockCtl tool, download and run the **CDM212364_Setup.exe** file from FTDI Chip to install the D2XX FTDI drivers.
2. Download the ClockCtl Tool.

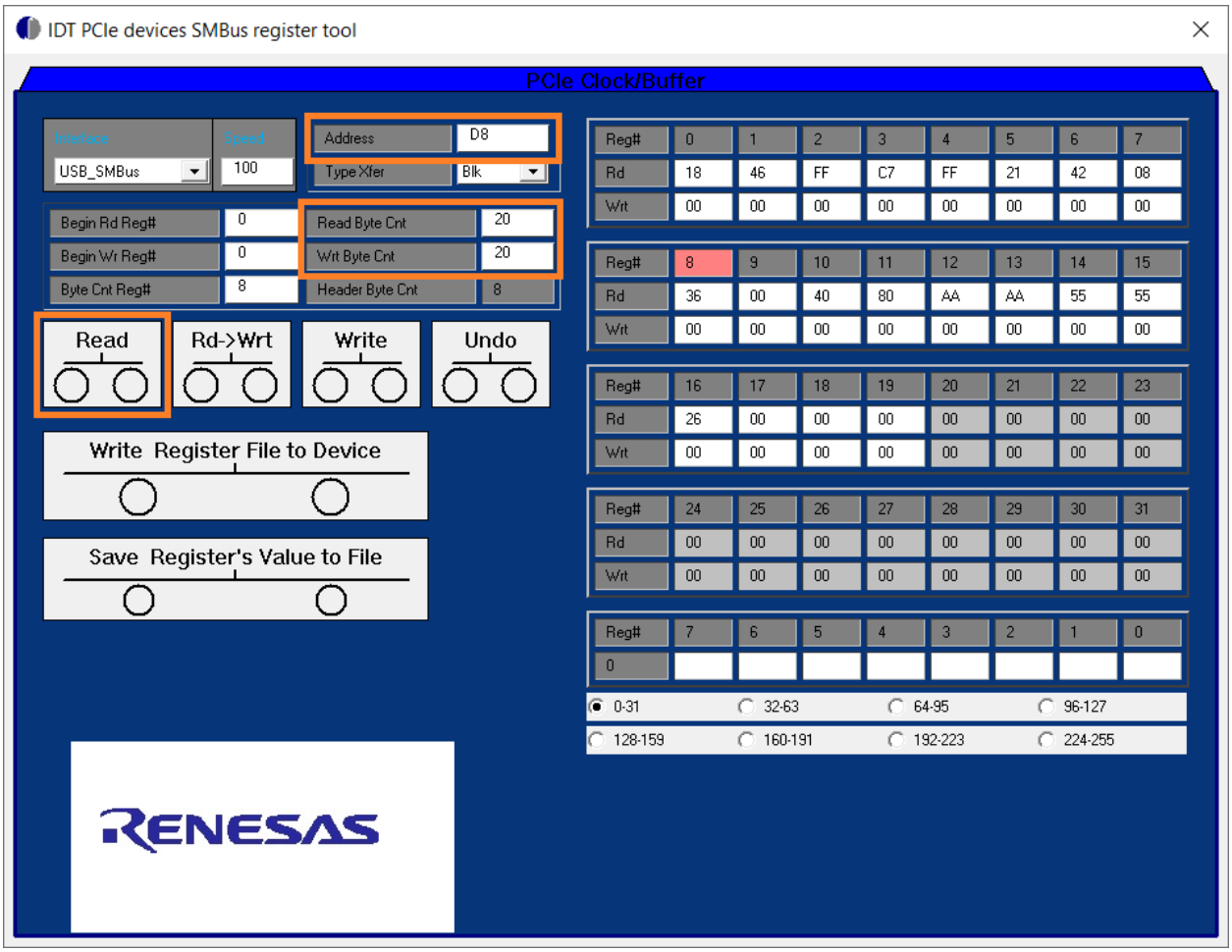

Figure 2. PCIe Devices SMBus Register Tool Window – Address Settings

3. Connect to the board with the provided USB cable.
4. Set the address according to the S_ADR_tri (SW7) DIP switch setting.
5. Enter **20** for the number of bytes to read and write (for register bytes 0 to 19).
6. Click the **Read** button to read the device registers into the ClockCtl tool's "Rd" values.

For this example, alter bits {1, 0} of register byte 1 (from Table 22 of the 9DBL02x2/9DBL04x2/9DBL06x1/9DBL08x1C datasheet).

Table 22. Byte 1: PLL Operating Mode and Output Amplitude Control

Byte 1	Bit	7	6	5	4	3	2	1	0
	Function	PLL Mode Readback		Enable software PLL Mode control	Software PLL Mode Control [1]		-	Output Amplitude	
	Type	R	R	RW	RW	RW	-	RW	RW
	Definition	See Table 17 (ZDB Operating Mode)		0 = B1[7:6] sets PLL Mode 1 = B1[4:3] sets PLL Mode	See Table 17 (ZDB Operating Mode)		Reserved	00 = 0.60V 01 = 0.68V 10 = 0.75V 11 = 0.85V	
All Devices	Name	PLLrbk1	PLLrbk0	PLLmdctrl	PLLmd1	PLLmd0	-	Amp1	Amp0
	Default	Latch	Latch	0	0	0	1	1	0

1. B1[5] must be set to a 1 for these bits to have any effect on the part.

Figure 3. Register Byte 1 Output Amplitude Settings

Read byte 1: 0x46 = 0100_0110

Set byte 1: 0100_0100 = 0x44

Set byte 1: 0100_0101 = 0x45

Set byte 1: 0100_0110 = 0x46

Set byte 1: 0100_0111 = 0x47

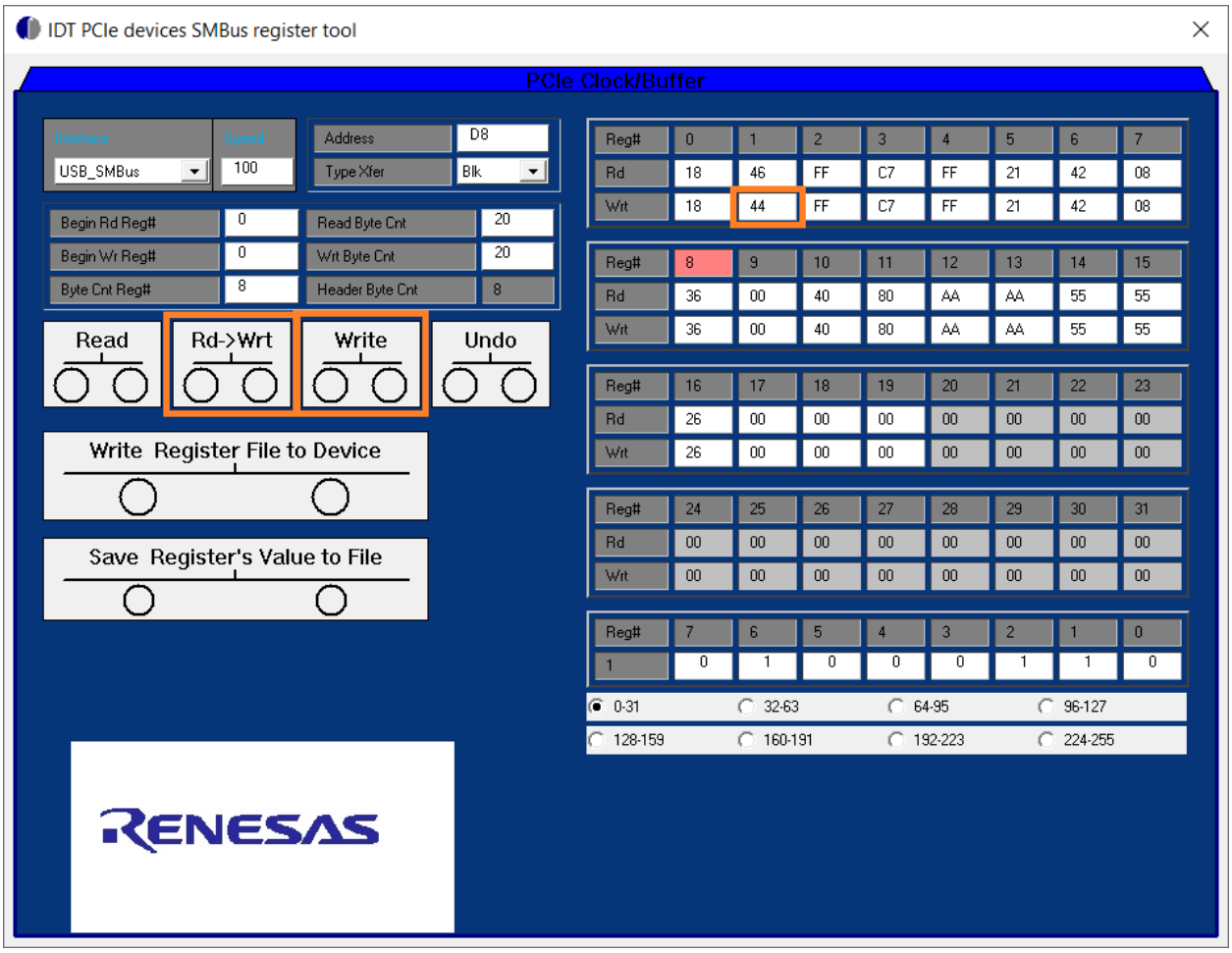

Figure 4. Copying the Previously Read (Rd) Values into the Written (Wrt) Values

7. Click the **Rd->Wrt** button to copy the values previously read (Rd) from the device into the values to be written (Wrt).
8. Enter the desired new register value. For this example, 0x44 into register byte 1.
9. Click the **Write** button to write the “Wrt” values to the device.

3. Oscilloscope Results

The oscilloscope capture in Figure 5 shows the output swing for output swing settings (register byte 1, bits [1, 0]) of [0, 0], [0, 1], [1, 0] and [1, 1].

Figure 5. Oscilloscope Results of Output Swing

4. Revision History

Revision	Date	Description
1.00	Aug 19, 2024	Initial release.

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