



Report No. MCR-25-0158
Date: March 31, 2025

RENESAS SEMICONDUCTOR RELIABILITY REPORT

DEVICE: RAJ2800044H12HPF

APPLICATION: Automotive

Quality Assurance Div.
Renesas Electronics Corporation

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Q100 Qualification Test Result for RAJ2800044H12HPF

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
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TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS

PC	A1	JESD22 A113 J-STD-020	Preconditioning: (Test @ Rm) SMD only; Moisture Preconditioning for THB, AC, TC, PTC; Peak Reflow Temp = 260°C	Min.MSL = 1			MSL = 1	
THB	A2	JESD22 A101	Temperature Humidity Bias: (Test @ Rm/Hot) Ta=85°C RH=85%, Specified Bias, 1000h	3	77	231	0 of 231	
AC	A3	JESD22 A102	Autoclave: (Test @ Rm) Ta=121°C RH=100%, 96h	3	77	231	0 of 231	
TC	A4	JESD22 A104	Temperature Cycle: (Test @ Hot) Ta=-65°C to +150°C, 500cycles	3	77	231	0 of 231	
PTC	A5	JESD22 A105	Power Temperature Cycle: (Test @ Rm/Hot)	1	45	45	0 of 45	IOL test is performed instead of PTC. IOL: Intermittent Operational Life Ta=25°C, Delta T=100°C 10kcycles ON/OFF = 3min
HTSL	A6	JESD22 A103	High Temperature Storage Life: (Test @ Rm/Hot) Ta=150°C, 1000h	1	45	45	0 of 45	

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
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TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS

HTOL	B1	JESD22 A108	High Temp Operating Life: (Test @ Rm/Hot/Cold) Ta=150°C, Specified Bias, 1000h	3	77	231	0 of 231	N/A
ELFR	B2	AEC-Q100-008	Early Life Failure Rate: (Test @ Rm/Hot) Ta=150°C, Specified Bias, 24h	3	800	2400	0 of 2400	N/A
EDR	B3	AEC-Q100-005	NVM Endurance & Data Retention Test: (Test @ Rm/Hot)	3	77	231	-	N/A Nonvolatile memory only.

TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS

WBS	C1	AEC-Q100-001	Wire Bond Shear Test: (Cpk > 1.67)	1	5 parts Min.	30 bonds	0 of 30	Cpk > 1.67
WBP	C2	Mil-STD-883 Method 2011	Wire Bond Pull initial: (Cpk > 1.67)	1	5 parts Min.	30 bonds	0 of 30	Cpk > 1.67
SD	C3	JESD22 B102	Solderability: (>95% coverage) Steam aging: 8h	1	15	15	0 of 15	>95% coverage
PD	C4	JESD22 B100, JESD22 B108	Physical Dimensions: (Cpk > 1.67)	3	10	30	0 of 30	Cpk > 1.67
SBS	C5	AEC-Q100-010	Solder Ball Shear: (Cpk > 1.67)	3	10parts Min.	150 balls	-	N/A BGA package only.
LI	C6	JESD22 B105	Lead Integrity: (No lead cracking or breaking); Through-hole only	1	10parts Min.	10 leads	-	N/A Through-hole device only.

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
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TEST GROUP D – DIE FABRICATION RELIABILITY TESTS

a	D1	JESD61	Electromigration:	-	-	-	PASS	Confirmed by TEG
TDDB	D2	JESD35	Time Dependent Dielectric Breakdown:	-	-	-	PASS	Confirmed by TEG
HCI	D3	JESD60 & 28	Hot Carrier Injection:	-	-	-	PASS	Confirmed by TEG
NBTI	D4	JESD90	Negative Bias Temperature Instability:	-	-	-	PASS	Confirmed by TEG
SM	D5	JESD61,87 & 202	Stress Migration:	-	-	-	PASS	Confirmed by TEG

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
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TEST GROUP E- ELECTRICAL VERIFICATION

TEST	E1	User/Supplier Specification	Pre and Post Stress Electrical Test:	All	All	All	0 of All	Refer to the each test items
HBM	E2	AEC-Q100-002	Electrostatic Discharge, Human Body Model: (Test @ Rm/Hot); (2KV HBM)	1	3	3	0 of 3 ESD Level= HBM: 2	HBM: 2KV Pass HBM Classification follows ANSI/ESDA/JEDEC JS-001-2017
CDM	E3	AEC-Q100-011	Electrostatic Discharge, Charged Device Model: (Test @ Rm/Hot); (750V corner leads, 500V all other leads)	1	3	3	0 of 3 ESD Level= CDM: C2a	Corner leads: 750V Pass All other leads: 500V Pass CDM Classification follows AEC-Q100-001 Rev. D
LU	E4	AEC-Q100-004	Latch-Up: (Test @ Rm/Hot)	-	-	-	-	N/A
ED	E5	AEC-Q100-009	Electrical Distributions: (Test @ Rm/Hot/Cold) (Cpk > 1.67)	3	30	90	0 of 90	Number of lots is fixed with customer's approval. Cpk > 1.67
FG	E6	AEC-Q100-007	Fault Grading:	-	-	-	Fault Grade ≥ 98%	
CHAR	E7	AEC-Q003	Characterization: (Test @ Rm/Hot/Cold)	-	-	-	PASS	Completed in accordance with the Renesas standard procedure.
EMC	E9	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions): <40dBuV at 150KHz-1GHz	-	-	-	-	N/A
SC	E10	AEC Q100-012	Short Circuit Characterization	3	10	30	PASS	Cold Repetitive Short Circuit Test TSC 0/30 Cold Repetitive Short Circuit Test LSC 0/30
SER	E11	JESD89-1 JESD89-2 JESD89-3	Soft Error Rate	1	3	3	-	N/A Device with memory only.
LI	E12	AEC-Q005	Lead (Pb) Free: (see AEC-Q005)	-	-	-	-	Solderability: See SD (C3) result. Solder heat resistance: N/A (Wave Solder is Not recommended.) Whisker: Performed on product TEG with test method based on JESD201

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
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TEST GROUP F – DEFECT SCREENING TESTS

PAT	F1	AEC-Q001	See AEC-Q001. This is highly recommended by Automotive Electronic Council to institute.	-	-	-	-	Apply to mass production according to Renesas standard procedure.
SBA	F2	AEC-Q002	See AEC-Q002. This is highly recommended by Automotive Electronic Council to institute.	-	-	-	-	Apply to mass production according to Renesas standard procedure.

·Calculation method of standard failure rate

Operating reliability is decided by inherent reliability of device and environment condition of use (See below).

·Calculation method of standard failure rate (λ)

$$\lambda = \lambda_b \times \pi T \quad (\text{fit})$$

①Basic failure rate(λ_b)
DEVICE: RAJ2800044H12HPF λ_b : 3.7 (fit)

②Temperature parameter (πT)

$$\pi T = \exp \left(11600 \times E_a \times \left(\frac{1}{273+55} - \frac{1}{273+T_a} \right) \right)$$

E_a : 0.7eV (Activation energy)
 T_a : ambient temperature

πT simplified chart										
Ta(j)	40	55	60	65	70	75	80	90	100	110
πT	0.31	1.00	1.45	2.08	2.95	4.15	5.77	10.88	19.82	35.00

③MTTF (Mean Time to Failure)

$$MTTF = \frac{1}{\lambda}$$

·Confidence level 60% ·Standard temperature $T_a = 55^\circ\text{C}$ for LSI devices