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V850E2/PJ4-E Product Features

Features	V850E2/PJ4-E
Product name	uPD70F3598
Operating voltage	5.0 V/1.2 V
Operating clock	Max. 128 MHz (CPUPLL)
Ambient temperature	-40 to +125 degrees
CPU core	V850E2M
CPU instruction	98 instructions / 73 instructions (FPU)
Internal ROM	1 MB
Internal RAM	80 KB
Cache	8 KB/2-way associative
Peripherals	Timer functions • 16-bits counter × 16 channels timer array unit A (TAUA) × 2 units • 32-bits counter × 4 channels timer array unit J (TAUJ) × 1 unit • Motor control timer (TSG2) × 2 units • PWM output timer pattern buffer for resolver excitation signal (TPBA) × 1 unit • Encoder timer (ENCA) × 2 channels • OS timer (OSTM) × 2 units • Window watchdog timer (WDTA)
	Serial interface • Asynchronous serial interface H (UARTH) × 3 channels • Clocked serial interface G (CSIG) × 3 channels • Clocked serial interface H (CSIH) × 1 channel • CAN controller (FCN) × 3 channels

Features	V850E2/PJ4-E
	Resolver sensor interface × 1 channel
	A/D converter • 10/12-bits resolution × 22 channels (S/H 6 channels + 16 channels) • 10/12-bits resolution × 10 channels (S/H 4 channels + 6 channels)
	Peripheral interconnection (PIC) × 1 unit
	Safety functions • Flash memory ECC error detection • RAM ECC error detection • Clock monitor • Built-in self test (BIST) • Safety guardian (SGA)
	On-chip debug (Nexus) × 1 channel
	DMA controller (8 channels), DTS controller (channel free）
Package	144-pin HLQFP (20 mm × 20 mm) 0.5 mm pitch