**September 29, 2011**

## Product Specifications of the SH7769 SoC

| Function | SH7769 Specification |
|---|---|
| Part number | R8A77690JBG |
| Power-supply voltage | 1.275 V (internal) / 3.3 V, 1.8 V, 1.5 V (external) |
| Operating frequency | 533 MHz / 400 MHz |
| Performance | 959 MIPS, 3.7 GFLOPS (@533 MHz) |
| CPU core | SH-4A core |
| On-chip RAM | ILRAM: 16 Kb + OLRAM: 16 Kb |
| Cache memory | 32 Kb instruction / 32 Kb data isolation × 2, 4-way associative, cache coherency support |
| External memory | DDR-I/F: DDR3-SDRAM (DDR1067/800) 16-bit bus (max. 1067 M word/sec) |
| | Local bus: 32-bit bus (67/50 MHz). SRAM and ROM are directly accessible |
| Local bus | Address space: 64 Mb × 3 |
| Major on-chip peripherals | 3D graphic engine SGX530 (OpenGLES 2.0) |
| | Display unit × 2-system output (RGB888 + LVDS output) |
| | LVDS interface (TIA/EIA-644-compliant, 4 pairs) |
| | Dynamic range compression of resolution |
| | Video input interface × 2 ch |
| | Analog composite video input × 1 ch |
| | Display out compare unit × 2 ch |
| | Distortion compensation unit (IMR-X) × 1 ch |
| | VIN/VDEC linked distortion compensation unit (IMR-LSX) × 1 ch |
| | SD host interface × 2 ch |
| | MMC interface × 1 ch |

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|---|---|
| | USB 2.0 host (× 2 ch), function (× 1 ch, common channel with the host) interface |
| | Dedicated DMAC × 35 ch |
| | Controller area network (CAN) interface × 2 ch |
| | Media local bus (MLB) interface × 1 ch |
| | Sound interface × 3 ch |
| | Serial communication interface (SCIF) × 3 ch |
| | I2C bus interface × 1 ch |
| | Serial peripheral interface (HSPI) × 2 ch |
| | PWM timer × 4 ch |
| | Watchdog timer × 1 ch |
| | Timer × 9 ch |
| | Interrupt controller (INTC) |
| | Clock oscillator (CPG): on-chip PLL |
| | On-chip debugging function |
| | Temperature sensor |
| Low-power consumption modes | Sleep mode |
| | Module standby (Clock halt in each module) |
| | DDR-SDRAM power-supply backup mode |
| Package | 496-pin BGA (21 mm × 21 mm, 0.8-mm pitch) |