RENESAS

August 28, 2014

Product Specifications of the R-Car V2H SoC

Item	Specification
Product #	R-Car V2H (R8A7792)
Power supply voltage	3.3/1.8V (IO), 1.5/1.35V (DDR3), 1.03V (Core)
CPU Core	ARM®Cortex™-A15 dual core
Maximum operating frequency	1.0 GHz
Processing performance	7000 DMIPS
Cache memory	L1 I/D cache 32/32 Kbytes, L2 cache 1 MByte L1D cache and L2 cache with ECC
External memory	DDR3-SDRAM can be connected directly Data bus width: 32 bits × 1 ECC
Expansion bus	Flash ROM and SRAM Data bus width: 8/16 bit
Image recognition	Renesas image recognition core IMP-X4
IMR dedicated to viewpoint conversion	Renesas Rendering core IMR-LSX3, 6 channels Reads data from the external memory or from the path directly connected to VIN H.264/JPEG decoder and outputs data in which distortion was corrected to the external memory Renesas Rendering core IMR-LX3, 1 channel Corrected to external memory
Video input (VIN)	PowerVR Series 5 SGX531 1 (3D)
	Graphics core (2D)
Video input (VIN)	6 channels (max. 12-bit serial YCbCr422) or 2 channels (max. 12-bit parallel YCbCr422) 1 channel and 2 channels each are switchable to either 1.8V IO or 3.3V IO

Item	Specification
Display unit	2 channels (24-bit RGB) Dynamic range compression (DRC)
Network	CAN 2 channels
	Ethernet AVB 1000 Mbps, 100 Mbps, IEEE802.3 PHY
Package	64-pin FCBGA
Supported OS	INTEGRITY® real-time OS from Green Hills Software

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