

October 22, 2014

## Product Specifications of the R-Car E2

Item	Specification	
Product number	R8A7794	
Power supply voltage	3.3/1.8 V (IO), 1.5/1.35 V (DDR3), 1.0 V (Core)	
CPU core	ARM® Cortex™-A7 Dual	SH-4A core
Cache memory	L1 Instruction cache: 32 KB L1 Operand cache: 32 KB L2 Cache: 512 KB	Instruction cache: 32 KB Operand cache: 32 KB
External memory	DDR3-SDRAM Data bus width: 32 bits	
Expansion bus	Flash ROM and SRAM, Data bus width: 8 or 16 bits	
Graphics	PowerVR™ SGX 540	
Video	Display Out × 2 ch (2 ch: RGB888)	
	Video Input × 2 ch	
	Video codec module (H.264/AVC, MPEG-2/4, VC-1)	
	IP conversion module	
	TS Interface × 1 ch	
	Video image processing (color conversion, image expansion, reduction, filter processing)	
	Distortion compensation module (image renderer) × 1 ch	
Audio	Audio DSP	
	Sampling rate converter × 6 ch	
	Serial sound interface × 10 ch	
	MOST DTCP	

Item	Specification
<b>Storage interface</b>	USB 2.0 host interface × 2 ports (wPHY)
	SD host interface × 3 ch (SDXC, UHS-I)
	Multimedia card interface × 1 ch
<b>In-car network and automotive peripherals</b>	Media local bus (MLB) Interface × 1 ch (3-pin interface selectable)
	CAN Interface × 2 ch
	IEBus™ Interface
<b>Security</b>	Crypto engine (AES, DES, Hash, RSA)
	Secure RAM
<b>Other peripherals</b>	DMA controller LBSC DMAC: 3 ch / SYS-DMAC: 30 ch / Audio-DMAC: 13 ch / Audio (peripheral)-DMAC: 29 ch
	32-bit timer × 12 ch
	PWM timer × 7 ch
	I <sup>2</sup> C bus interface × 8 ch
	Serial communication interface (SCIF) × 18 ch
	Quad serial peripheral interface (QSPI) × 1 ch (for boot)
	Clock-synchronized serial interface (MSIOF) × 3 ch (SPI/IIS)
	Ethernet AVB controller (IEEE802.1BA/802.1AS/802.1Qav/IEEE1722, GMII/MII, without PHY)
	Ethernet controller (IEEE802.3u, RMII, without PHY)
	Interrupt controller (INTC)
	Clock generator (CPG) with built-in PLL
	On-chip debugger interface
	<b>Package</b>

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