R-Car V3M, V3H, V3H2 Overview & Block Diagram

Rev.1.0
July 30, 2021

1. Overview

1.1 Introduction

R-Car V3M

- Two 800-MHz Arm® Cortex®-A53 MPCore™ cores,
- 800-MHz Arm® Cortex®-R7 core,
- Memory controller for DDR3L-1600 with 32 bits × 1 channel,
- Image recognition engine (IMP-X5-V3M),
- Image signal processor (ISP),
- Video Output (4 lanes × 1 channel LVDS, 1 channel digital),
- Video Input (4 lanes × 1 channel MIPI-CSI2, 2 channels digital),
- 2 channels FlexRay interface,
- 8 channels 12-bit 1.6 MSps Analog to Digital Converter,
- Supporting metric targets for ASIL B (sensor layer, application processors)

R-Car V3H R-Car V3H2

- Four 1.0-GHz Arm® Cortex®-A53 MPCore™ cores,
- 800-MHz Arm® Cortex®-R7 core,
- Memory controller for LPDDR4-3200 with 32 bits × 1 channel,
- Image recognition engine (IMP-X5-V3H),
- Image signal processor (ISP) × 2 channels,
- Video Output (4 lanes × 1 channel LVDS, 1 channel digital),
- Video Input (4 lanes × 2 channels MIPI-CSI2, 2 channels digital),
- 2 channels FlexRay interface,
- PCI Express interface
- Supporting metric targets for ASIL B (sensor layer, application processors)

R-Car V3H2

- 3.7 TOPS for CNN (Option)
- Supporting metric targets for ASIL C (real time domain) safety goals (Option)

R-CarV3M R-Car V3H R-Car V3H2

- Video processing units,
- CAN interface, and
- EthernetAVB interface.

*: The “DDR3/DDR3L-1856” indicates the DDR3/DDR3L-SDRAM bus interface which operates at a frequency of 928 MHz in this manual.

Note: Arm and Cortex are registered trademark of Arm Limited. All other brands or product names are the property of their respective holders.

1.2 List of Specifications

1.2.1 Arm Core

Item	Description
System CPU Cortex-A53	R-Car V3M • Arm Cortex-A53 Dual MPCore 800Hz • L1 I/D cache 32/32 KBytes, L2 cache 512 Kbytes R-Car V3H R-Car V3H2 • Arm Cortex-A53 Quad MPCore 1.0GHz • L1 I/D cache 32/32 KBytes, L2 cache 1 Mbytes R-Car V3M R-Car V3H R-Car V3H2 • NEON™/VFPv4 supported • Security extension supported • Virtualization supported • Armv8 architecture
Debug and Trace	• JTAG/SWD I/F supported • ETM-A57/A53 supported (each CPU) • ETF 16 KBytes for program flow trace (each cluster)

1.2.2 Arm Realtime Core

Item	Description
Arm Realtime Core Cortex-R7	• Arm Cortex-R7 800 MHz • L1 I/D cache 32/32 Kbytes (ECC) • I-TCM/D-TCM (32/32 Kbytes) (ECC) • Dual Lock-Step supported (safety function) • VFPv3 supported • Armv7 architecture
Debug and Trace	• JTAG/SWD I/F supported • ETM-R7 supported • ETF 4 KBytes for program flow trace

1.2.3 CPU Core Peripherals

Item	Description
Clock Pulse Generator (CPG)	• Generates the clocks from external clock (EXTAL). R-Car V3M — Maximum Cortex-A53 clock: 800 MHz — Maximum Cortex-R7 clock: 800 MHz — Maximum AXI-bus clock: 266 MHz — Maximum SDRAM bus clock: 800 MHz (DDR3L-1600) — Maximum peripheral clock (HPϕ): 133 MHz — Maximum IMP/ISP clock: 400 MHz R-Car V3H R-Car V3H2 — Maximum Cortex-A53 clock: 1.0 GHz — Maximum Cortex-R7 clock: 800 MHz — Maximum AXI-bus clock: 400 MHz — Maximum SDRAM bus clock: 1600 MHz (LPDDR4-3200) — Maximum media clock: 400 MHz R-Car V3M R-Car V3H R-Car V3H2 • System-CPU shut down mode control supported • Module-standby mode supported • Includes module reset registers to control reset operation of individual on-chip peripheral modules
System Controller (SYSC)	• Shuts down and restores power to target modules. Target modules: R-Car V3M — Cortex-A53 (with independent shutting down of CPUs 0, 1 and SCU+L2 cache) R-Car V3H R-Car V3H2 — Cortex-A53 (with independent shutting down of CPUs 0, 1, 2, 3, and SCU+L2 cache) R-Car V3M R-Car V3H R-Car V3H2 — Cortex-R7 — IMP-X5 • Low leakage standby mode supported.
RESET	• Includes one reset-signal external output port for external modules • Includes Boot Address Register etc.
Pin function controller (PFC)	• Setting multiplexed pin functions for LSI pins Function of the LSI pin selectable by setting the registers in the PFC module • Module selection Enable and disable the functions of LSI pins to which pin functions from multiple pin groups are assigned by setting the registers in the PFC module. • Pull-up/down control for each LSI pin On/off and up/down of the pull register on each LSI pin can be controlled by setting the registers in the PFC module.
General-purpose I/O (GPIO)	• General-purpose I/O ports • Supports GPIO interrupts

Item	Description
Thermal sensor / Chip Internal Voltage Monitor (THS/CIVM)	R-Car V3H R-Car V3H2 • 2 channels of thermal sensor R-Car V3M • 1 channel of thermal sensor R-Car V3M R-Car V3H R-Car V3H2 • Programmable 3 temperature level for the sensor, to indicate the temperature level • Interrupt when the temperature reaches programmed

1.2.4 External Bus Module

Item	Description
External Bus Controller for EX-Bus (LBSC)	• EX-BUS interface: max. 16-bit bus • Frequency: 66 MHz or 44.4 MHz • External area divided into several areas and managed — Allocation to space of area 0, area 1. — Area 0 supports 1-MByte memory space (startup mode). — I/F settings, bus width settings, and wait state insertion are possible for each area • SRAM interface — Wait states can be inserted through register settings Period of waiting is set in cycle unit, and the maximum value is 15. — EX_WAIT pin can be used for wait state insertion — Connectable bus widths: 16 bits or 8 bits • Supports external buffer enable/direction control • Supports Burst ROM interface • Supports Byte-control SRAM interface
External Flash Controller	• Supports RPC-IF (Reduced Pin Count interface) flash memory or QSPI flash memory Maximum Frequency 160 MHz (320MB/s) for RPC-IF, 80 MHz (80MB/s)* for QSPI (QSPI0) Dual QSPI operation for two 4-bit serial flash memories is also available; 80 MHz (160MB/s)* for Dual QSPI (QSPI0+QSPI1).
External Bus Controller for LPDDR4/DDR3/DDR3L SDRAM (DBSC4)	R-Car V3H R-Car V3H • 1 channel (32-bit bus mode) • LPDDR4-3200 can be connected directly. Note. The LPDDR4X (JESD209-4-1) is not supported. • Memory Size: Up to 4GB (*) • Auto Refresh/Self Refresh/Partial Array Self Refresh supported • Auto Pre-charge Mode • DDR Back Up supported (*): LPDDR4-SDRAM compliant with JEDEC JESD209-4B. (Supports memory with sizes from 4 Gbits to 16 Gbits.) • Cache memory for DDR-Memory access efficiency • Decompression of lossless compressed image • Memory access protection for secure/safety regions

Item	Description
External Bus Controller for DDR3L SDRAM (DBSC4)	R-Car V3M • 1 channel (32-bit bus mode) • DDR3L-1600 can be connected directly (DDR3 and LPDDR4 are not supported). • Memory Size: Up to 2GB • Auto Refresh/Self Refresh/Partial Array Self Refresh supported • Auto Pre-charge Mode • DDR Back Up supported

1.2.5 Internal Bus Module

Item	Description
AXI-bus	• On-chip main bus — Bus protocol: AXI3 with QoS control R-Car V3H R-Car V3H2 — Frequency: 400 MHz — Bus width: 512 bits/256 bits/128 bits R-Car V3M — Frequency: 266 MHz — Bus width: 256 bits/128 bits/64 bits • On-chip CPU bus R-Car V3M — Bus protocol: AMBA®4 ACE™ and ACE-Lite™ — Frequency: 800 MHz — Bus width: 128 bits R-Car V3H R-Car V3H2 — Bus protocol: AXI3 — Frequency: 800 MHz — Bus width: 128 bits
Direct Memory Access Controller for System (SYS-DMAC)	• 16 channels for TOP domain (SYDM0) • Address space: 4 GBytes on architecture • Data transfer length: Byte, word (2 Bytes), longword (4 Bytes), 8 Bytes, 16 Bytes, 32 Bytes and 64 Bytes • Maximum number of transfer times: 16,777,215 times • Transfer request: Selectable from on-chip peripheral module request and auto request • Bus mode: Selectable from normal mode and slow mode • Priority: Selectable from fixed channel priority mode and round-robin mode • Interrupt request: Supports interrupt request to CPU at the end of data transfer • Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function) • Descriptor function (each channel) supported • MMU (each channel) supported • Channel bandwidth arbiter (each channel)
Boot	• System startup with selectable boot mode at power-on reset • Either external ROM boot (area 0)* or on-chip ROM boot can be selected through MD pin on development chip. • In on-chip ROM boot, RPC-IF or QSPI serial ROM boot is supported. • Program downloaded to internal memory (System RAM) • Autorun function for the downloaded program • Secure boot supported. Integrity check of boot image is proceeded before executing. • On secure chip, boot operation is restricted to on-chip ROM boot mode. • About detail information of BOOT, refer to Section 19 (Boot) and Appendix B (Active sequence).

Item	Description
Realtime Direct Memory Access Controller (RT-DMAC)	• 32 channels for Realtime domain • Address space: 4 GBytes on architecture • Data transfer length: Byte, word (2 Bytes), longword (4 Bytes), 8 Bytes, 16 Bytes, 32 Bytes and 64 Bytes • Maximum number of transfer times: 16,777,215 times • Transfer request: Selectable from on-chip peripheral module request and auto request • Bus mode: Selectable from normal mode and slow mode • Priority: Selectable from fixed channel priority mode and round-robin mode • Interrupt request: Supports interrupt request to CPU at the end of data transfer • Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function) • Descriptor function (each channel) supported • MMU (each channel) supported • Channel bandwidth arbiter (each channel)
IPMMU	• An IPMMU is a memory management unit (MMU) which provides address translation and access protection functionalities to processing units and interconnect networks.
Interrupt Controller (INTC)	INTC-AP (For All Products; for AP-System core Cortex-A57/Cortex-A53)	R-Car V3M — 5 interrupt pins which can detect external interrupts — Max. 480 shared peripheral interrupts supported R-Car V3H R-Car V3H2 — 6 interrupt pins which can detect external interrupts — Max. 384 shared peripheral interrupts supported R-Car V3M R-Car V3H R-Car V3H2 — Fall/rise/high level/low level detection is selectable — On-chip peripheral interrupts: Priority can be specified for each module — 16 software interrupts that have been generated and 6 private peripheral interrupts supported — 32-level priority selectable — Trust Zone supported
Interrupt Controller (INTC)	INTC-RT for RealTime CPU Cortex-R7	R-Car V3M — 5 interrupt pins which can detect external interrupts R-Car V3H R-Car V3H2 — 6 interrupt pins which can detect external interrupts R-Car V3M R-Car V3H R-Car V3H2 — Fall/rise/high level/low level detection is selectable — On-chip peripheral interrupts: Priority can be specified for each module — Max. 384 peripheral interrupts supported
Multifunctional Interface (MFIS)	• Interrupt generation between SYS domain and RT domain • Fifteen external source bits for controlling 32-K types of interrupts • Lock function for exclusive access supported • Error checking function control and arbitrate error signal from other module.

1.2.6 Internal Memory

Item	Description
System RAM	R-Car V3H R-Car V3H2 RAM of 384 KBytes R-Car V3M RAM of 448 Kbytes

1.2.7 Display Unit

Item	Description	
Display Unit (DU)	Display channel	1 channel
	Interface	• LVDS 1 channel • Digital RGB 1channel (8-bit precision for each RGB color)
	LVDS interface (per channel)	• Output: compliant with TIA/EIA-644; five pairs of differential output (four pairs of data and one pair of clock) • Operating frequency: Dotclk 148.5 MHz
	Screen size and number of composite planes per channel	• Maximum screen size: 1920 × 1440 @30fps, 1920 × 1080@60fps • Number of planes specifiable: 5 (VSP2 processing) • Number of planes specifiable: 1 (DU)
	CRT scanning method	Non-interlaced
	Synchronization method	Master
	Internal color palette (VSP2)	• Includes four color palette planes which can display 256 of 260 thousands colors at the same time.
	Output display numbers	• One output channel • 8-bit precision for each RGB color
	Blending ratio settings (VSP2)	Number of color palette planes with blending ratio: 4
	Dot clock	Switchable between external input and internal clock
Video Input Module (VIN)	MIPI-CSI2 interface	R-Car V3M • 1 channel (4lane × 1 channel) R-Car V3H R-Car V3H2 • 2 channels (4-lane × 2 channels) R-Car V3M R-Car V3H R-Car V3H2 • 1.125Gbps/Lane for RAW data (ISP) for R-Car V3M, 1.5Gbps/Lane for RAW data (ISP) for R-Car V3H/V3H_2 RAW8, RAW10*, RAW12*, RAW14* (HDR sensor Input), RAW16* (HDR sensor Input), RAW20* (HDR sensor Input) are supported *: RAW10, RAW12, RAW14, RAW16, and RAW20 can be input only via ISP module. • 1.0Gbps/Lane for RGB/YUV (ISP bypass) YUV422 8/10bit, Embedded 8bit, User Defined 8bit are supported

Video Input Module (VIN)	digital interface	• 2 channels (YCbCr/Raw for ISP) • Dotclk 100 MHz • RAW data input (ISP) • RAW8 / RAW10* /RAW12* are supported *: RAW10 and RAW12 can be input only via ISP module. • RGB/YCbCr input (ISP bypass) ITU-R BT.601 interface: 8-, 10- (same size only (not scaling)), or 12-bit (same size only (not scaling)) YCbCr422 ITU-R BT.656 interface: 8-, 10- (same size only (not scaling)), or 12-bit (same size only (not scaling)) YCbCr422
	Capturing function	R-Car V3M Up to 4 input images can be captured (using VC, DT filtering) R-Car V3H R-Car V3H2 • Up to 6 input images can be captured (using VC, DT filtering)
	Clipping function	R-Car V3M Up to 4096 × 4096 Note: When max size image is input, ISP can't be used. And input frame rate is in accordance with the less than 1.0Gbps/lane (case of using MIPI-CSI2 interface) or dotclk 100 MHz (case of using digital pin). R-Car V3H R-Car V3H2 Up to 4096 × 4096 • Note: When max size image is input, ISP can't be used. And input frame rate is in accordance with the less than 1.5Gbps/lane (case of using MIPI-CSI2 interface) or dotclk 100 MHz (case of using digital pin).
	Output format	R-Car V3M Y: 10bpp, UV: 10bpp R-Car V3H R-Car V3H2 • RGB-565, ARGB-1555, ARGB8888, YCbCr422, RGB888, YCbCr420 YC separation, and extraction of the Y component
IMR-LX4	R-Car V3M • IMR-LX4-V3M • 4 Image Renders for camera image distortion correction application Pixel Performance: 400Mpixel/sec (peak, @400 MHz) per one IMR-LX4-V3M	
	R-Car V3H • IMR-LX4-V3H • 4 Image Renders for camera image distortion correction application • Pixel Performance: 400Mpixel/sec (peak, @400 MHz) per one IMR-LX4-V3H Rotator/Scaler function support (2 channels)	
	R-Car V3H2 • IMR-LX4-V3H • 5 Image Renders for camera image distortion correction application • Pixel Performance: 400Mpixel/sec (peak, @400 MHz) per one IMR-LX4-V3H • Rotator/Scaler function support (2 channels)	

	R-Car V3M R-Car V3H R-Car V3H2 • HDR sensor support • Edge-adaptive de-mosaicking support for RGGB pattern • Edge adaptive de-mosaicking supporting non-Bayer pattern (2 × 2 quadruple pattern) • Edge-adaptive support for RCCB pattern • Color space conversion engine (RGB to Luminance + 2 × Color) LUT based remapping engine before de-mosaicking
Image Signal Processor (ISP)	R-Car V3M R-Car V3H R-Car V3H2 • HDR sensor support • Edge-adaptive de-mosaicking support for RGGB pattern • Edge adaptive de-mosaicking supporting non-Bayer pattern (2 × 2 quadruple pattern) • Edge-adaptive support for RCCB pattern • Color space conversion engine (RGB to Luminance + 2 × Color) • LUT based remapping engine before de-mosaicking R-Car V3M R-Car V3H Maximum resolution: 2560 (w) x 1280 (h) R-Car V3H2 Maximum resolution: 3900 (w) x 2300 (h)

1.2.8 Video Processing

Item	Description
Video Signal Processor (VSPD)	VSPD has the following features. 1 set of VSPD is integrated. (1) Supports Various Data Formats and Conversion — Supports YCbCr444/422/420, RGB, αRGB, αplane — Color space conversion and changes to the number of colors by dithering — Color keying — Supports combination between pixel alpha and global alpha — Supports generating pre multiplied alpha. (2) Video processing — Blending of 5 picture layers and raster operations (ROPs) — Vertical flipping in case of output to memory (3) Direct connection to display module — Supports 2048 pixels in horizontal direction [R-Car V3M/R-Car V3H/V3H2] — Writing back image data which is transferred to Display Unit (DU) to memory (4) Supports DISCOM function
Video Encoding Processor for inter-device video transfer (iVCP1E)	• Low-latency encoder of H.264/AVC High 10 Profile • Input color format: YCbCr 4:2:0 and 4:2:2 • Input bit depth: 8bit, 10bit and 12bit • Encoding color format: YCbCr 4:2:0 • Encoding bit depth: 8bit or 10bit • Performance: 1920 pixels × 1080 lines × 30 frames/second (R-Car V3M) 1920 pixels × 1080 lines × 60 frames/second (R-Car V3H/V3H_2) • Max resolution: 1920 pixels × 1080 lines — Use the software from Renesas to handle iVCP1E functions.

1.2.9 Storage

Item	Description
Multimedia Card Interface (MMC)	R-Car V3M • 1 channel • eMMC 4.5 base, Support HS200 class transfer rate R-Car V3H R-Car V3H2 • 1 channel • eMMC 5.0 base, Support HS400 class transfer rate

1.2.10 Network

Item	Description
CAN-FD	R-Car V3M R-Car V3H • 2 interfaces • 8 Mbps (CAN clock 40 MHz) R-Car V3H2 • 3 interfaces • 8 Mbps (CAN clock 40 MHz)
PCIE Controller	R-Car V3H R-Car V3H2 • PCI Express Base Specification Revision 2.0 • PHY integrated • 2 Lanes × 1 channel
EthernetAVB-IF	• Supports IEEE802.1BA, IEEE802.1AS, IEEE802.1Qav and IEEE1722 functions • Magic packet detection • Supports Reception Filtering to separate streaming frames from different sources • Supports interface conforming to IEEE802.3 PHY RGMII (Reduced Gigabit Media Independent Interface) RGMII v1.3 R-Car V3M R-Car V3H2 • Supports transfer at 1000 Mbps and 100 Mbps. R-Car V3H • Supports transfer at 100 Mbps
FlexRay	• 2 channels • Comply with FlexRay protocol specification v2.1 Revision A • Data transfer rate: up to 10 Mbit/s on each channel

1.2.11 Timer

Item	Description
RCLK Watchdog Timer	• 1 channel • Internal 16-bit watchdog timer operated by RCLK • Programmable overflow time period: more than 1 hour count capable
16-Bit Timer Pulse Unit (TPU)	• 4-channel 16-bit timers • Each channel outputs PWM
System Watchdog Timer	• 1 channel • Internal 16-bit watchdog timer • Programmable overflow time period: more than 1 hour count capable initial counter value 171[s]
Window Watchdog Timer (WWDT)	R-Car V3M • 2 channels R-Car V3H R-Car V3H2 • 5 channels R-Car V3M R-Car V3H R-Car V3H2 • Window watchdog function; Window & 75% interrupt • Generates Reset or NMI on error detection • 3 start mode selectable. (Automatic, Intelligent automatic, software trigger.) • Configuration can be done by configuration terminals information

Item	Description
Compare Match Timer Type0 (CMT0)	• 2 channels • 32-bit timer (16 bits/32 bits can be selected) • Source clock: RCLK clock • Compare match function provided • Interrupt requests
Compare Match Timer Type1 (CMT1)	• 8 channels • 48-bit timer (16 bits/32 bits/48 bits can be selected) • Source clock: RCLK/system clock • Compare match function provided • Interrupt requests
Compare match timer 2 (CMT2)	(same as CMT1)
Compare match timer 3 (CMT3)	(same as CMT1)
System Timer	• 32-bit timer, 1channel (16 bits/32 bits can be selected) • Compare match function provided • Interrupt requests
System up-time clock	• 1 channel • Internal 32-bit timer • Programmable overflow time period: maximum 24 hours
Timer Unit (TMU)	• 15 channels • 32-bit timer • Auto-reload type 32-bit down counter • Internal prescaler • Interrupt request R-Car V3M • 2 channels for input capture R-Car V3H R-Car V3H2 • 3 channels for input capture

1.2.12 Peripheral Module

Item	Description
Secure Engine	R-Car V3M • 2 Cores (1 Core for secure world operation and 1 Core for PKA acceleration) • PKA Engine (RSA, ECC) • Hash Engine (SHA1, SHA2, MD5) • Bulk Encryption Engine (DES, 3DES, AES) • Internal RAM for Secure Engine R-Car V3H R-Car V3H2 • The Intelligent Cryptographic Unit/Master Extension (ICUMXA) is a hardware security module (HSM). • Run the user-defined security services • Supports a block cipher algorithm based on the AES (Advanced Encryption Standard, FIPS PUB 197), supports DMA transfer for AES block data. • Integrates several public key cryptographic algorithms like RSA, ECC. • Integrates an accelerator that supports HASH function based on SHA-1, SHA-224, and SHA-256(Secure Hash Algorithm, FIPS-PUB 180) • Integrates a true random number generator • Exclusive read access and programming access to a specific area of memory
I2C Bus Interface (I2C)	R-Car V3M • 5 channels for LVTTL buffers R-Car V3H R-Car V3H2 • 6 channels for LVTTL buffers R-Car V3M R-Car V3H R-Car V3H2 • NXP I2C bus interface method supported • Master/slave functions • Multi-master functions • Transfer rate up to 400 kbps supported • Programmable clock generation from the system clock • Master and Slave function DMA supported

Item	Description	
Serial communication interface with FIFO (SCIF)	Overall specification	• 4 channels • Asynchronous, clock-synchronized modes • Asynchronous serial communication mode The SCIF performs serial data communication based on a character-by-character asynchronous system. This feature enables serial data communication with standard asynchronous communication chips that support Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communication Interface Adapter (ACIA). There is a choice of eight serial data transfer formats. — Data length: 7 bits or 8 bits — Stop bits: 1 bit or 2 bits — Parity: Even/odd/none — Receive error detection: Parity, framing, and overrun errors — Break detection: A break is detected when a framing error lasts for more than 1 frame length at Space 0 (low level). When a framing error occurs, a break can also be detected by reading the RX pin level directly from the serial port register (SCSPTR). • Clock synchronous serial communication mode The SCIF performs serial data communication synchronized with a clock. This feature enables serial data communication with other LSIs that support synchronous communication. There is a single serial data communication format for clock synchronous serial communication. — Data length: 8 bits — Receive error detection: Overrun errors • Full-duplex communication capability The SCIF has an independent transmitter and receiver that enable simultaneous transmission and reception. The transmitter and receiver both have a 16-stage FIFO buffer structure, enabling continuous serial data transmission and reception. • On-chip baud rate generator, enabling any bit rate to be selected The SCIF enables choice of a clock source for transmission/reception: a clock from the on-chip baud rate generator based on the internal clock or an external clock. • Eight interrupt sources The SCIF has eight types of interrupt sources. receive-data-ready, receive-FIFO-data-full, break, transmit-FIFO-data-empty, transmit-end, receive-error, overrun-error and time-out and enables any of them to be requested independently.
Serial Communication Interface with FIFO (SCIF)	Overall specification	• DMA data transfer When the transmit FIFO register is empty or the receive FIFO register has received data, issuing a DMA transfer request activates the DMA controller (DMAC) to execute a data transfer. • In asynchronous mode using channels 0, 1, 3, and 4, modem control functions (RTS and CTS) are stored. • RTS and CTS are not implement for SCIF2 and SCIF5

Item	Description
	• The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available. • In asynchronous mode, a receive data ready (DR) or a timeout error (TO) can be detected during reception.
Clock-Synchronized Serial Interface with FIFO (MSIOF)	• 4 channels • Internal 32-bit × 64-stage transmit FIFOs/internal 32-bit × 256-stage receive FIFOs • Supports master and slave modes • Internal prescaler • Supports serial formats: IIS, SPI (master and slave modes) • Interrupt request, DMAC request
High Speed Serial Communication Interface with FIFO (HSCIF)	• 4 channels • Asynchronous serial communication mode • Capable of full-duplex communication • On-chip baud rate generator, enabling any bit rate to be selected • Eight interrupt sources • DMA data transfer • Modem control functions (HRTS# and HCTS#) are stored. • The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available. • A receive data ready (DR) or a timeout error (TO) can be detected during reception.
PWM	• 5 channels • High-level width (10 bits) of PWM output can be set. • Output cycle periods (10 bits) of PWM can be set. • Periods in the range from two to 2^{24} × 1023 cycles of the Pϕ clock can be set. • Continuous pulse or single pulse output selectable
Speed-pulse I/F	• 1 channel • 16-bit speed pulse counter • Internal noise filter (low-pass filter) removes chattering and bounce from speed pulses. • The pulse width to be filtered out by the noise filter is selectable by the user. Passing all pulses without filtering can also be selected. • Two types of pulse count register are provided: one for indicating the count in realtime and another for latching the count every 100 ms. • Five types of pulse width measurement registers are provided: two for the elapsed time, one for the pulse width, and two for the observation period. • Counts are incremented in synchronization with the rising edge of the speed pulse.
A/D Converter (ADC) R-Car V3M	• 8 channels for external input • Successive Approximation Register ADC • 12-bit resolution • 1.6 MSps (max) sampling rate • 256 entries FIFO for each channel • DMA support

1.2.13 Special Edition Modules

Item	Description
Image Processing Unit (IMP-X5)	R-Car V3M • IMP-X5-V3M • 4 Image Processor Cores to accelerate functions by optimized hardware operators. • 2 OCV Cores in each 32 parallel operation cores with ISA optimized for image recognition application • 869KB local memory • 1 DMAC for transferring image data from DDR to local memory in IMP-X5-V3M • IMP PSC for image scaling engine R-Car V3H • IMP-X5-V3H • 5 Image Processor Cores + 1 slim Image Process Core to accelerate functions by optimized hardware operators. • 5 OCV Cores in each 32 parallel operation cores with ISA optimized for image recognition application • 2MB local memory • 2 DMAC for transferring image data from DDR to local memory in IMP-X5-V3H • IMP PSC for image scaling engine R-Car V3H2 • IMP-X5-V3H • 5 Image Processor Cores + 1 slim Image Process Core to accelerate functions by optimized hardware operators. • 5 OCV Cores in each 32 parallel operation cores with ISA optimized for image recognition application • 2MB local memory • 3 DMAC for transferring image data from DDR to local memory in IMP-X5-V3H • IMP PSC for image scaling engine
CNN Engine (IMP CNN)	The IMP CNN is an engine to enable a fast execution of a Convolutional Neural Network. It supports up to n* input DMA and m* output DMA channels. Next to the convolution with a size of up to 5x5, optional a Rectified Linear Units(RELU) or pooling over output channels and x/y direction is supported. The IMP CNN supports the following features: • Image format: unsigned 8-bit, signed 8/16-bit • Processing size: Tile size up to 2048 line times 128 pixels • Input channel: Up to n* channel (Input DMA) • Output channel: Up to m* channel (Output DMA) • Convolution size: Up to 5 x 5 • Magnification setting: 1/5, 1/4, 1/3, 1/2, 1, 2, 3, 4, 5 n = 4 R-Car V3M m = 4 R-Car V3H R-Car V3H2 m = 8
Vision IPs(Option) R-Car V3H R-Car V3H2	Vision IPs support stereo vision (estimate disparity from a pair of images), optical flow (optical flow vectors generation from a pair of images), and classifier engines (feature classifier from image). ● 1x STV : High quality Stereo Vision from a pair of images ● 1x DOF : Dense type of Optical Flow vectors generation. ● 5x ACF : Aggregated Channels Features classifier engines

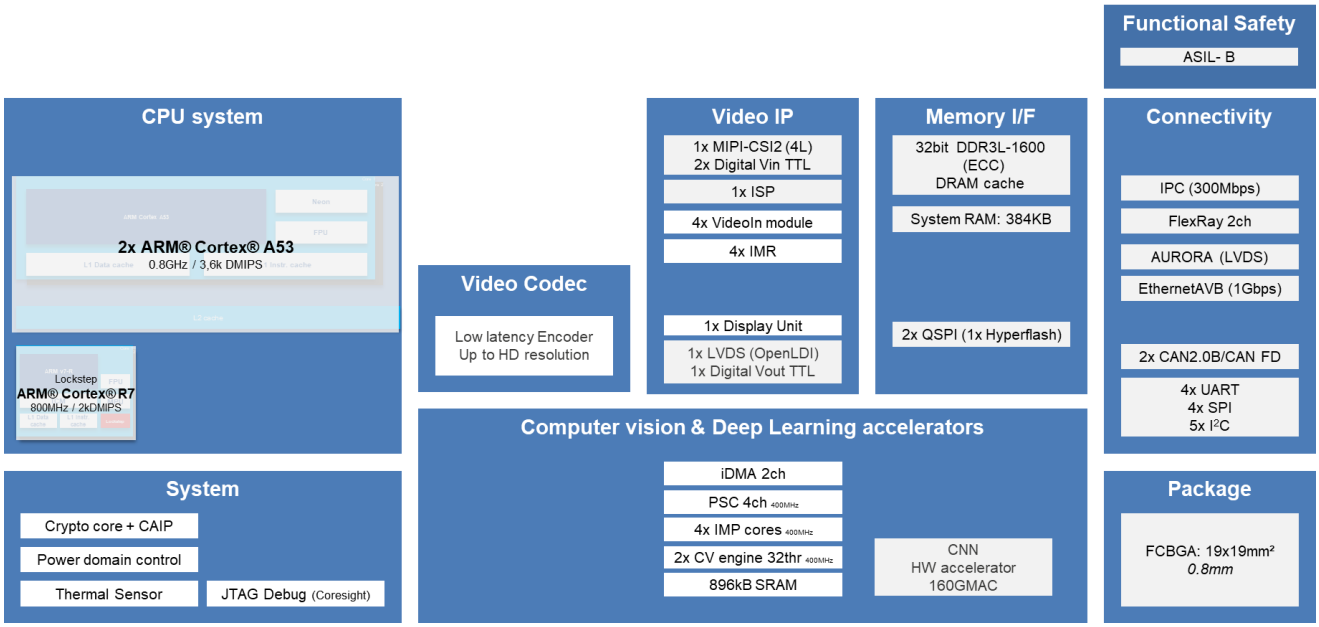
Item	Description
CRC R-Car V3M	The cyclic redundancy check (CRC) block is a function block to generate and check CRC codes of input data via the APB bus. The 32-bit Ethernet polynomial (CRC-32-IEEE 802.3) is used as the generator polynomial. The CRC codes based on this generator polynomial are stored in the register.
Failure Self-Detection Output (RFSO)	This module distinguishes between permanent failure and temporary failure detected by CPU or other important circuit module; moreover, detects time-out error in the process of detecting failures. The failure of CPU or other important circuit will be detected by other circuit (Runtime Test). Also, this module will be used for managing FTTI of this LSI.

1.2.14 Others

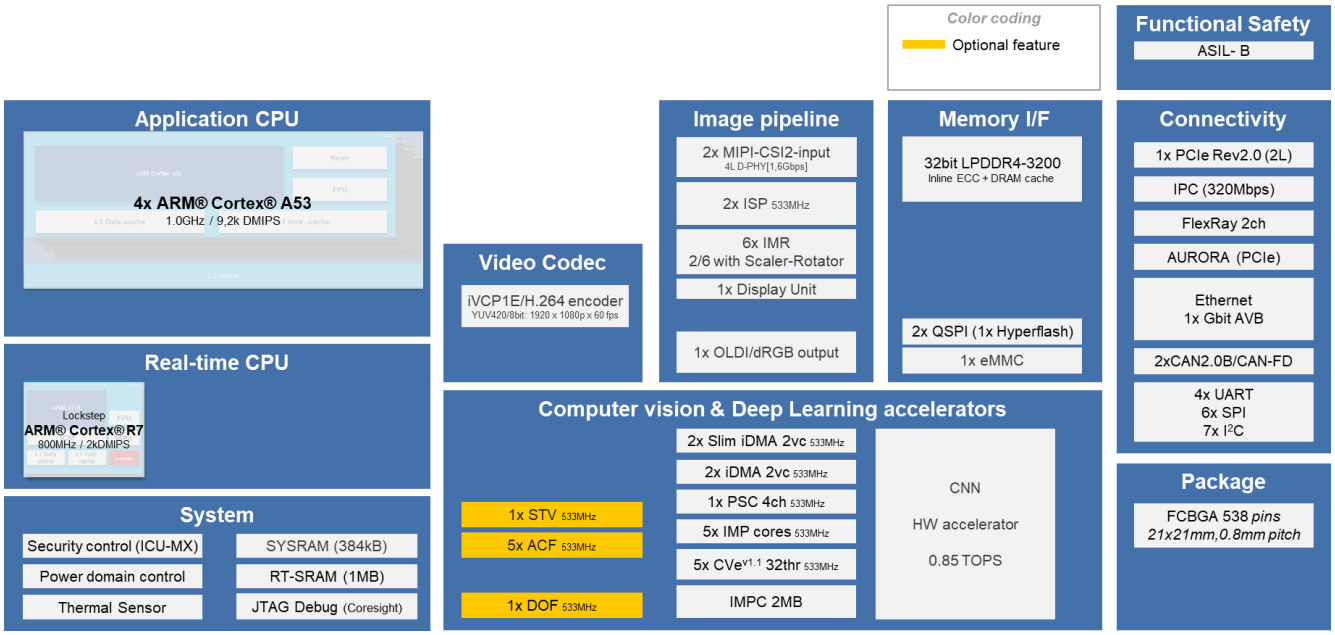
Item	Description
Boundary Scan	• Boundary scan based on IEEE 1149.1 via JTAG interface is supported. Note that some module pins are not available on this boundary scan.

1.3 Block Diagram

1.3.1 R-Car V3M Block Diagram



1.3.2 R-Car V3H Block Diagram



1.3.3 R-Car V3H2 Block Diagram