High Performance Timing Devices for the Most Demanding Applications

IDT Netcom high performance silicon and SAW timing devices deliver exceptional flexibility and dependability, backed by expert service and worldwide support

Introduction

Designers of today's enterprise class networking, communications and advanced computing systems have created the demand for high performance, ultra-dependable clock devices that ensure low jitter, phase noise and skew with minimal process variation.

IDT meets this demand with its highest performing clock devices developed to the exacting specifications of the networking and communications industries under the category IDT **Netcom**. For more information on high performance clocks from IDT visit: **www.IDT.com/go/hiperclocks**.

IDT Netcom Solutions: Robust, Nimble and Reliable

IDT Netcom high performance clocking devices are the choice of advanced-system designers seeking top performance, versatility, selection and value. Featuring over 1,000 silicon timing products, the IDT Netcom portfolio is the industry's largest, offering end-to-end solutions for complete network design. An industry leader in timing device development, IDT is acclaimed for breakthrough products such as its FemtoClock® family, the largest array of general-purpose and application optimized sub-1 picosecond (ps) phase noise devices.

All devices are field proven and compliant with IEEE, Telcordia, ITU, DOCSIS, JEDEC and other standards to ensure high quality, customer confidence and swift time to market. Wafer fabrication, packaging and quality remain stable over time, providing long term availability.

IDT Netcom support professionals provide in-depth application and systems understanding for all of your complex timing needs. Customers can depend on complete clock tree support and service from concept, architecting and prototyping to production and beyond.

FemtoClock® Devices

The largest array of sub-1 picosecond (ps) phase noise devices in the clocking industry lets designers choose their ideal solution

Functions

IDT Netcom FemtoClock devices deliver integrated clock tree functions unavailable in traditional, fixed frequency oscillators:

- Multiple outputs or output styles
- Multiple frequencies produced from a single device
- Frequency margining (under-clocking and over-clocking in small-percentage steps)
- Spread spectrum clocking for EMI reduction

Benefits/Features

- Lower cost than oscillators
- Shorter lead time than oscillators
- Reduced part count

IDT FemtoClock® devices are advanced clock frequency synthesizers employing a simple, low cost, fundamental-mode quartz crystal as the low frequency reference from which they synthesize high quality, high frequency clock signals. Yielding phase noise jitter of less than 1 picosecond (ps) RMS, they are ideal reference clocks for almost any jitter-sensitive application.

FemtoClocks provide output clocks up to 800 MHz. Often used to replace third overtone and high frequency fundamental (HFF, inverted mesa) crystal oscillators or expensive surface acoustic wave (SAW) oscillators traditionally used to generate high frequency clock signals, they are more reliable, cost less, and are more readily available. Unlike fixed frequency oscillators, FemtoClocks are a frequency-synthesis technology capable of multiple clock frequencies and more flexibility in any application. Because FemtoClocks are silicon IC-based clock devices, additional clock tree functions unavailable in a single function fixed frequency oscillator can be integrated into a single device.

The IDT FemtoClock family delivers a wide range of device packages and capabilities, starting with small 8-pin TSSOP devices that provide one clean, low jitter clock signal. Also available are devices with more integrated functions, multiple outputs, multiple frequencies and other more complex programmable synthesis functions. While generally optimized for synthesizing reference clock frequencies commonly used in communication applications, there are also a variety of FemtoClock devices with frequencies useful for CPU, memory, logic and other general-purpose clocking applications, including:

- ASICs, DSPs, CPUs and memory
- Communication (including SONET/SDH and SPI4.2)
- HDTV Video
- Networking (including 1 Gb, 10 Gb, XAUI and 12 Gb Ethernet)
- PCI Express®
- SERDES and PHY Reference Clocks
- Serial Storage (SAS, SATA, Fibre Channel 4, 8 and 10 Gb)
- Wireless Infrastructure (including CPRI, RP3)

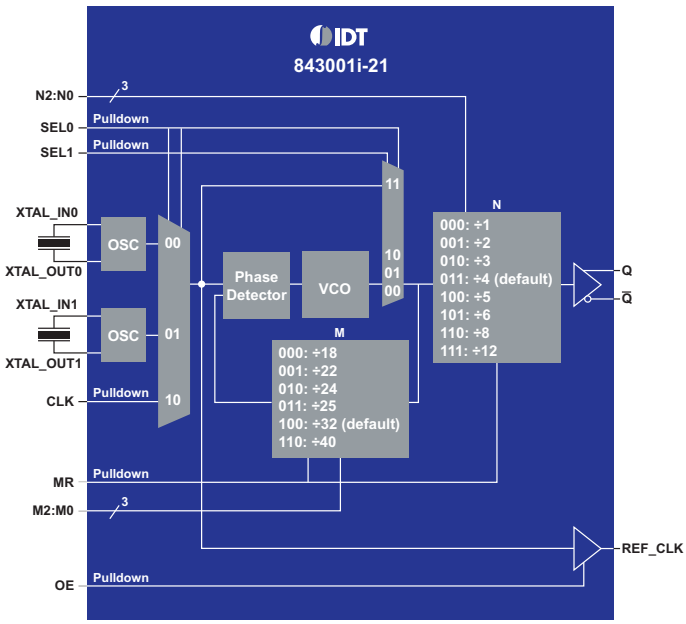


Figure 1. Typical FemtoClock block diagram (843001i-21 shown)

General Purpose Synthesizers

Designers can frequency tune and ease component management, using fewer device part numbers for more boards and applications

Functions

IDT Netcom general purpose synthesizers offer:

- Single and multiple frequencies
- Integrated fan-out
- Integer and fractional feedback architectures
- Spread spectrum and PLL lock indication

Benefits/Features

- Large range of output frequencies with high resolution programmability
- Available in multiple output styles

General purpose synthesizers are asynchronous clock sources with output frequencies readily selected with very high resolution (very small frequency steps) over a breadth of output frequencies. They use a simple, low cost fundamental-mode quartz crystal as the frequency reference, from which they synthesize low-jitter output clocks. Allowing on-the-fly configuration of the output frequency through either a parallel or serial interface, these flexible synthesizers support many wide frequency, low jitter clocking applications.

IDT Netcom CMOS synthesizers support frequencies up to 800 MHz, while our new ICs using SiGe technology support frequencies up to 3 GHz. Unlike many other frequency synthesis technologies, IDT Netcom synthesizers use a proprietary PLL architecture that simultaneously provides low jitter performance with a wide frequency range. Using silicon device integration techniques, they offer more functionality than fixed-frequency oscillators.

Designers can choose from a wide range of clock I/Os. Differential standards such as LVPECL, LVDS, HSTL, HCSL and CML are supported. For frequencies lower than 250 MHz, single-ended LVCMOS is available. Typically, IDT synthesizers use 2.5V or 3.3V supplies and are available in commercial and industrial temperature ranges.

The wide range of frequencies each device can cover and the flexibility and capability of each function make these synthesizers suitable for almost any general purpose, low-jitter application. They are often used to clock ASICs, CPUs and DSPs, as well as memory and logic, in applications ranging from high performance computing, storage, networking, communications and professional video.

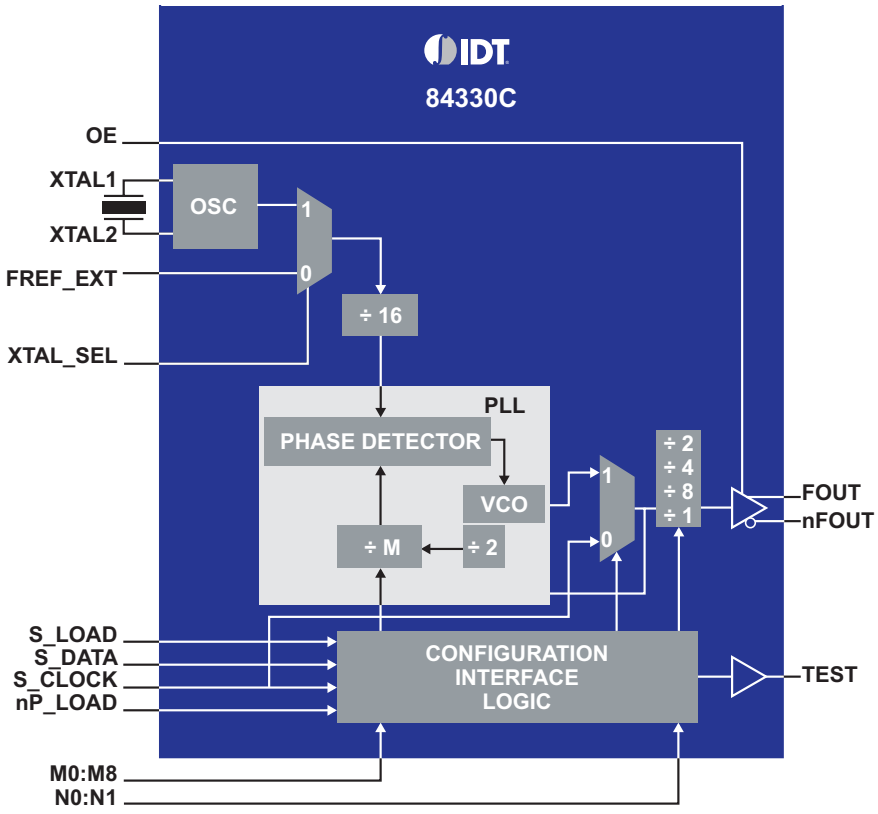


Figure 2. Typical frequency synthesizer (84330C shown)

Embedded Processor Clocks and QUICCclocks™

High performance gives designers confidence, simplicity promotes faster time to market

Functions

IDT Netcom embedded processor clocks deliver:

- Multiple frequencies
- Mixed output styles

Benefits/Features

- Single chip solution replaces multiple oscillators and buffers
- Integration reduces part count and enables simpler board design
- 25 MHz crystal reference also used to provide reference clocks to Ethernet PHY

Embedded processor clocks are a family of purpose built, fully integrated clocking devices. As single chip solutions, they provide all of the common clocks necessary for typical embedded processor applications. These include QUICCclocks™ devices that are optimized for use with PowerQUICC™ and Power Architecture™ processors, as well as devices optimized for Cavium™ processors. Every clock meets the needs of today's embedded processor boards.

These devices use a simple, low-cost fundamental mode 25 MHz quartz crystal or external system clock as the frequency reference. From this low frequency reference, they synthesize multiple output clock frequencies to provide all of the necessary clocks for common embedded processor applications, including low phase noise reference clocks for high speed serial links (e.g., Ethernet, PCIe®, Serial RapidIO®). On most devices the 25 MHz reference frequency is also buffered out to provide Ethernet PHY clocks.

The use of these devices allows for a simple, single chip integrated solution that replaces multiple oscillators, synthesizers and buffers. These devices provide better performance, use less board space and power, and cost less than discrete solutions.

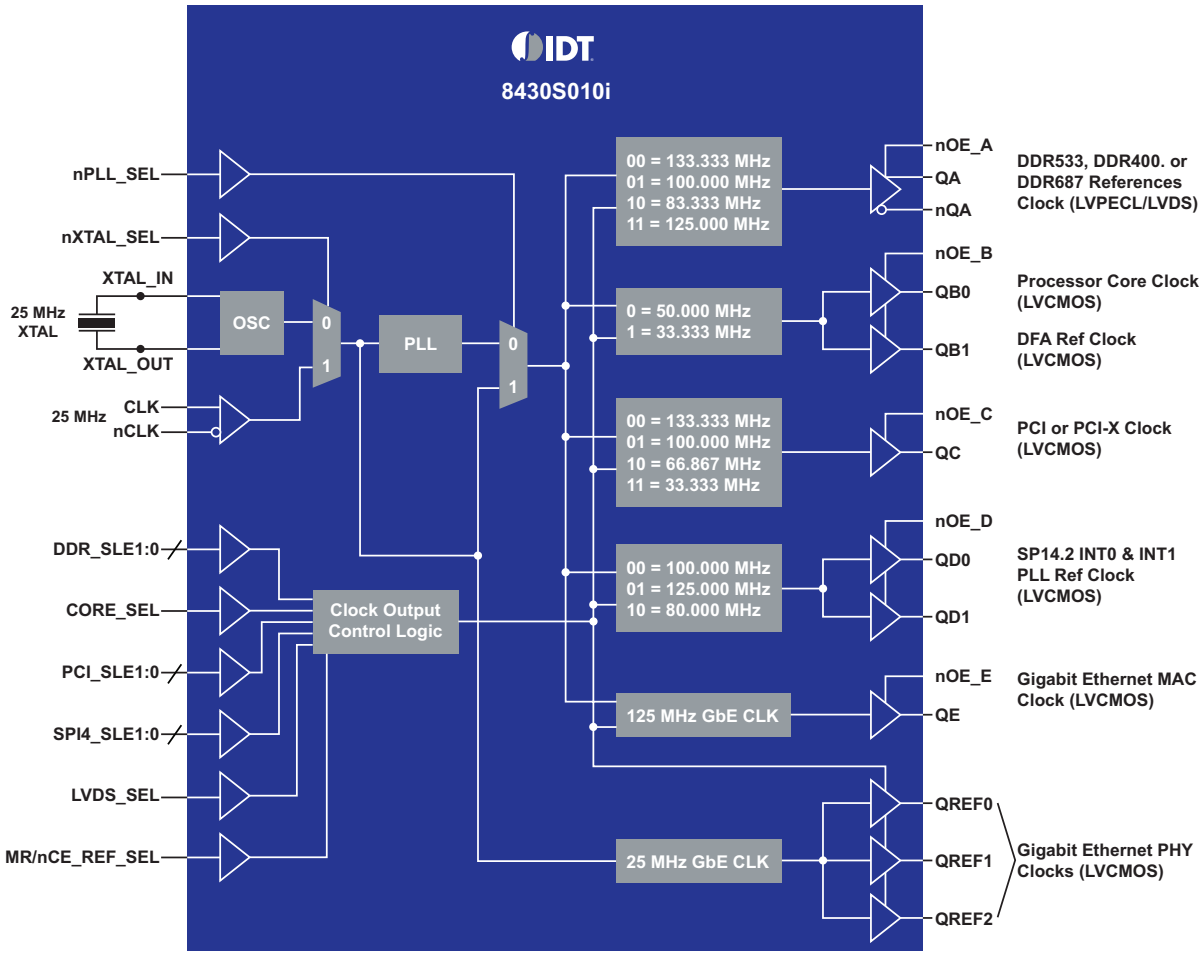


Figure 3. Typical embedded processor clock (8430S010i shown)

SOs and VCSOs

Delivering ultra low phase noise and stable high frequency operation

Functions

IDT Netcom SOs and VCSOs offer:

- Single and multiple frequencies, tunable by VIN control pin
- Jitter attenuation and frequency translation

Benefits/Features

- Output frequencies up to 3 GHz
- Better close-in phase noise than traditional crystal oscillators
- RMS phase noise performance that exceeds OC-192 standards

IDT Netcom offers a family of fixed-frequency surface acoustic wave (SAW) oscillators (SO) and variable frequency voltage-controlled SAW oscillators (VCSO). They are available in 5 mm x 7 mm and 9 mm x 14 mm hermetically sealed ceramic surface mount packages that incorporate the oscillator IC and the SAW delay in both package sizes. Standard output frequencies, from 100 MHz to 900 MHz, are readily available.

The high-Q quartz SAW delay lines that control the frequency of the SOs and VCSOs yield low phase noise and jitter, as well as an extremely stable frequency, over the operating temperature range. For applications requiring ultra-low phase noise or operation up to 3 GHz, IDT Netcom offers devices in a 15.24 mm x 20.32 mm surface mount module. Featuring a discrete RF design, these modules use analog frequency multiplication for output frequencies greater than 900 MHz.

IDT Netcom SOs are used anywhere fixed-frequency oscillators with ultra-low phase noise are needed. The VCSOs are well suited for high performance phase-locked loop circuits such as jitter attenuation and frequency translation, as well as other timing applications in telecom and optical networking systems.

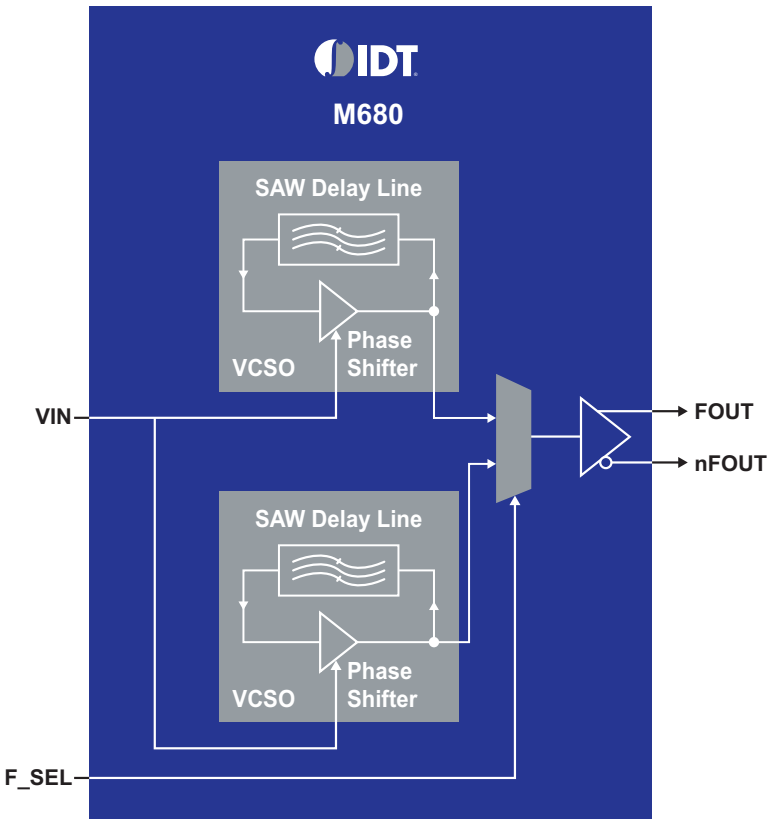


Figure 4. Typical voltage controlled SAW oscillator (M680 shown)

VCXO and VCXO + FemtoClock®

IDT Netcom voltage controlled crystal oscillator (VCXO) and VCXO + FemtoClock devices provide variable-frequency clock outputs that serve as the variable-frequency oscillator (VFO) element in a discrete PLL circuit

Functions

IDT Netcom VCXOs and VCXO + FemtoClock® products offer:

- Single and multiple frequencies, tunable by a VIN control pin
- Jitter attenuation and frequency translation

Benefits/Features

- Lower cost and shorter lead time than oscillators
- Reduced part count
- Greater functionality than traditional VCSOs

Using a pullable fundamental-mode crystal in the range of 12 MHz to 40 MHz, the VCXO device buffers the crystal frequency out to multiple outputs. VCXO + FemtoClock devices integrate the same fundamental mode VCXO and follow it with a FemtoClock frequency multiplier to provide high frequency outputs up to 800 MHz. All can be used in many applications to replace expensive single frequency VCSO products. The FemtoClock multiplier stage provides additional functionality and flexibility not available in VCSOs and at a lower cost.

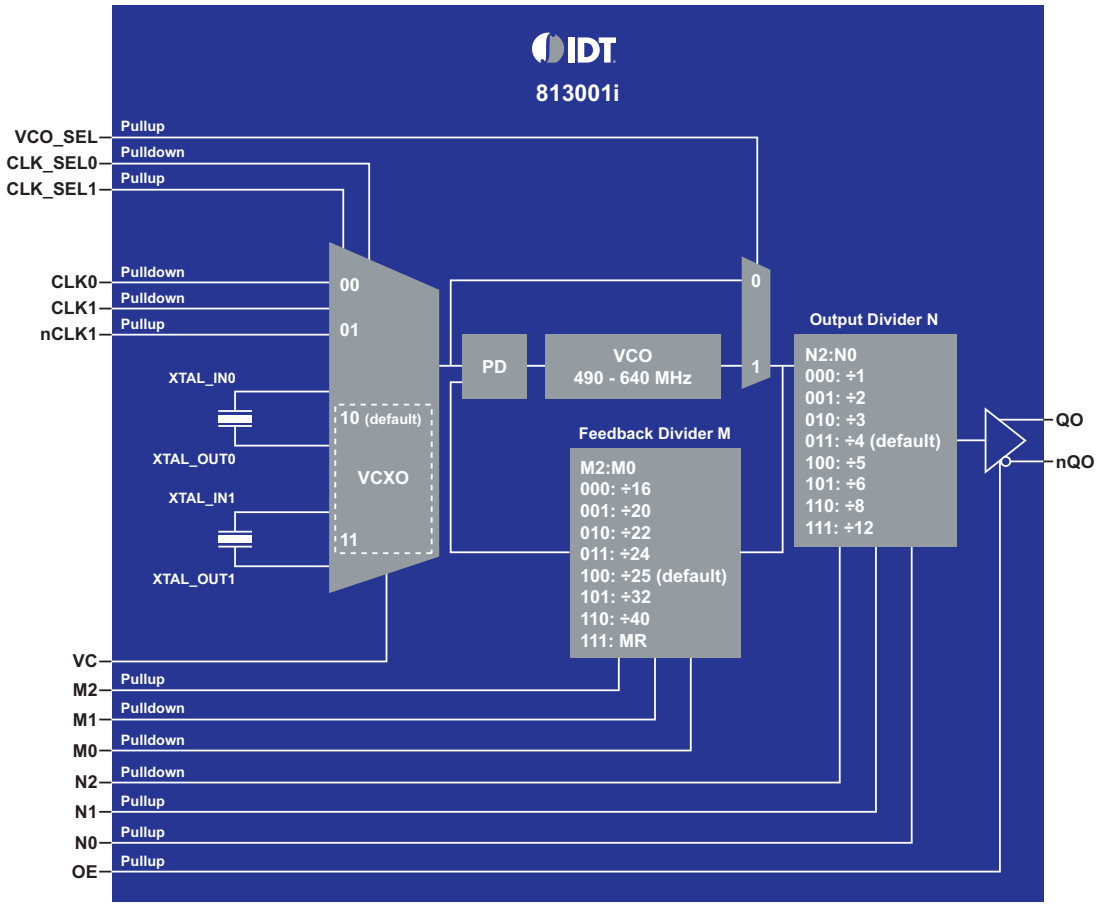


Figure 5. Typical VCXO + FemtoClock frequency synthesizer (813001i shown)

VCXO PLL + FemtoClock®

Replace expensive VCXO PLLs with high frequency, low noise FemtoClocks

Functions

IDT Netcom VCXO PLL + FemtoClock devices perform these and other functions:

- Jitter attenuation and frequency translation
- Synchronous clocking

Benefits/Features

- Lower cost than alternative, VCXO-based jitter attenuation solutions
- Multiple configurations and output styles available for each part
- Low jitter clock signals using FemtoClock PLL technology
- Reduced bit error when driving serial links
- Lower conversion error rates when driving DAC/ADC circuits

IDT Netcom voltage-controlled crystal oscillator (VCXO) PLL + FemtoClock® devices are synchronous jitter attenuation and frequency-translation products featuring a VCXO-based PLL stage with either internal VCXO requiring only an external pullable crystal, or with an external low-frequency VCXO. This PLL stage is typically configured with low loop bandwidth to provide jitter attenuation. It can also accommodate numerous pre- feedback- and output-divider combinations to allow for frequency translation. The output frequency from the VCXO PLL stage is then followed by a FemtoClock frequency multiplier that provides the capability to generate output frequencies up to 800 MHz with typical random phase-noise jitter of 1 ps RMS.

These devices can be used in many applications to replace expensive VCSO PLLs. Applications for VCXO PLL + FemtoClocks include synchronous Ethernet, wireless infrastructure, SONET/SDH, telecom and professional video.

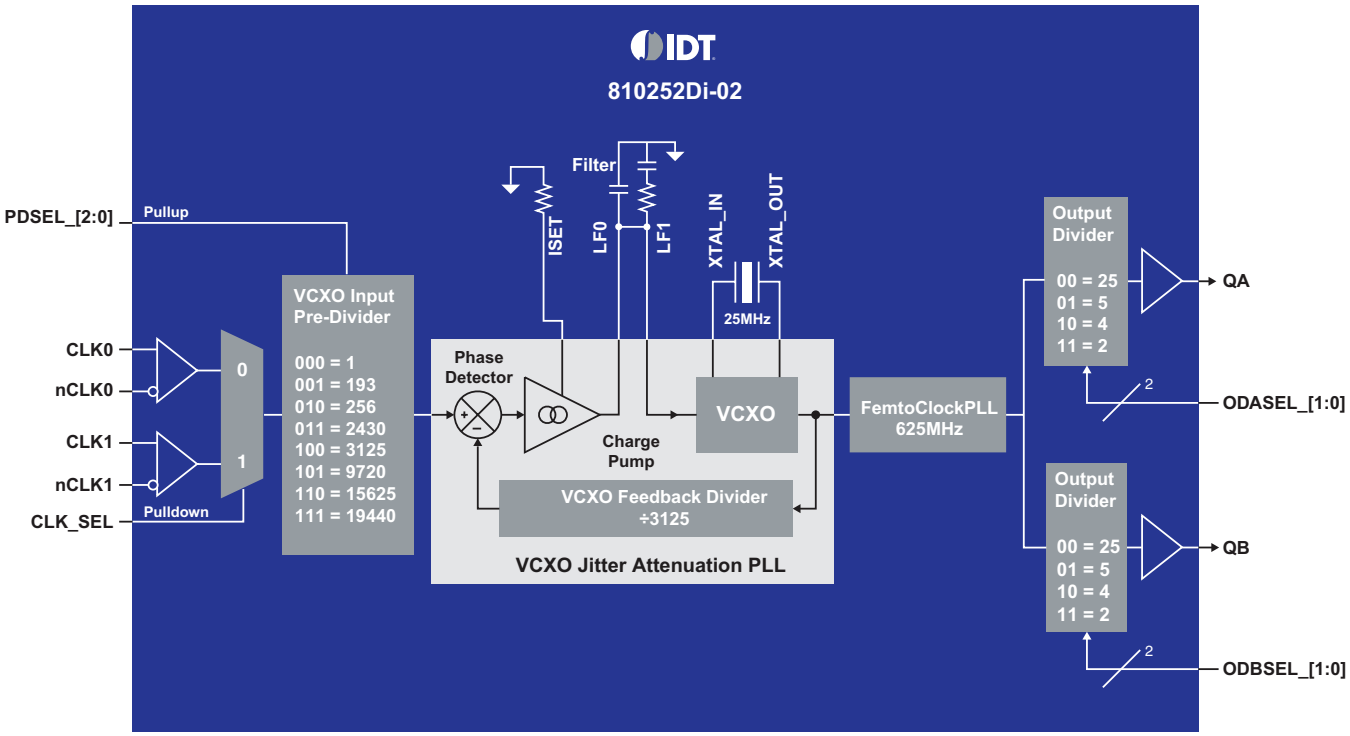


Figure 6. Typical VCXO PLL + FemtoClock frequency translator and jitter attenuator (810252Di-02 shown)

WAN PLLs

Flexible, fully programmable and cost effective

Functions

IDT Netcom WAN-PLLs offer:

- Compliance with Stratum Level 2, 3E, 3, SMC, 4E and 4 timing requirements
- Jitter attenuation using internal analog PLL

Benefits/Features

- Simplifies Stratum compliant clock systems design
- Monolithic solution for network synchronization in access, metro and core equipment
- Field proven to meet equipment standards from Telcordia, ITU, 3GPP and others
- Output jitter suitable to drive SONET chipsets up to OC-12 without external filtering
- Master/slave support enhances high availability systems with failover
- Broad family of devices with software compatibility enhances design portability
- Offloads critical system processor tasks such as automatic switching of revertive clock inputs

These highly-integrated digital PLL devices feature Stratum compliance for use in communication systems. Key benefits include ease of use due to full compliance with telecommunication standards, a rich feature set and programmability for high flexibility, and the reduction of board component count.

Wide Area Network (WAN) PLLs generate and synchronize telecommunication-specific clock signals, achieve clock redundancy and circuit protection, attenuate clock signal phase noise and jitter generation, and convert standard telecommunication clock signals. Typically used on line cards and central timing cards, they use an architecture combining digital and analog PLLs on a single chip:

- The digital PLL provides compliance to telecom standards such as high frequency accuracy on Stratum level 2, 3E, 3, SMC, 4E and 4 timing requirements and clock jitter attenuation. It provides circuit protection through integrated clock redundancy, including hitless switching, clock frequency holdover and phase build-out.
- The analog PLL converts clock frequencies, saving external components for frequency division and multiplication.

IDT WAN PLLs support three types of input clock sources: recovered clocks from STM-n or OC-n, PDH network synchronization timing and external references. The wide input clock range covers telecommunication frequencies from 2 kHz to 622.08 MHz and frame signals of 2 kHz, 4 kHz and 8 kHz. Clock outputs can be configured to generate frequencies from 1 kHz to 622.08 MHz and additionally generate frame signals at 2 kHz and 8 kHz. The 82V3255, 82V3280, and 82V3288 WAN-PLLs support T0 and T4 clock paths independently; other devices in this family are specifically designed to support the synchronization on DS0 (8 kHz), T1 (1.544 MHz), E1 (2.048 MHz) or OC-n (19.44 MHz) timing signals. The newest developments (82V3380 and 82V3355) support Ethernet clock frequencies for synchronous Ethernet applications.

The portfolio of WAN PLLs consists of frequency programmable and fixed frequency devices. The programmable devices with up to 14 redundant inputs and up to 11 outputs, such as the 82V3288, are the most flexible solutions. These are targeted for applications requiring flexibility in output frequency configuration and maximum support of circuit protection and redundancy. The fixed frequency devices are optimized for cost and board space in specific applications that have a defined frequency plan, require fewer protection features or require a smaller number of I/Os.

The IDT WAN PLL family provides a variety of application specific integrated circuits (ASIC) targeted at wireless infrastructure and wire line, access, transmission and network core applications.

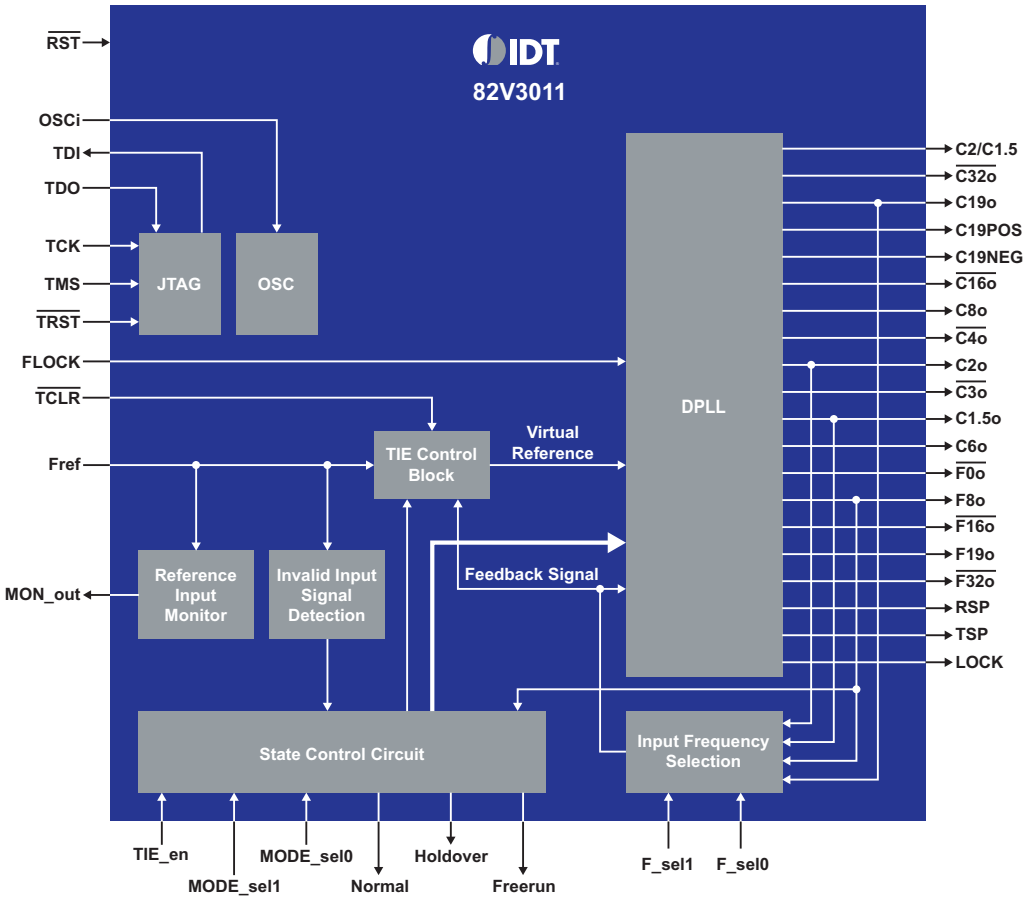


Figure 7. Simple WAN PLL (82V3011 shown)

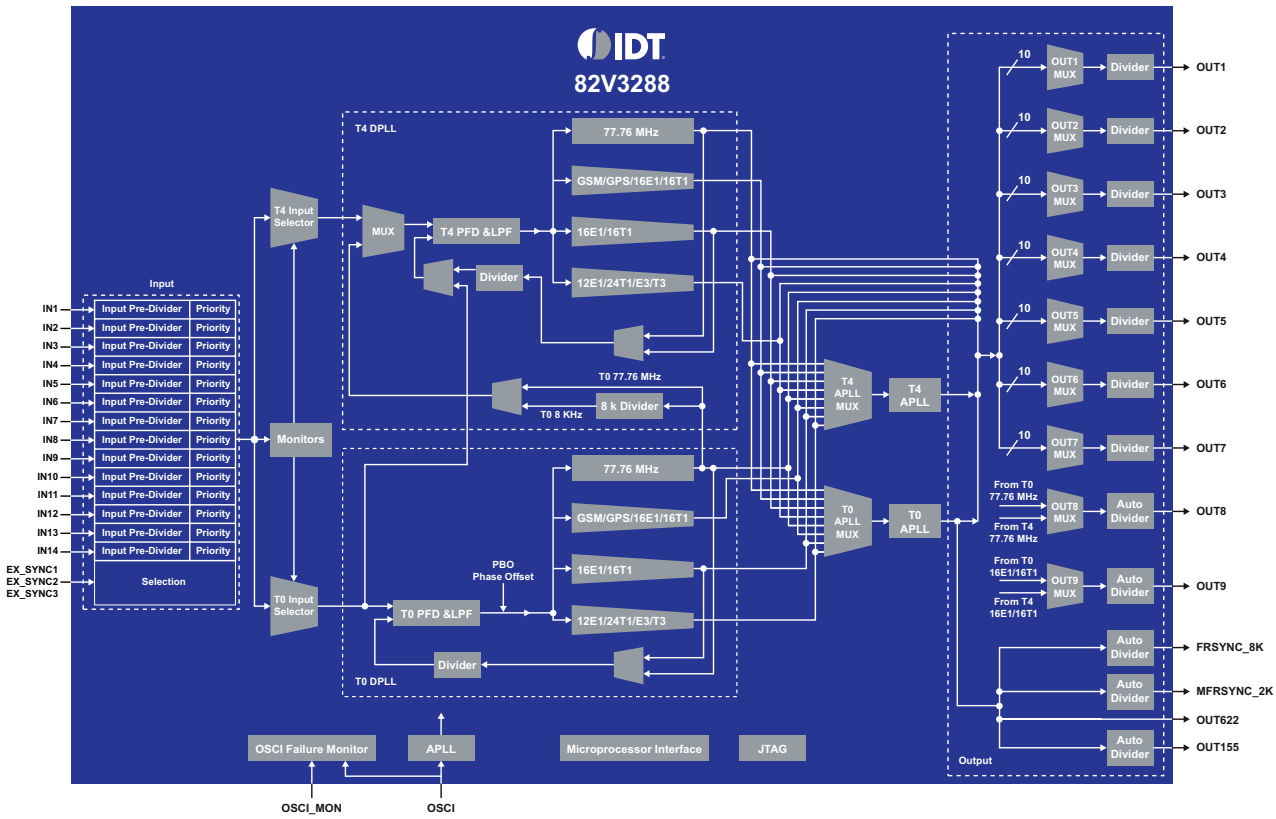


Figure 8. Full featured WAN PLL (82V3288 shown)

VCSO PLL Modules

VCSO PLL modules provide low noise jitter for optical networking and clock generation applications

Functions

IDT Netcom VCSO PLL modules offer:

- Single and multiple frequencies
- Jitter attenuation and frequency translation
- FEC and DFEC translation

Benefits/Features

- RMS phase noise performance exceeds OC-192 standards
- Device capable of phase build-out, hitless-switching and auto-switch
- Programmable outputs

The M900, M1000 and M2000 families of voltage-controlled SAW oscillator (VCSO) PLL modules combine an IDT Netcom custom IC and an IDT Netcom high-Q quartz surface acoustic wave (SAW) delay line in a 9mm x 9mm, hermetically sealed ceramic surface mount package. This provides a high performance, feature-rich solution that easily meets the ultra-low phase noise and jitter requirements of telecom and optical networking systems.

Each device uses a low-noise VCSO as part of a phase-locked loop (PLL). All of the functionality, including the VCSO circuitry, is in the custom IDT IC. The SAW delay line sets the output frequency. Each part number incorporates additional features such as phase build-out, hitless-switching, auto-switch and simplified divider programming with FEC and DFEC look-up tables and multiple outputs with programmable dividers to address particular applications.

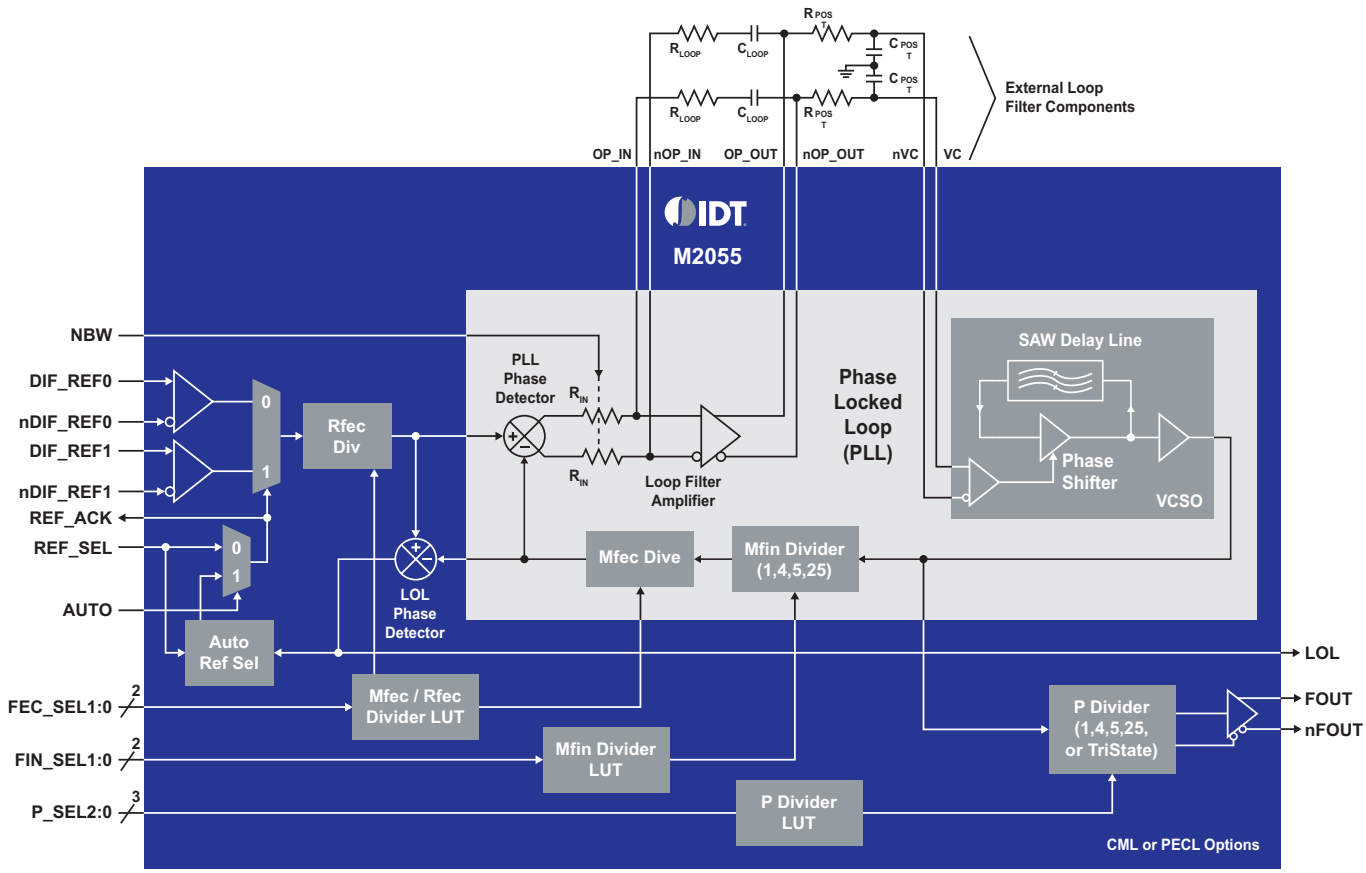


Figure 9. Typical voltage controlled SAW oscillator PLL module (M2055 shown)

PCI Express® Clocks

Flexible high performance clock solutions benefit advanced and industrial computing, as well as networking and telecommunication systems

Functions

The IDT Netcom PCI Express clock family delivers:

- High performance clock generation
- Jitter attenuation
- Zero-delay distribution
- Fan-out capabilities

Benefits/Features

- Output frequencies up to 250 MHz
- PCI Express Gen1 and Gen2 performance
- LVDS and HCSL output styles available in most devices

IDT Netcom PCI Express® clocks provide reference signals for PCI Express SERDES devices and for the integrated PCI Express ports of FPGAs and embedded microprocessors.

Within this family, there are devices available with integrated oscillators for use with an external, low-cost 25 MHz fundamental-mode quartz crystal. These devices asynchronously synthesize a system reference clock. There are also devices that can accept the system clock (typically 100 MHz or 125 MHz) as the reference clock input and feature configurable settings that allow synchronous translation of the input frequency to a different output frequency. Common output frequencies include 100, 125 and 250 MHz. These frequency translation devices regenerate the clock signal and attenuate unwanted clock jitter, which is beneficial in systems where the reference clock contains an undesirable amount of jitter.

For optimum flexibility, some devices allow the selection of PLL loop bandwidth to balance jitter attenuation and phase-tracking skew. The low-bandwidth mode provides maximum jitter attenuation. The high-bandwidth mode provides the phase best tracking skew and passes most spread spectrum modulation profiles.

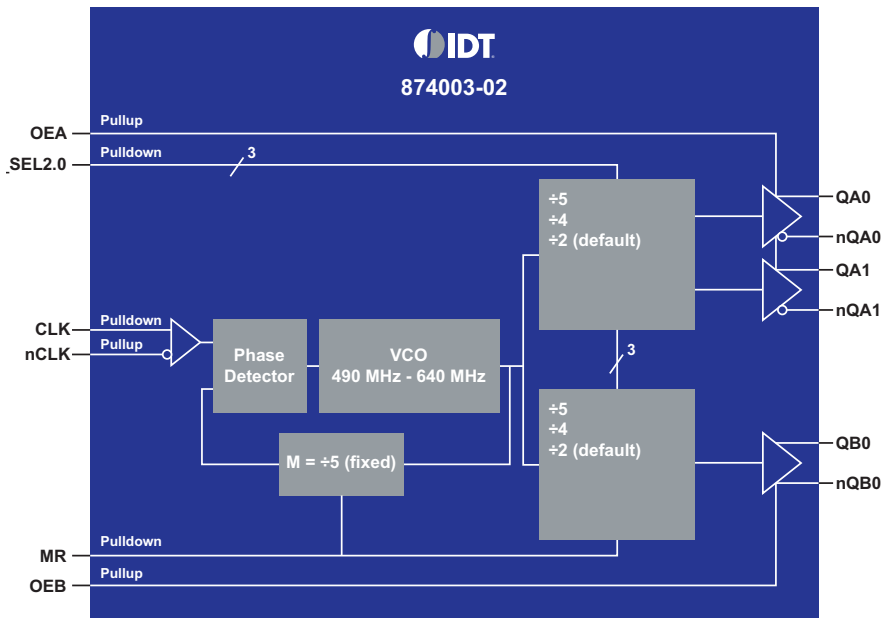


Figure 10. Typical PCI Express jitter attenuator (874003-02 shown)

Zero-Delay Buffers

Ideal for applications requiring synchronized clocking for FPGAs, CPUs, logic and synchronous memory

Functions

IDT Netcom zero-delay buffers offer:

- Synchronous copy of input to all outputs with minimal delay error
- Adjustability through external delay line

Benefits/Features

- Output frequencies up to 700 MHz
- 2.5V and 3.3V supply
- Wide variety of differential and single-ended output styles

Zero-delay buffers are PLL-based devices that regenerate the input clock signal with fan-out to drive multiple loads. The delay through the device can be adjusted through an external feedback path. This allows precise control of the timing of the clock signals to the loads.

Zero-delay buffers provide a synchronous copy of the input clock at the outputs, usually without frequency translation. Simple frequency translation is possible when a single divider is used for all outputs, including feedback output, to maintain clock synchronization.

The zero-delay buffer portfolio consists of many useful functions including devices with up to 18 outputs, differential outputs such as LVPECL, LVDS, and HSTL are supported for output frequencies up to 700 MHz and single-ended LVCMOS outputs for frequencies up to 250 MHz. Typically, IDT zero-delay buffers use 2.5V or 3.3V supply and are available in commercial and industrial temperature ranges.

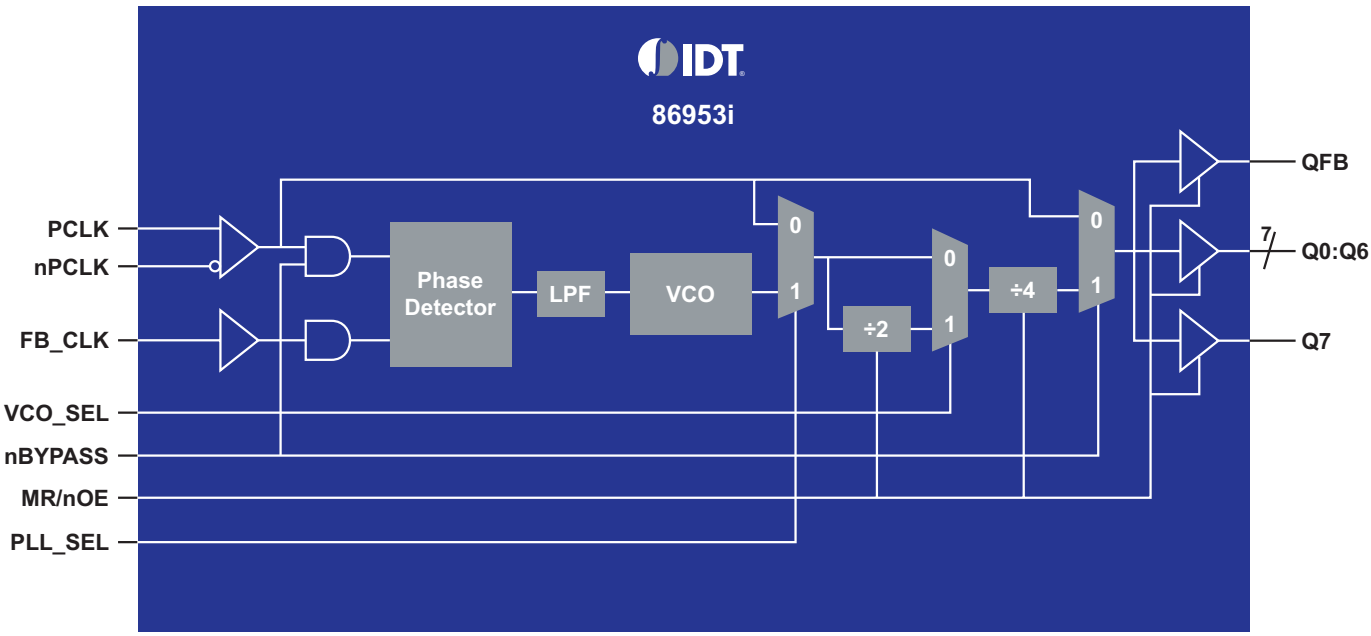


Figure 11. Typical zero-delay buffer (86953i shown)

Clock Generators

Frequency translation and jitter attenuation for FPGAs, CPUs, logic and memory

Functions

IDT Netcom clock generators support:

- Devices with up to 21 outputs
- Differential outputs such as LVPECL, LVDS, HSTL and SSTL
- Output frequencies up to 1.125 GHz and single ended LVCMOS outputs for frequencies up to 250 MHz

Benefits/Features

- Low cycle-to-cycle and period jitter
- External feedback for delay adjustments
- 2.5V or 3.3V supply modes

Clock generators are PLL-based products that regenerate the input clock signal with fan-out to drive multiple loads. They also allow for frequency translation—multiplication or division. The delay through these devices can be adjusted through an external feedback path, permitting precise control of clock signal timing to loads.

These frequency translation devices regenerate the clock signal and attenuate unwanted clock jitter. This is beneficial in systems where the reference clock contains an undesirable amount of jitter. Typically, IDT clock generators use 2.5V or 3.3V supplies and are available in commercial and industrial temperature ranges.

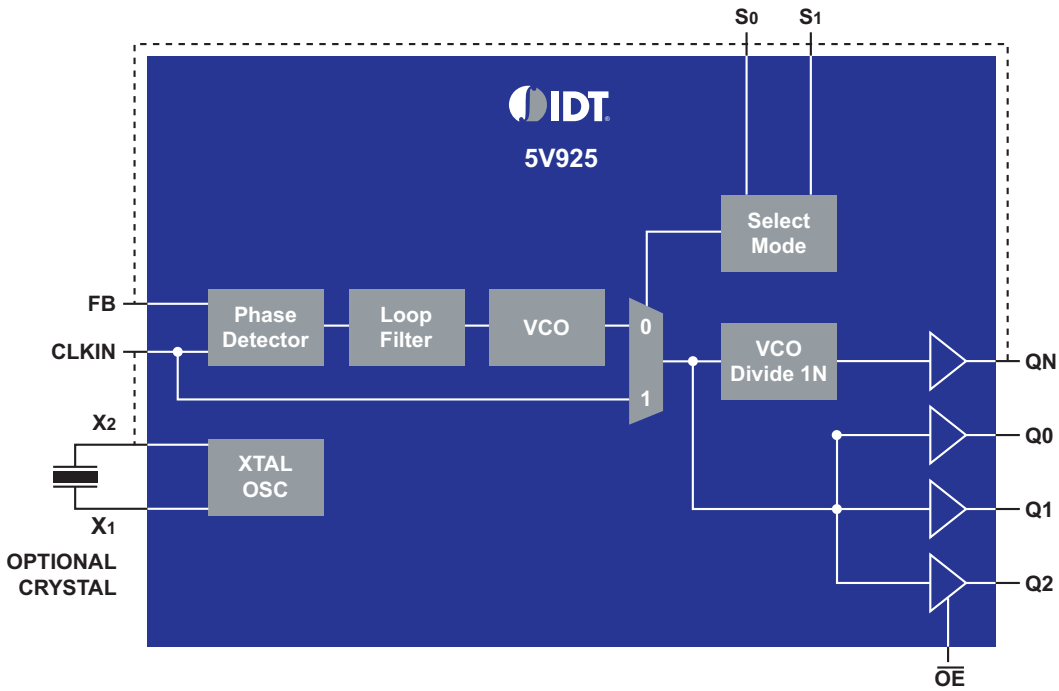


Figure 12. Typical clock generator (5V925 shown)

Dynamic Clock Switches (DCS)

Seamless support for redundancy requirements on the clock level

Functions

IDT Netcom dynamic clock switches deliver:

- Input clock monitoring circuitry
- Phase bump elimination during input switchover

Benefits/Features

- Low phase noise FemtoClock® PLL technology
- Minimal output period delta during clock switchover

Dynamic clock switches (DCS) are PLL-based clock generators specifically designed for redundant clock distribution systems. They are most often used in master and slave clocking circuits of high reliability equipment, such as core and edge routers and switches in networking or in high-end servers.

The devices monitor input clock signals to detect a failing reference clock signal and dynamically switch to a redundant clock signal. Smoothly controlling the output phase during the switching, they eliminate the phase bump typically caused by a clock failure. The switch from a failing clock to a redundant clock occurs without interruption of the output clock.

DCS offerings include LVPECL output parts for output frequencies up to 640 MHz and single-ended LVCMOS output parts for output frequencies up to 300 MHz. Typically, IDT Netcom dynamic clock switches use 2.5V or 3.3V supplies and are available in commercial and industrial temperature ranges.

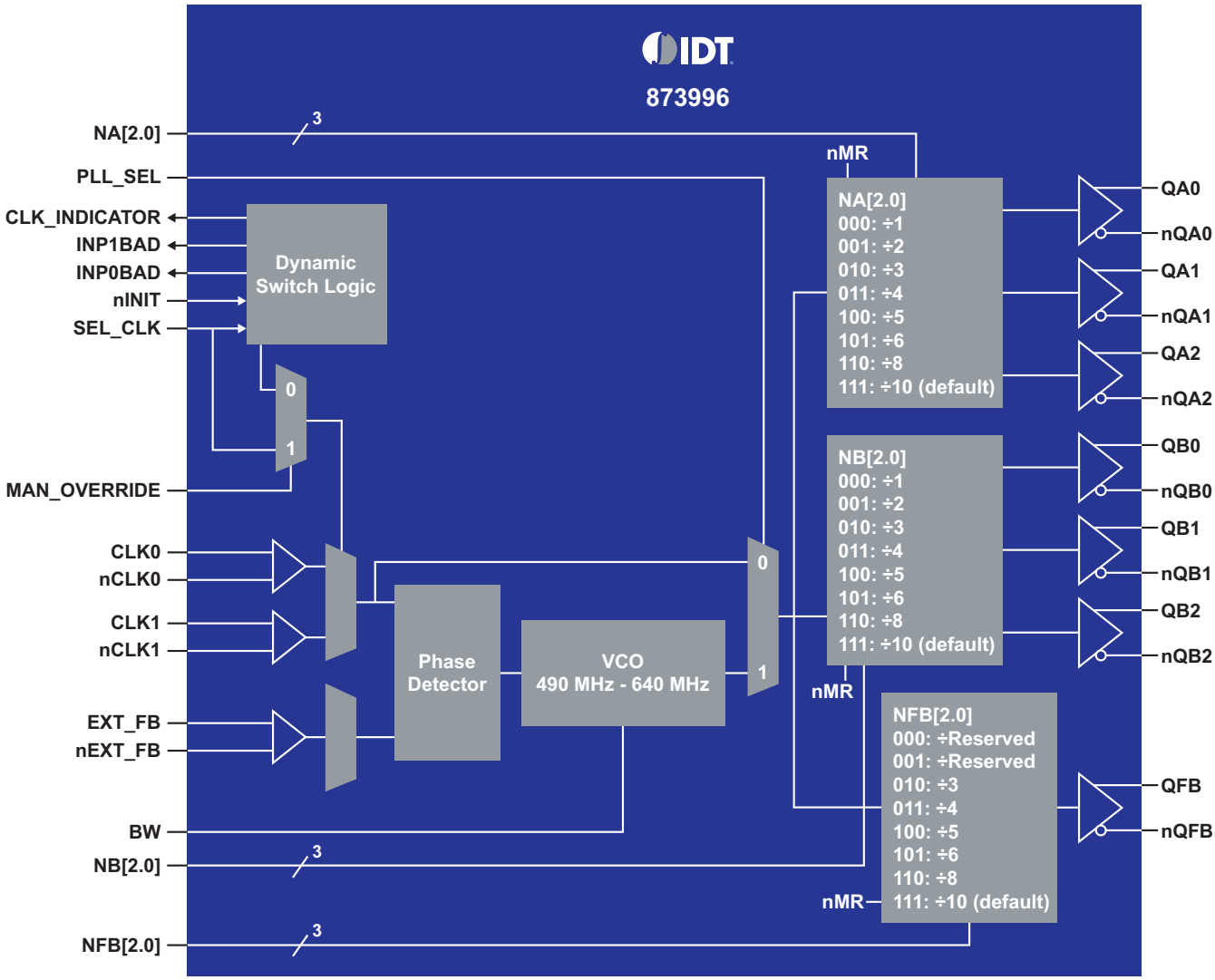


Figure 13. Typical dynamic clock switch clock generator (873996 shown)

Fan-out Buffers

Designed for tight timing budgets, optimized for low skew, delay and jitter

Functions

IDT Netcom fan-out buffers support:

- Devices with up to 27 outputs
- Differential outputs such as LVPECL, LVDS, HSTL and SSTL
- Differential output frequencies up to 3.2 GHz and single ended LVCMOS outputs for frequencies up to 350 MHz

Benefits/Features

- Full differential internal architecture
- Wide variety of output styles
- 1.8V, 2.5V or 3.3V supply modes
- Crystal fan-out buffers have an internal oscillator

Fan-out buffers are a useful building block of many clock trees, providing signal buffering and multiple copies of the input signal. Single output buffers are useful for translating a clock from one signaling standard to another (e.g. LVCMOS-in to LVPECL-out). Some devices have an integrated crystal oscillator, requiring only a low cost external fundamental-mode quartz crystal. The integrated oscillator provides an extremely low phase noise reference clock to drive jitter-sensitive devices such as the clock inputs of PHYs.

Almost all IDT fan-out buffers feature fully differential internal architecture—even devices with single-ended I/Os—reducing jitter caused by inherent common-mode noise rejection and improving output skew. The differential circuitry is constant-current and therefore injects less noise into system power supplies than single-ended solutions, reducing EMI compliance concerns.

The IDT Netcom fan-out buffer portfolio includes devices with up to 27 outputs. Differential outputs such as LVPECL, LVDS, DCM (HCSL), CML, HSTL, as well as selectable outputs, are supported for output frequencies up to 3200 MHz and single-ended LVCMOS outputs for frequencies up to 350 MHz. Some buffers are available with mixed output signaling. Typically, IDT buffers use 1.8V, 2.5V or 3.3V supplies and are available in the commercial and industrial temperature ranges.

If the exact buffer configuration is not found in the extensive IDT Netcom fan-out buffer offerings, please also consider devices in the IDT Netcom non-PLL clock divider portfolio that, when used in divide-by-1 mode, can also function as a fan-out buffer.

Fan-out buffers are general-purpose clock building block devices that can be used in any number of applications. Their high performance makes them well suited for use in networking, communications and high-end computing systems.

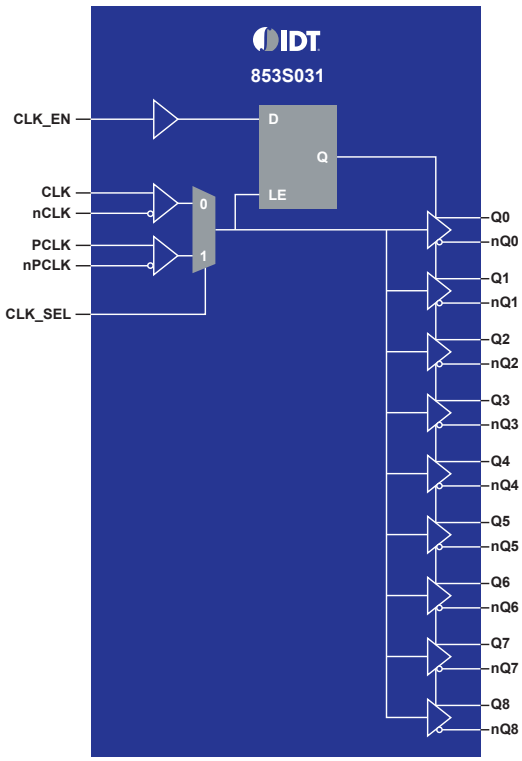


Figure 14. Typical fan-out buffer (853S031 shown)

Clock Dividers (Non-PLL)

The core building blocks of many clock trees

Functions

The IDT Netcom clock divider family offers:

- Devices with up to 20 outputs
- Differential outputs such as LVPECL, LVDS, HSTL and SSTL
- Output dividers up to divide-by-32

Benefits/Features

- Full differential internal architecture
- Wide variety of output styles
- 1.8V, 2.5V or 3.3V supply modes

Clock dividers provide an output clock signal that is a divided frequency of the input. They can also be used to provide signal buffering and make multiple copies of the input signal. Clock divider devices, when used in divide-by-1 mode, can also function as a fan-out buffer.

Most IDT Netcom clock dividers—even those with single-ended I/Os—feature fully differential internal architecture. Inherent common-mode noise rejection reduces jitter and improves output skew. The differential circuitry is constant-current and therefore injects less noise into system power supplies than single-ended solutions. This decreases EMI compliance concerns.

The IDT clock divider portfolio includes devices with up to 20 outputs. Various divide ratios, from divide-by-1 through divide-by-32, are available. Differential outputs such as LVPECL, LVDS, and selectable outputs are supported for output frequencies up to 3 GHz and single-ended LVCMOS outputs for frequencies up to 250 MHz. Also available are HCSL and LVCMOS outputs for specific applications. Typically, IDT buffers use 1.8V, 2.5V, or 3.3V supplies and are available in commercial and industrial temperature ranges.

Clock dividers are general-purpose clock building block devices that can be used in any number of applications. Due to their high performance, they are especially suited for use in networking, communications and high-end computing systems.

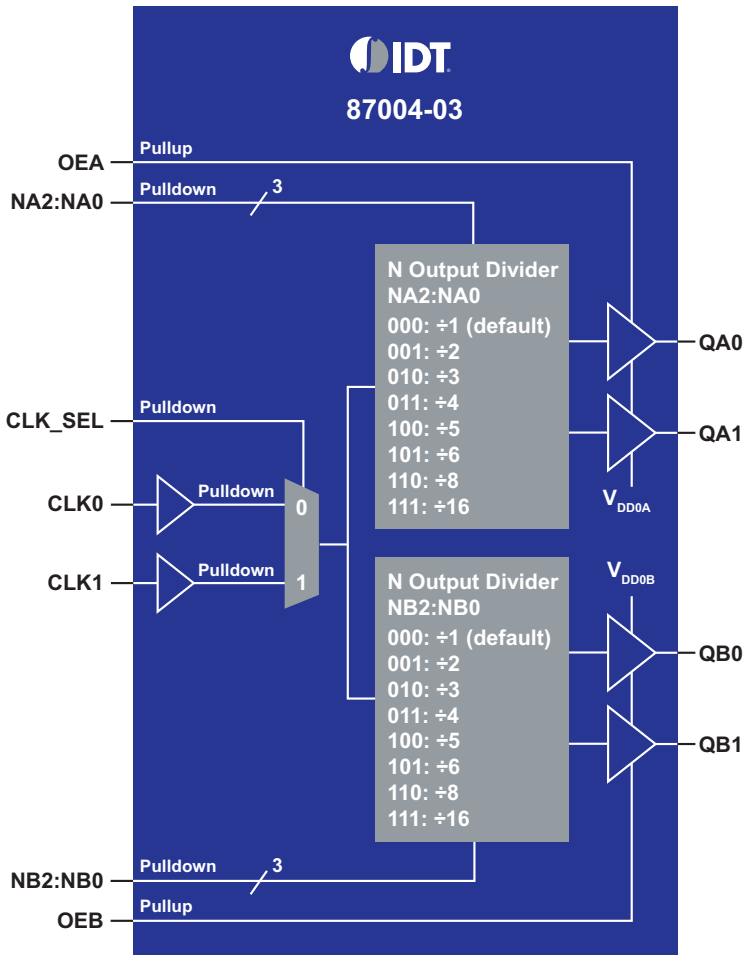


Figure 15. Typical clock divider (non-PLL) (87004-03 shown)

Multiplexers

Fully differential internal architecture improves jitter

Functions

The IDT Netcom multiplexer family offers:

- Devices with up to 16 inputs
- Differential outputs such as LVPECL, LVDS, HSTL and SSTL
- Support for differential output frequencies up to 3.2 GHz and single ended LVCMOS outputs for frequencies up to 350 MHz

Benefits/Features

- Full differential internal architecture
- Wide variety of output styles
- 1.8V, 2.5V or 3.3V supply modes
- >-50 dBMUX isolation between input paths

IDT Netcom multiplexers allow the selection from multiple clock inputs to drive the output. Devices are available with fan-out capability of the output signal. Some devices have integrated crystal oscillators, requiring only low cost external fundamental-mode quartz crystals. The integrated oscillators provide an extremely low phase noise reference clock to drive jitter sensitive devices such as the clock inputs of PHYs.

Almost all IDT multiplexers, even devices with single-ended I/Os, feature fully differential internal architecture. This improves jitter due to inherent common-mode noise rejection and improves output skew. The differential circuitry is constant-current and therefore injects less noise into system power supplies than single-ended solutions, reducing noise and decreasing EMI compliance concerns.

The IDT multiplexer portfolio includes devices with up to 16 inputs. Differential outputs such as LVPECL, LVDS, and selectable outputs are supported for output frequencies up to 3.2 GHz and single-ended LVCMOS outputs for frequencies up to 350 MHz. Typically, IDT multiplexers use 1.8V, 2.5V or 3.3V supplies and are available in the commercial and industrial temperature ranges.

IDT Netcom multiplexers are general-purpose clock building block devices for multiple applications. They are especially suited for use in networking, communications and high-end computing systems which require high performance.

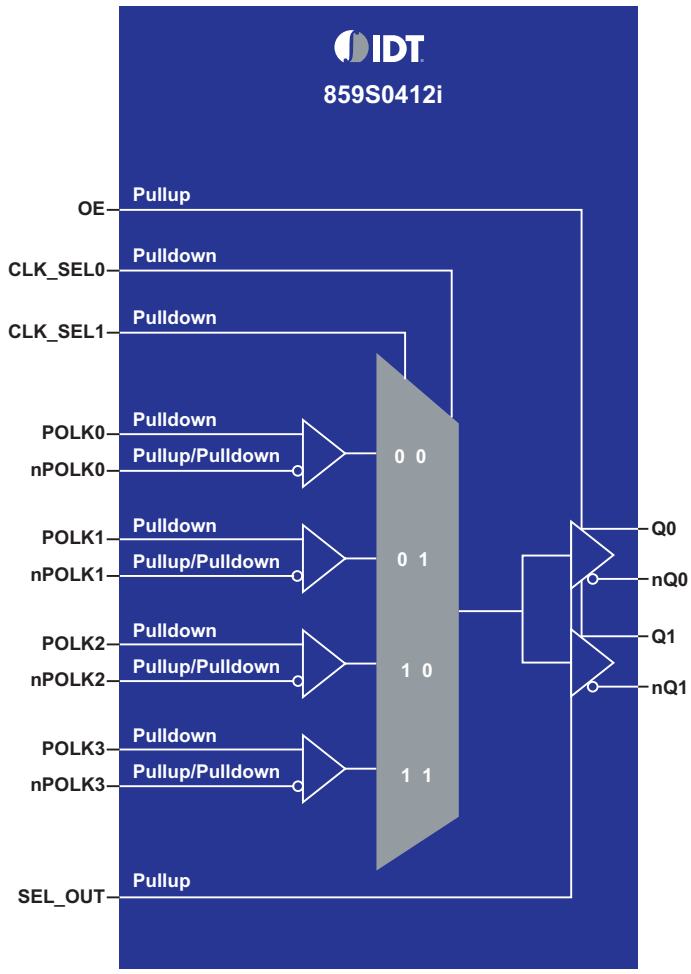


Figure 16. Typical multiplexer (859S0412i shown)

Programmable Skew

Versatile building block devices for use in networking, communications and advanced computing systems

Features

The IDT Netcom family of programmable skew products offers:

- Devices with up to 16 outputs
- Selectable HSTL or LVCMOS outputs
- Programmable skew increments as small as 250 picoseconds

Benefits/Features

- Frequency support up to 250 MHz
- LVCMOS or HSTL/LVCMOS outputs
- 2.5V, 3.3V or 5.0V supply modes

Programmable skew devices provide multiple copies of the clock input, where each bank of outputs can be individually programmed to different path delays to control skew. This provides flexibility for last minute clock skew management in the system.

The IDT programmable skew portfolio includes functions with up to 16 inputs, programmable output divide ratios up to divide-by-12, programmable skew increments as small as 250 picoseconds, and frequencies up to 250 MHz. Single-ended LVCMOS outputs and selectable HSTL/LVCMOS outputs are supported. Typically, IDT programmable skew devices use 2.5V, 3.3V or 5.0V supplies.

These high performance, general-purpose clock building block devices can be used in any number of applications, and are ideal for networking, communications and high-end computing systems.

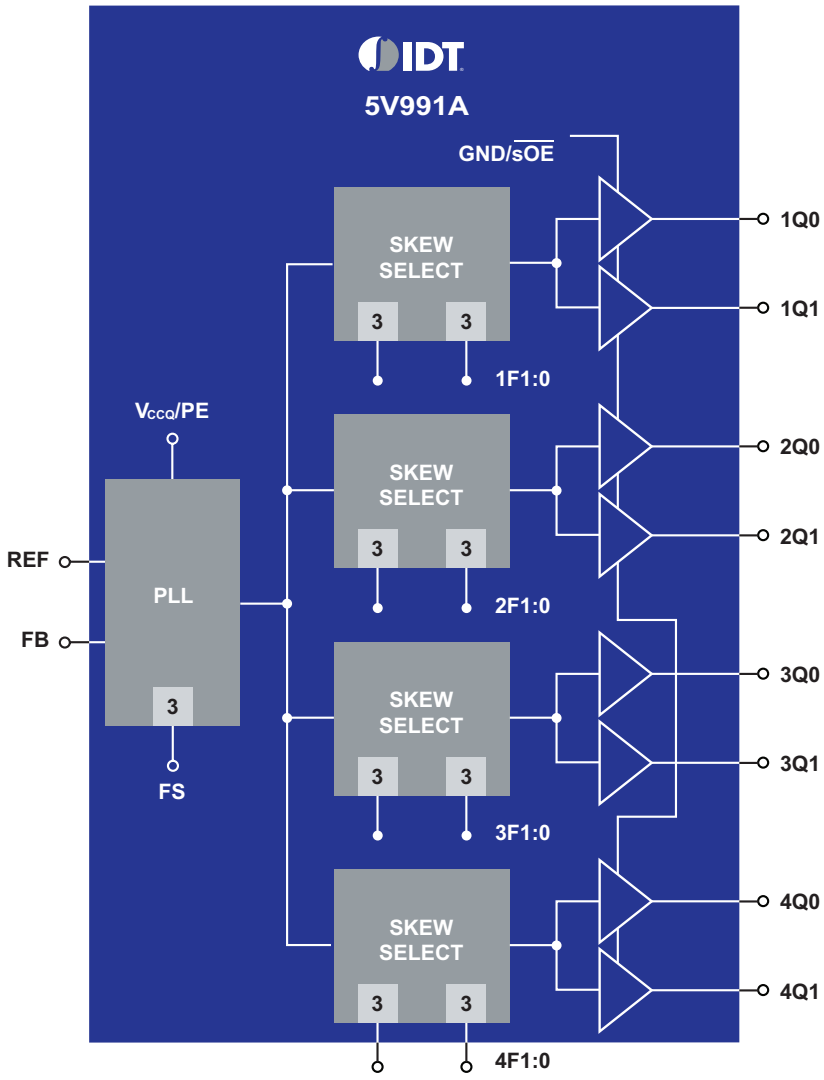


Figure 17. Typical programmable skew buffer (5V991A shown)

General Data Transceivers

IDT Netcom general data transceivers are used for bi-directional switching of data signals in telecommunications, networking and Ethernet data transmission

Functions

IDT Netcom general data transceivers deliver:

- MUX and DEMUX high speed data and clock paths
- Differential outputs such as LVPECL and LVDS

Benefits/Features

- I^2C programmability available on some devices
- Full differential internal architecture
- 2.5V or 3.3V supply modes

General data transceivers are simple buffer/translator devices featuring fully differential internal architecture. This reduces jitter caused by inherent common-mode noise rejection and improves skew. The differential circuitry is constant-current and therefore injects less noise into system power supplies than single-ended solutions, resulting in less noise coupling and decreasing EMI compliance concerns.

The IDT general data transceiver portfolio includes functions with differential outputs such as MLVDS, LVPECL and LVDS. Typically, the transceivers use 2.5V or 3.3V supplies and are available in the commercial and industrial temperature ranges.

The MUX and DEMUX functions are designed for flexible configuration changes of intra-system, high speed data and clock paths. A typical use of these functions is the data interface between ATCA and AMC boards in telecommunication applications. The devices enable the multiplexing, de-multiplexing and loopback of serial data streams such as Ethernet and high speed SERDES ports. Various device options support a uni- and bi-directional data transfer of single and multiple channels. Typical applications for the MUX/DEMUX family are telecommunications, networking, Ethernet data transmission and ATCA/AMC.

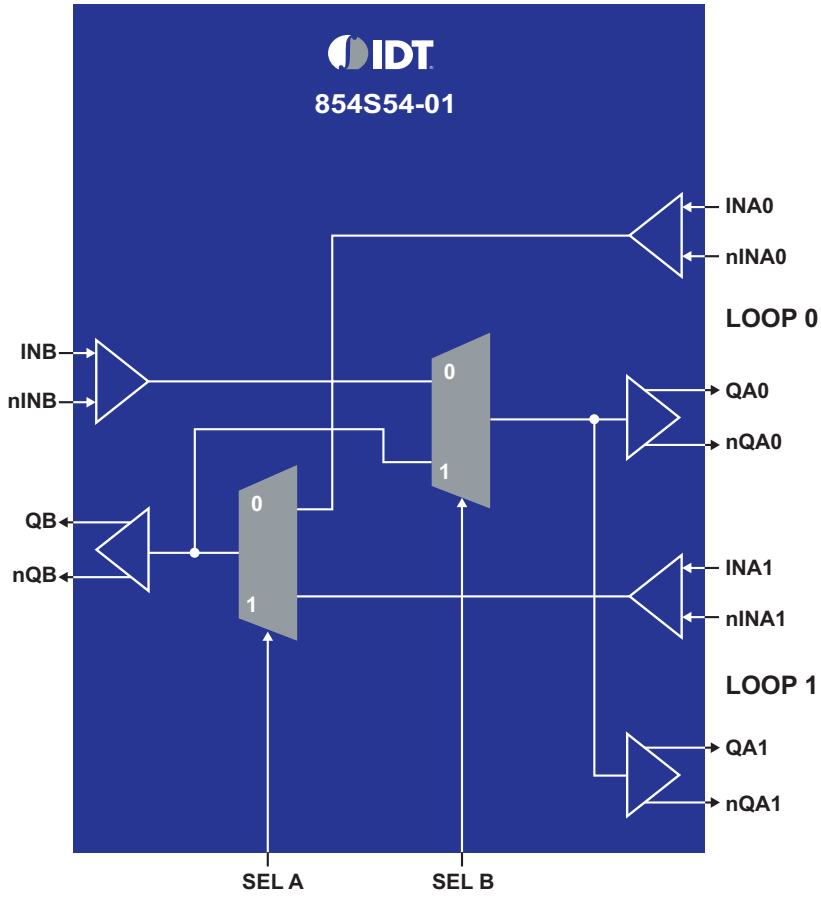


Figure 18. Typical general data transceiver (854S54-01 shown)

Programmable Delay Lines

Programmable delay lines provide variable delay of a differential input signal

Functions

IDT Netcom programmable delay lines provide:

- Clock de-skewing
- Timing and aperture adjustments

Benefits/Features

- Resolution down to 10 ps steps
- Full differential internal architecture
- 2.5V or 3.3V supply modes

High performance delay lines use an array of gates and multiplexers to provide programmable delay in precision circuits. Clock de-skewing and timing adjustment is accomplished using a digital control signal (10-bit long control word) which provides delay in 10 ps steps. Further enhancement of this 10 ps resolution for the delay is offered in versions which include a tunable gate (FTUNE).

The IDT Netcom programmable delay portfolio includes devices with differential outputs such as LVPECL and LVDS. They offer extremely low jitter and are targeted for many different end-applications, including test systems. Typically, the devices will operate from a 2.5V or 3.3V supply and are available in the commercial and industrial temperature ranges.

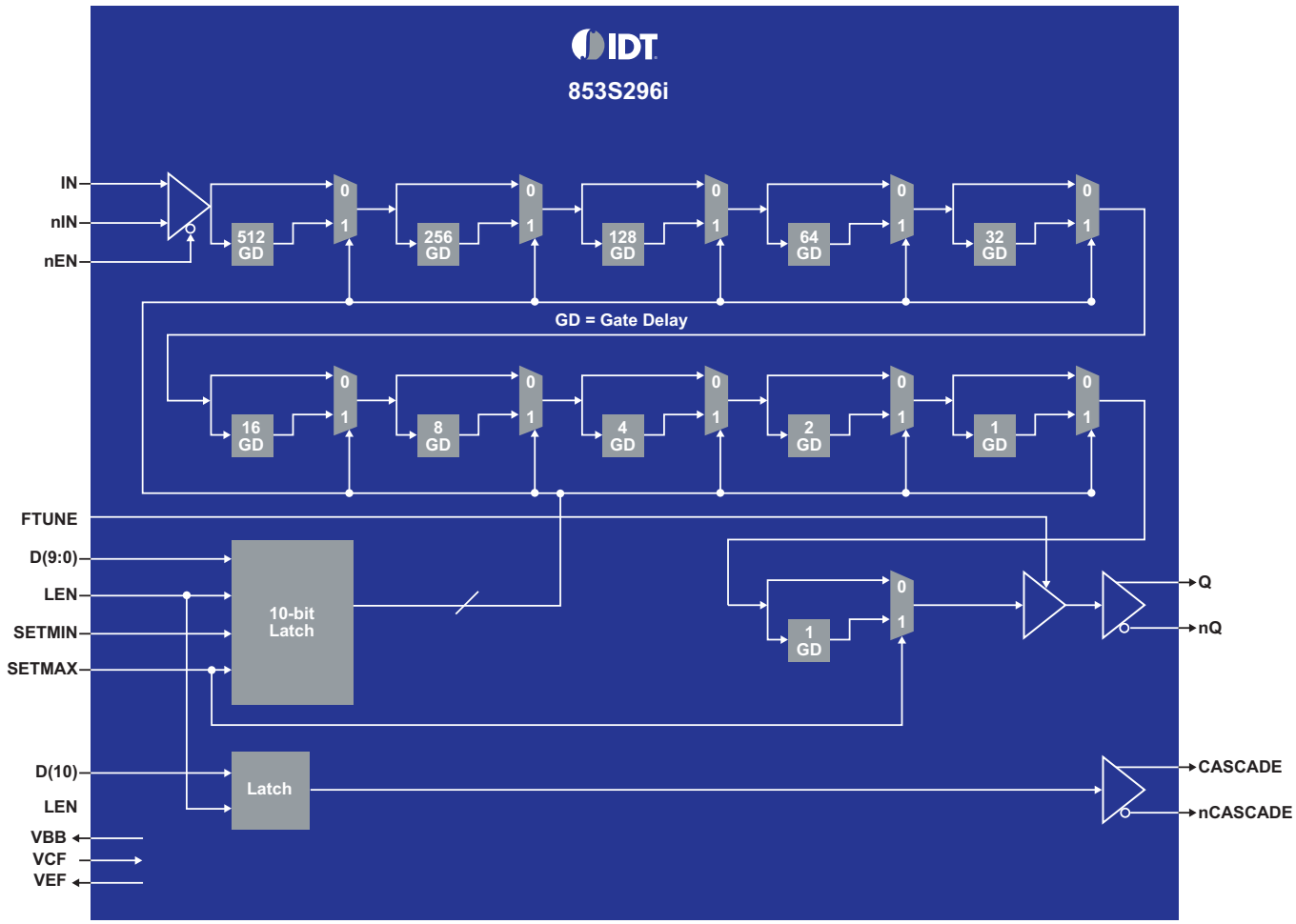


Figure 19. Typical programmable delay line (853S296i shown)

Clock and Data Recovery Devices

Clock and data recovery (CDR) circuits extract the clock signal from NRZ-coded input data signals

Functions

IDT Netcom clock and data recovery products provide:

- NRZ data input of 155.52 or 622.08 MBit/s
- Output clock signal of 155.52 or 622.08 MHz
- Low jitter clock outputs

Benefits/Features

- Proven solution for OC-3/-12 and STM-1/-4 clock/data recovery
- Differential clock inputs and outputs
- Lock reference input and PLL lock detect output
- 3.3V supply mode

CDR devices accept 622.08 or 155.52 MBit/s data signals and output both the recovered clock and re-timed data signals. Each device uses an internal phase-locked loop (PLL) based on the IDT proprietary FemtoClock® PLL technology.

CDR circuits use differential inputs and outputs to support high clock and data rates for the best signal integrity. All control panel inputs and outputs are single-ended signals. A signal-detect input and a lock-detect output are designed into each device, which enables users to interface with electro-optical modules.

IDT CDR devices can be used in STM-1/-4 (OC-3/-12) data streams, wireless infrastructure (transport and backhaul), wired communication, ADM equipment and any other application requiring direct interface with an electro-optical module.

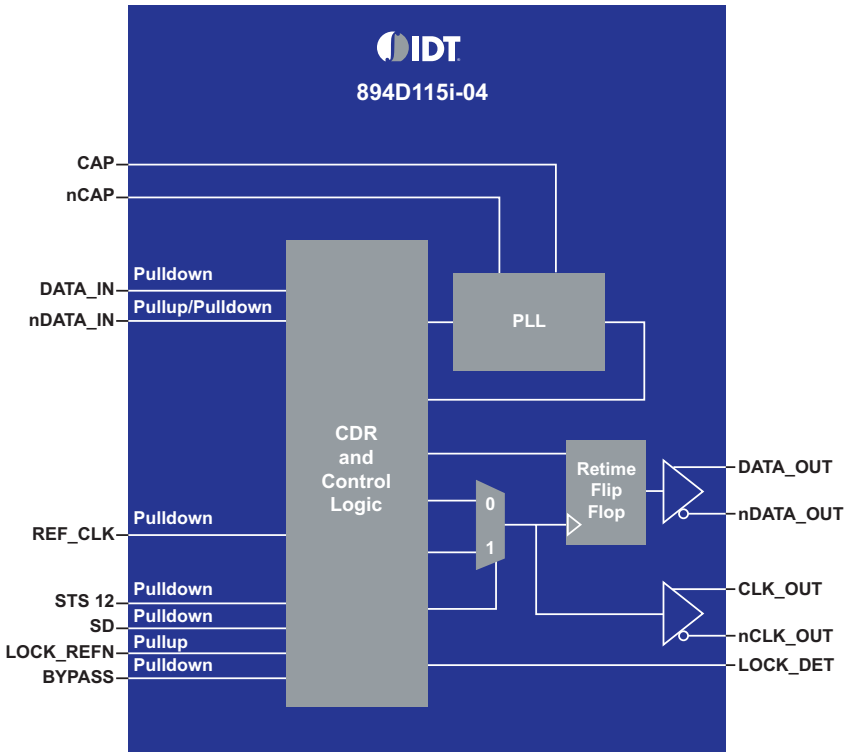
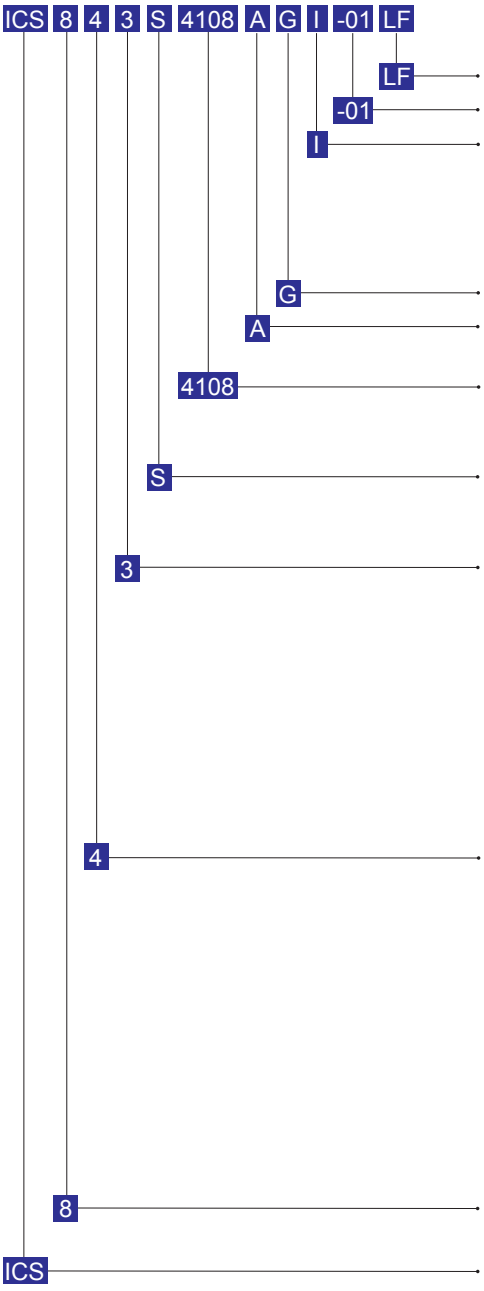


Figure 20. Typical clock and data recovery device (894D115i-04 shown)

Part Number Legend

Netcom nomenclature

There are three basic part number types in the IDT high-performance clock nomenclature. This is because when IDT acquired product lines from ICS and Freescale™, clients preferred that established part numbers be maintained for future orders. The three clock families can be identified by their marketing part number prefix (i.e., ICS, IDT, MPC/MC), and are defined in the following charts.



LF — Optional LF suffix on the end of a part number indicates “Lead Free” packaging

-01 — Optoinal dash number indicates a different function

I — Optional I suffix indicates “Industrial” (-40dC - 85dC) operating temperature range. Absence of “I” indicates “Commercial” (0dC - 70dC) operating temperature range. There are a series of bipolar timing devices that are Industrial operating temperature range but do not have “I” in the part number. See datasheet for details. Other non-standard temperature ranges indicated on the datasheet.

G — The letter in this position indicates the package. See datasheet for package details.

A — The first letter suffix is the device revision. Devices are initially provided at the “A” revision. Improvements are released using subsequent letters of the alphabet.

4108 — Function code. Usually one to four digits in length. A dash-number suffix can modify the function. In some products, the final one or two digits indicate the number of outputs.

S — S = Device uses SiGe fab process. Absense of “S” indicates that the part is in another process, usually CMOS or Bipolar.
D = Clock Data Recovery device.

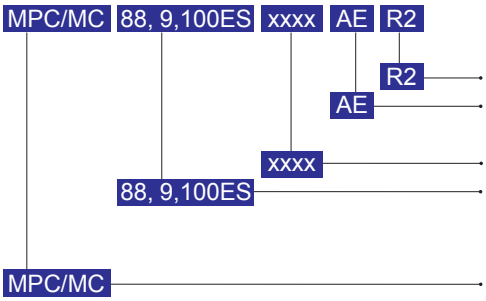
3 — The third digit can be a part of the function code, but usually indicates the style of outputs:
0 = LVCMOS
1 = HCSL/DCM (PCI Express)
2 = HSTL
3 = LVPECL
4 = LVDS
5 = CML
8 = SSTL
9 = Selectable

4 — The second digit can be a part of the function code, but usually indicates the type of device:
1 = VCXO based device
2 = Internal use only
3 = Non PLL Buffer, single-ended outputs
4 = PLL frequency Synthesizer (internal feedback, input is usually a crystal)
5 = Non PLL Buffer, differential outputs
6 = PLL Zero Delay Buffer (no frequency multiplication/division)
7 =a) Non PLL Buffer/Dividers
b) PLL based frequency multiplication/division (external feedback, zero delay type PLLs. Usually use a reference clock rather than a crystal input.
9 = Dual output device capable of either LVPECL or LVDS output levels

8 — An “8” in the first digit location indicates that the product is in the “Netcom” line of high-performance timing products for enterprise-class applications.

ICS — The “ICS” prefix indicates that the device is part of the timing line of products from IDT. This is a marketing prefix only, and is not contained in the orderable part number.

Part Number Legend *(continued)*



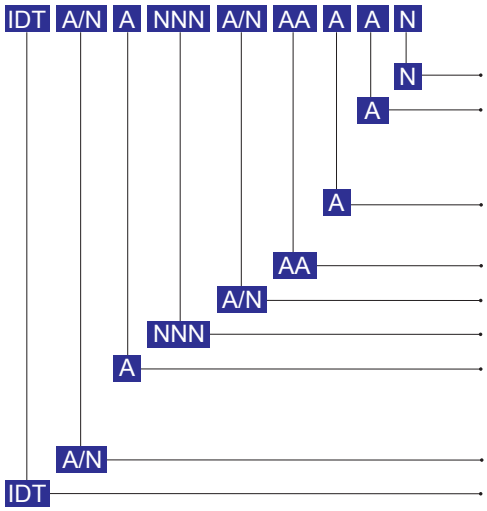
R2 — Optional R2 suffix on the end of a part number indicates “Tape and Reel” packaging.

AE — The two alpha characters in this position indicates the package type. See datasheet for package details.

xxxx — Specific product definition. Three, four or five digits in length.

88, 9,100ES — 88 = Freescale “88K” Legacy devices.
9 = LVCMOS PLL based clock or LVCMOS buffer.
100ES = SiGe fab process and is a differential buffer.

MPC/MC — The “MPC” or “MC” prefix indicates that the device is part of the timing line of products that were obtained from Freescale Semiconductor. This prefix must be included as part of the orderable part number.



N — Optional 8 suffix on the end of a part number indicates Tape and Reel packaging.

A — Temperature
None = “Commercial” (0dC - 70dC) operating temperature range.
I = “Industrial” (-40dC - 85dC) operating temperature range.

A — None = Standard Packaging
G = Green packaging

AA — Package Type. See datasheet for package details.

A/N — Speed—Refer to data sheet.

NNN — Device Type - Refer to data sheet.

A — Voltage
V = 3.3V (applies to family 5V only)
T = 2.5V (applies to family 5V only)

A/N — Product Family

IDT — The “IDT” prefix indicates that the device is part of the timing line of products from IDT. This prefix should not be included as part of the orderable part number.

Glossary

3GPP	3rd Generation Partnership Project
ATCA/AMC	Advanced Telecommunications Computing Architecture / Advanced mezzanine card
CML	Current mode logic
CMOS	Complimentary metal oxide semiconductor
DOCSIS	Data over cable service interface specification
DSP	Digital signal processor
HCSL	Host clock signal level
HSTL	High-speed transceiver logic
IEEE	Institute of Electrical and Electronics Engineers
ITU	International Telecommunication Union
JEDEC	Joint Electronic Devices Engineering Council
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS	Low voltage differential signal
LVPECL	Low-voltage positive emitter-coupled logic
MLVDS	Multipoint low voltage differential signal
NRZ	Not return to zero
PCIe®	Peripheral Component Interface Express
PHY	PHYsical, as in physical layer
PLL	Phase-locked loop
RMS	Root mean squared
SAW	Surface acoustic wave
SERDES	SERializer / DESerializer
SO	SAW oscillator
SONET/SDH	Synchronous optical NETwork / Synchronous Digital Hierarchy
SPI 4.2	SPI-4.2 is a version of the System Packet Interface
Telcordia	Telcordia Technologies (formerly Bell published by the Optical Internetworking Forum Communications Research, Inc. or Bellcore)
VCSO	Voltage-controlled saw oscillator
VCXO	Voltage-controlled crystal oscillator

Applications	Associated product lines	
Communications		
Enterprise	• Clocks/Timing • FIFO products • Multi-Port memories • PCI Express® switches	• Search engines & Accelerators • Serial RapidIO® solutions • Telecommunication ICs
Telecom	• Clocks/Timing • FIFO products • Multi-Port memories • Physical layer devices	• Search engines & Accelerators • SRAMs • Telecommunication ICs
Wireless Base Stations	• Clocks/Timing • FIFO products • Multi-Port memories	• SAW filters • Serial RapidIO® solutions • Telecommunication ICs
Computing		
Desktops	• Advanced Memory Buffers • Clocks/Timing	• PC Audio solutions • PCI Express® switches
Embedded	• Clocks/Timing • Multi-Port memories	• PC Audio solutions • PCI Express® switches
Notebooks	• Clocks/Timing • PC Audio solutions	• Video interfaces
Servers	• Advanced Memory Buffers • Clocks/Timing	• PCI Express® switches
Consumer		
Digital TV	• Clocks/Timing • Video processing	• Video interfaces
Gaming	• Clocks/Timing	• PC Audio solutions
Portable consumer devices/handsets	• Clocks/Timing • FIFO products	• Multi-Port memories
Set Top Box	• Clocks/Timing	

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