PRODUCT ADVISORY

Data Sheet Specification Change for Intersil Product ISL36111*

Refer to:
PA10105

Date: October 27, 2010

October 27, 2010

To: Our Valued Intersil Customers

Subject: **Data Sheet Specification Change for Intersil Product ISL36111***

This advisory is to inform you that Intersil has updated the data sheet specification for the listed ISL36111* products. The updates consist of the following:

i) The description for the VDD pin in the Pin Descriptions table was updated to recommend the use of parallel 100pF and *47nF* decoupling capacitors to ground for each of these pins.
ii) The description for the CP[A,B] pin in the Pin Descriptions table was updated to indicate the pins are read as a *2-digit* number to set the boost level.
iii) Added Figure 8 - Typical Application Reference Schematic and a section titled PCB Layout Considerations.

Modifications to the data sheet are complete. The updated data sheet is available on the Intersil web site at http://www.intersil.com/data/fn/fn6974.pdf.

Products Affected: **ISL36111DRZ-T7 ISL36111DRZ-TS**

There have been no changes made to the silicon or device itself.

Intersil will take all necessary actions to conform to customer requirements and to ensure the continued high quality and reliability of Intersil products being supplied. Customers may expect to continue receiving product processed to the same established conditions and systems used for screening of material supplied today.

If you have concerns with this change notice, Intersil must hear from you promptly. Please contact the nearest Intersil Sales Office or call the Intersil Corporate line at 1-888-468-3774, in the United States, or 1-321-724-7143 outside of the United States.

Jon Brewster

Jon Brewster
Intersil Corporation PA10105

CC: J. Touvell A. Dave G. Oganessyan J. Mitchell

PA10105 – Pin Description Table Updates

Current

Pin Descriptions

PIN NAME	PIN NUMBER	DESCRIPTION
V_{DD}	1, 9, 12	Power supply. 1.2V supply voltage. The use of parallel 100pF and 10nF decoupling capacitors to ground is recommended for each of these pins for broad high-frequency noise suppression.
IN[P,N]	2, 3	Equalizer differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
LOSB	4	LOS BAR indicator. Low output when input signal is below DT threshold. This pin is internally pulled HIGH with an 11kΩ resistor.
CP[A,B,]	6, 7	Control pins for setting equalizer boost level. Tri-state inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and B is the LSB.
GND	5, 8, 13, 16	These pins must be grounded.
OUT[P,N]	11, 10	Equalizer differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
DT	15	Detection Threshold. Reference DC voltage threshold for input signal power detection. Data output OUT[P,N] is muted when the power of the input signal IN[P,N] falls below the threshold. Tie to ground to disable electrical idle preservation and always enable the output driver.
Exposed Pad	-	Exposed pad. For proper electrical and thermal performance, this pad should be connected to the PCB ground plane.

New

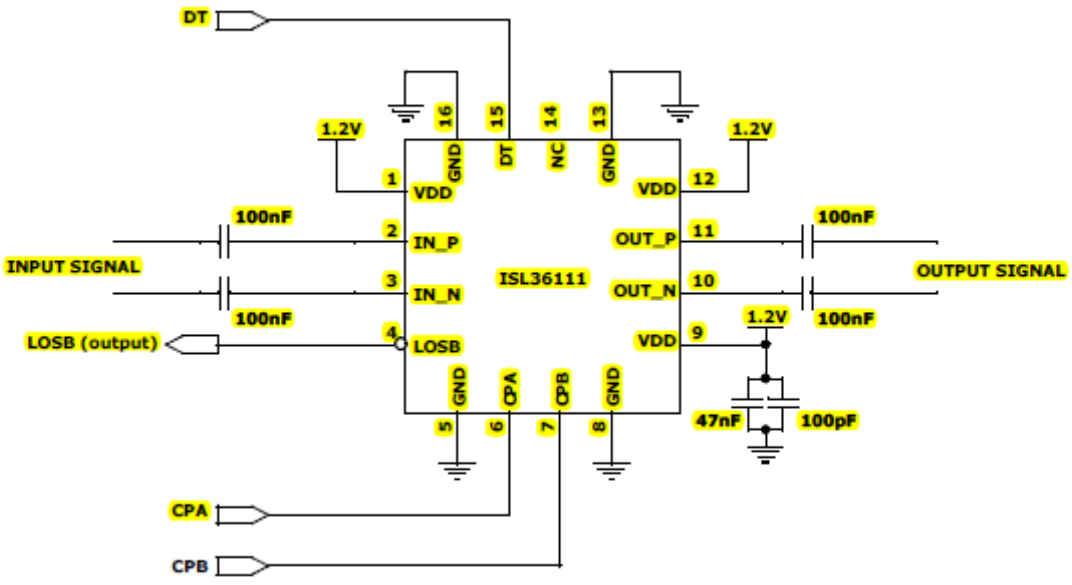
Pin Descriptions

PIN NAME	PIN NUMBER	DESCRIPTION
V_{DD}	1, 9, 12	Power supply. 1.2V supply voltage. The use of parallel 100pF and 47nF decoupling capacitors to ground is recommended for each of these pins for broad high-frequency noise suppression.
IN[P,N]	2, 3	Equalizer differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
LOSB	4	LOS BAR indicator. Low output when input signal is below DT threshold. This pin is internally pulled HIGH with an 11kΩ resistor.
CP[A,B]	6, 7	Control pins for setting equalizer boost level. Tri-state inputs. Pins are read as a 2-digit number to set the boost level. A is the MSB, and B is the LSB.
GND	5, 8, 13, 16	These pins must be grounded.
OUT[P,N]	11, 10	Equalizer differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
DT	15	Detection Threshold. Reference DC voltage threshold for input signal power detection. Data output OUT[P,N] is muted when the power of the input signal IN[P,N] falls below the threshold. Tie to ground to disable electrical idle preservation and always enable the output driver.
Exposed Pad	-	Exposed pad. For proper electrical and thermal performance, this pad should be connected to the PCB ground plane.

PA10105 – Application Information Updates

Application Information

Typical application schematic for ISL36111 is shown in Figure 8.



NOTES:

14. See "Control Pin Boost Setting" on page 5 for information on how to connect the CP pins
15. See "Detection Thereshold (DT) Pin Functionality" on page 6 for details on DT pin operation.
16. Although the filtering network is shown only for one V_{DD} pin for simplicity, all the V_{DD} pins need to be connected in this way.

FIGURE 8. TYPICAL APPLICATION REFERENCE SCHEMATIC FOR ISL36111

PCB Layout Considerations

Because of the high speed of the ISL36111 signals, careful PCB layout is critical to maximize performance. The following guidelines should be adhered to as closely as possible:

- All high speed differential pair traces should have a characteristic impedance of 50Ω with respect to ground plane and 100Ω with respect to each other.
- Avoid using vias for high speed traces as this will create discontinuity in the traces characteristic impedance.
- Input and output traces need to have DC blocking capacitors (100nF). Capacitors should be placed as close to the chip as possible.
- For each differential pair, the positive trace and the negative trace need to be of same length in order to avoid intra-pair skew. Serpentine technique may be used to match trace lengths.
- Maintain a constant solid ground plane underneath the high-speed differential traces
- Each V_{DD} pin should be connected to 1.2V and also bypassed to ground through a 47nF and a 100pF capacitor in parallel. Minimize the trace length and avoid vias between the V_{DD} pin and the bypass capacitors in order to maximize the power supply noise rejection.

About Q:ACTIVE®

Intersil has long realized that to enable the complex server clusters of next generation datacenters, it is critical to manage the signal integrity issues of electrical interconnects. To address this, Intersil has developed its groundbreaking Q:ACTIVE® product line. By integrating its analog ICs inside cabling interconnects, Intersil is able to achieve unsurpassed improvements in reach, power consumption, latency, and cable gauge size as well as increased airflow in tomorrow's datacenters. This new technology transforms passive cabling into intelligent "roadways" that yield lower operating expenses and capital expenditures for the expanding datacenter.

Intersil Lane Extenders allow greater reach over existing cabling while reducing the need for thicker cables. This significantly reduces cable weight and clutter, increases airflow, and improves power consumption.