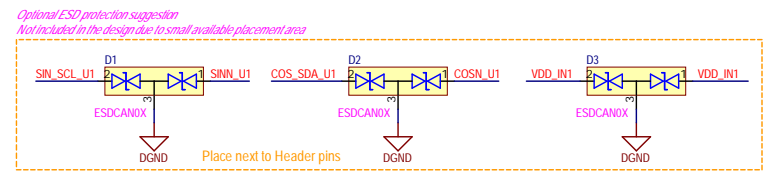




A_28_IPS2550_4x90_OD32_ID15

Date: 09.05.2022
Project: A_28_V10_IPS2550_4x90_OD32_ID15.PrjPcb
Version: 1.0
Content: Schematic
Sensor PCB Layout
Sensor PCB 3D Model
Bill of Materials
PCB Manufacturing Requirements
Sensor PCB Layer Stack
Sensor PCB Placement
Target PCB Layout
Target PCB 3D Model

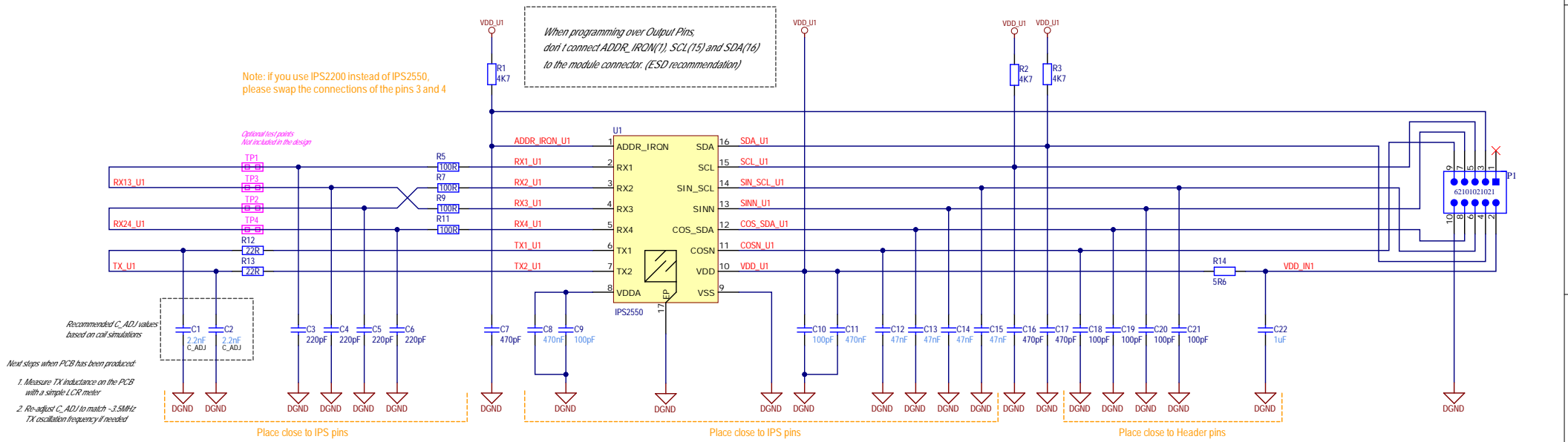
ESD protection diodes are recommended for voltage levels over 20kV.
E.g. using 150pF / 3300hm ESD gun for test



When programming over Output Pins, don't connect ADDR_IRON(1), SCL(15) and SDA(16) to the module connector. (ESD recommendation)

Note: if you use IPS2200 instead of IPS2550, please swap the connections of the pins 3 and 4

Optional test points
Not included in the design



Recommended C_ADJ values based on coil simulations

Next steps when PCB has been produced

1. Measure TX inductance on the PCB with a simple LCR meter
2. Re-adjust C_ADJ to match ~3.5MHz TX oscillation frequency if needed

$$f_{TX} = \frac{1}{2\pi\sqrt{L_{TX}C_{TX}}} \rightarrow C_{TX} = \frac{1}{(2\pi f_{TX})^2 L_{TX}}$$

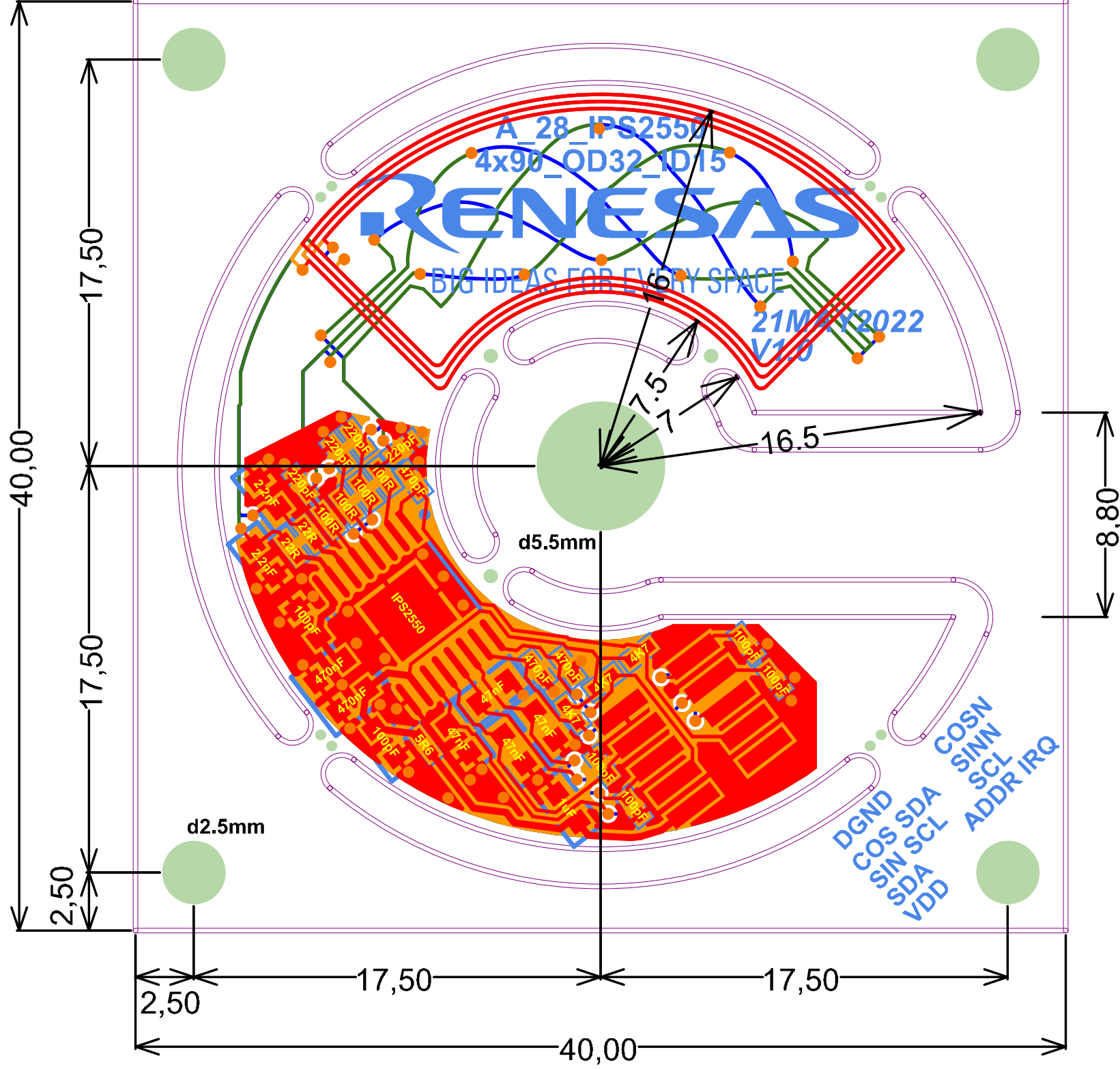
C_ADJ = To be adjusted according to coil inductivity. Calculate C_TX with the given formula.
C_ADJ = 2 x C_TX
It's recommended to use C0G or NP0 ceramic capacitors
Use dielectric strength Vr >= 50V X7R capacitors for C7 + (C10 .. C22)

LEGEND

- Component Size 0603
- Component Size 0402
- Net Name
- Component Placement Suggestion
- Optional Component

Project name	A_28_V10_IPS2550_4x90_OD32_ID15.PrfPcb	Version	1.0
Sheet title	A_28_V10_IPS2550_4x90_OD32_ID15	Size	A3
File name	A_28_V10_IPS2550_4x90_OD32_ID15.SchDoc		
Date	26.07.2022	Drawn by	B.GOMBOR
	<i>SYSP. APP. ENG. TEAM</i>	Sheet	1 of 1





A_28_IPS2550
4x90_OD32_ID15

RENESAS

BIG IDEAS FOR EVERY SPACE

21MAY2022
V1.0
















DGND
COS SDA
SIN SCL
VDD
COSN
SINN
SCL
ADDR IRQ

PCB Manufacturing requirements

Project Name	A_28_V10_IPS2550_4x90_OD32_ID15.PrjPcb
Number of copper layers	4
PCB Base material	FR-4
Final PCB Thickness	1.55mm +/-10%
Thickness of copper coating	35um
Final cover	ENIG
Minimal copper width	0.15
Minimal copper to copper distance	0.15mm
Via hole/pad diameter	Through-hole (1:4) 0.2/0.5mm
Slotted holes	Yes, see milling paths
Panel size	40x40mm
Silk screen color	White on TOP
Solder mask color	Green

Board Stack Report

Stack Up		Layer Stack			
Layer	Board Layer Stack	Name	Material	Thickness	Constant
1		Top Paste			
2		Top Overlay			
3		Top Solder	Solder Resist	0,010mm	3,5
4		Top Layer	Copper	0,035mm	
5		Dielectric 1	PP-022	0,208mm	4,5
6		Inner Layer 1	Copper	0,035mm	
7		Core	Core-042	0,991mm	4,6
8		Inner Layer 2	Copper	0,035mm	
9		Dielectric 2	PP-022	0,208mm	4,5
10		Bottom Layer	Copper	0,035mm	
11		Bottom Solder	Solder Resist	0,010mm	3,5
12		Bottom Overlay			
13		Bottom Paste			
	Height : 1,567mm				

Designator	Value	Quantity	Footprint
D1, D2, D3		3	SOT23-BAT54X
P1		1	62101021021
C22	1uF	1	C0603 3D
C1, C2	2.2nF	2	C0603 3D
R1, R2, R3	4K7	3	R0402 3D
R14	5R6	1	R0402 3D
R12, R13	22R	2	R0402 3D
C12, C13, C14, C15	47nF	4	C0603 3D
C9, C10	100pF	2	C0603 3D
C18, C19, C20, C21	100pF	4	C0402 3D
R5, R7, R9, R11	100R	4	R0402 3D
C3, C4, C5, C6	220pF	4	C0402 3D
C8, C11	470nF	2	C0603 3D
C7, C16, C17	470pF	3	C0402 3D
U1	IPS2xxx	1	TSOP65P640X120_HS-17N

