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REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

F

F

# HSP50415EVAL1 SCHEMATICS

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PAGE 2: HSP50415  
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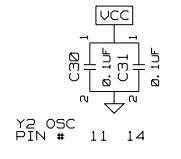
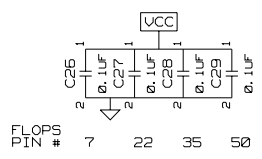
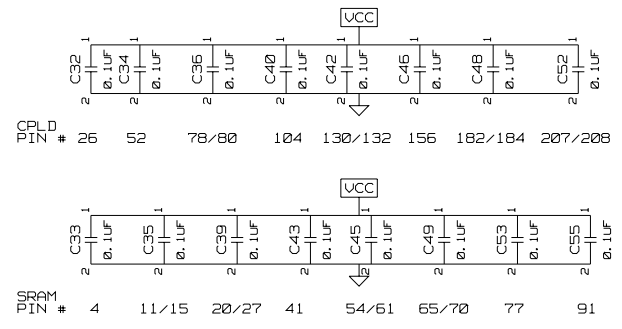
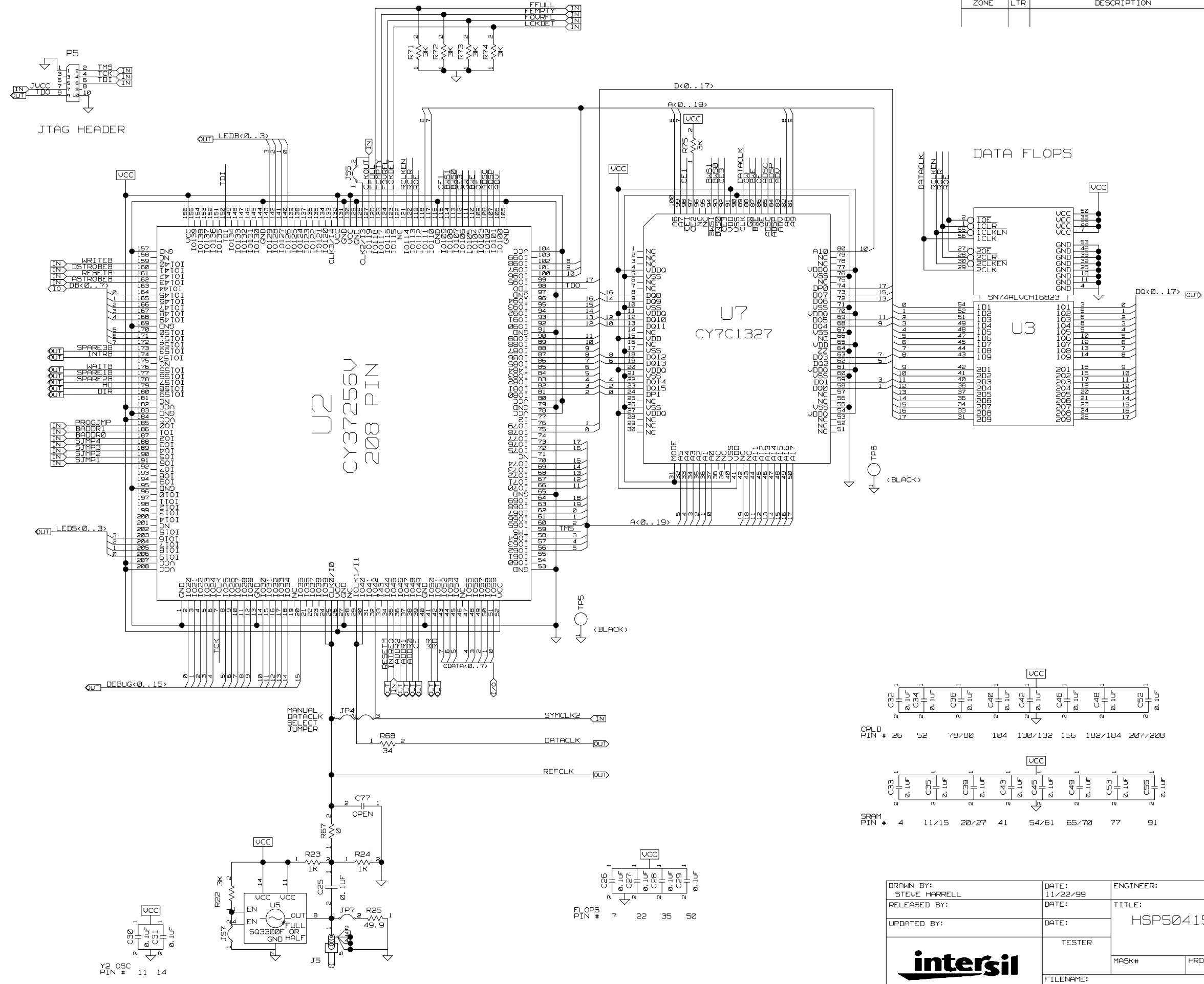
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DRAWN BY: STEVE HARRELL	DATE: 11/22/99	ENGINEER:	DATE:
RELEASED BY:	DATE:	TITLE: HSP50415EVAL1	
UPDATED BY:	DATE:		
	TESTER:	MASK#	HRDWR ID
	FILENAME:	REV. B2	
	SHEET 1 OF 4		



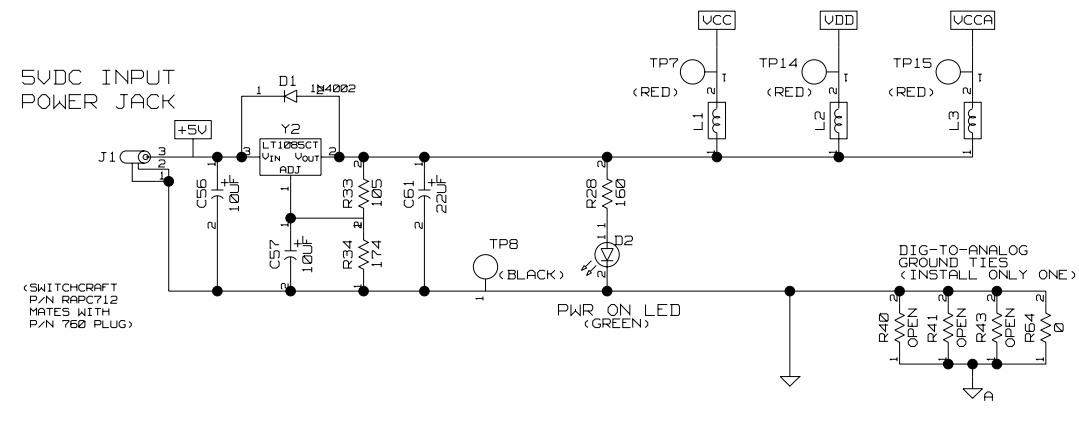
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ZONE	LTR	DESCRIPTION	DATE	APPR.



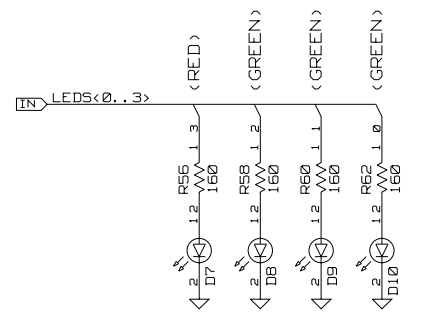
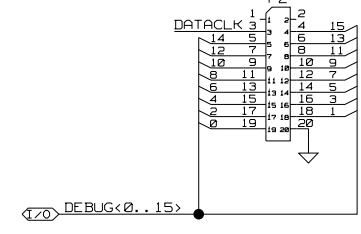
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UPDATED BY:	DATE:	TESTER:	MASK#
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		3 OF 4	

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

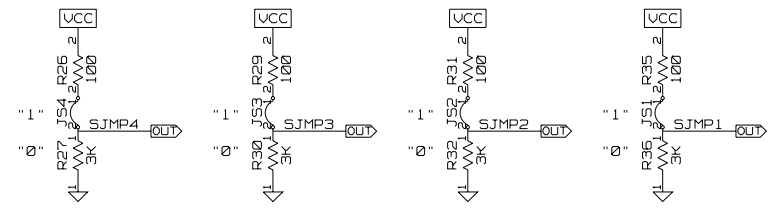
3.3VDC POWER DISTRIBUTION



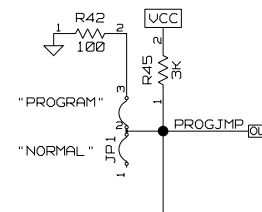
CPLD DEBUG



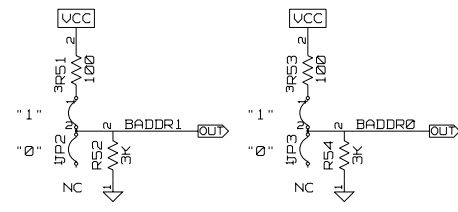
BOARD REVISION SOLDER JUMPERS



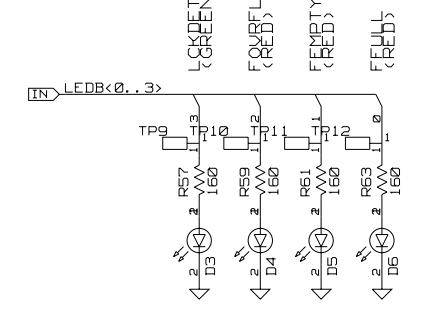
CPLD JTAG JUMPER



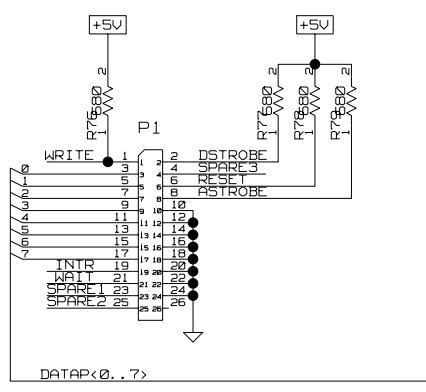
BOARD ADDRESS JUMPERS



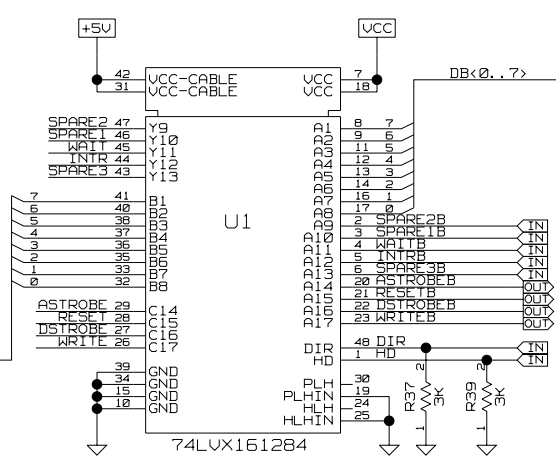
'415 STATUS LEDs



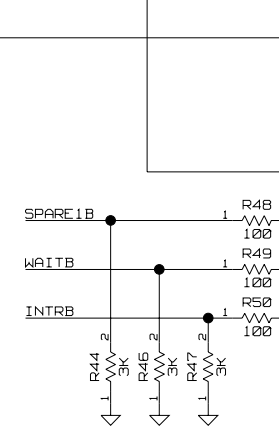
IDC26 PIN HEADER (HOST PRN INTERFACE)



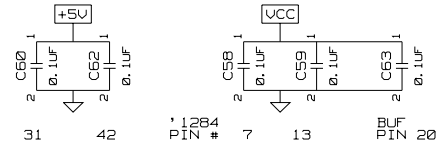
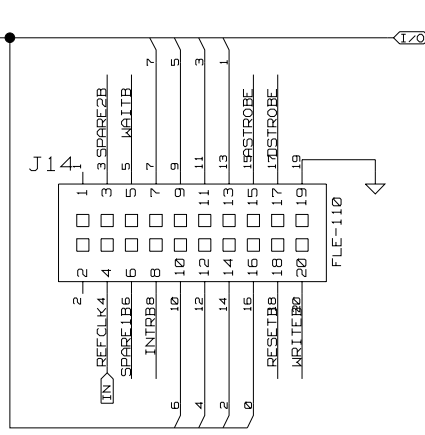
IEEE1284 TRANSCEIVER



JTAG BUFFER



HOST DEBUG



DRAWN BY: STEVE HARRELL	DATE: 11/22/99	ENGINEER:	DATE:
RELEASED BY:	DATE:	TITLE: HSP5041SEVAL 1	
UPDATED BY:	DATE:	TESTER:	
		MASK#	HRDWR ID
		REV. B2	
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