

Product Change Notification

Product Change Notification Number: PDF-033

Notification Date: Nov 28, 2017

Title: 64-Mbit Standard Serial Flash® (AT25QF641) – Product Improvement Changes			
Affected Product(s): AT25QF641 All packages, variants, SL codes, CAN codes and QS codes.			
Reason for Change:	<input type="checkbox"/> Material / Composition	<input type="checkbox"/> Design / Firmware	<input type="checkbox"/> Manufacturing Location
	<input type="checkbox"/> Processing / Manufacturing	<input checked="" type="checkbox"/> Configuration(s)	<input type="checkbox"/> Quality / Reliability
Change Description: Improved Write Status Register command operation to match customer requirements. Removed extended operation of 133MHz. See attached Errata			
Quantifiable Impact on Quality & Reliability: No change in Quality or Reliability			
Customer Impact and Recommended Action: <ul style="list-style-type: none"> Extended operation of 133MHz removed, Full 104MHz operation unchanged: no customer impact. Write Status Register command has changed to improve product compatibility. 			
Qualification Data: <i>Request the qualification report at</i> pcn@adestotech.com			
	<input type="checkbox"/> Available	<input type="checkbox"/> Target available date (mm/dd/yr):	<input checked="" type="checkbox"/> Not Applicable
Implementation Date:	November 30, 2017		
Samples: <i>To order samples, contact an authorized distributor, Adesto manufacturing Representative or visit</i> PCN@adestotech.com			
Adesto Contact: PCN@adestotech.com			
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Errata

In previous releases of this product (products shipped with a date code prior to 2217), the Write Status Register command operated differently. Previously, when executing the 01H command, if CS was driven high after the eighth clock, the CMP, QE and SRP1 bits were cleared to 0. In this release of the product, when CS is driven high after the eighth clock, the CMP, QE and SRP1 bits are not cleared and the CMP, QE and SRP1 bits retain their settings.