Product Change Notification

Product Change Notification Number: PDF-033 **Notification Date: Nov 28, 2017**

Title: 64-Mbit Standard Serial Flash® (AT25QF641) – Product Improvement Changes

Affected Product(s): AT25QF641

All packages, variants, SL codes, CAN codes and QS codes.

Reason for Change:

☐ Material / Composition ☐ Design / Firmware ☐ Manufacturing Location

☐ Processing / Manufacturing ☒ Configuration(s) ☐ Quality / Reliability

Change Description:

Improved Write Status Register command operation to match customer requirements. Removed extended operation of 133MHz.

See attached Errata

Quantifiable Impact on Quality & Reliability:

No change in Quality or Reliability

Customer Impact and Recommended Action:

- Extended operation of 133MHz removed, Full 104MHz operation unchanged: no customer impact.
- Write Status Register command has changed to improve product compatibility.

Qualification Data:

Request the qualification report at pcn@adestotech.com

☐ Available ☐ Target available date (mm/dd/yr): ☑ Not Applicable

Implementation Date: November 30, 2017

Samples: *To order samples, contact an authorized distributor, Adesto manufacturing Representative or visit* PCN@adestotech.com

Adesto Contact: PCN@adestotech.com

CUSTOMER ACKNOWLEDGEMENT OF RECEIPT: Adesto requests your acknowledgement of the receipt of this Notice. Please email to *PCN@adestotech.com* to grant approval or request additional information.
Adesto will deem this change accepted unless specific conditions of acceptance are received via an email addressed *to* *PCN@adestotech.com* **within 30 days from the date of this notice.**

Errata

In previous releases of this product (products shipped with a date code prior to 2217), the Write Status Register command operated differently. Previously, when executing the 01H command, if CS was driven high after the eighth clock, the CMP, QE and SRP1 bits were cleared to 0. In this release of the product, when CS is driven high after the eighth clock, the CMP, QE and SRP1 bits are not cleared and the CMP, QE and SRP1 bits retain their settings.