PRODUCT CHANGE NOTICE

Data Sheet and Wafer Fabrication Site Change for Intersil Product EL9115*

Refer to:
PCN11102

Date: October 3, 2011

October 3, 2011

To: Our Valued Intersil Customer

Subject: **Data Sheet and Wafer Fabrication Site Change for Intersil Product EL9115* –**
NXP Semiconductor Nijmegen, Netherlands

This notice is to inform you that Intersil has qualified the NXP Semiconductor facility in Nijmegen, the Netherlands for wafer fabrication of the EL9115* HS6 technology products. The change in wafer fabrication site is necessary as the NXP facility in Fishkill, New York has discontinued manufacturing operations. The HS6 wafer fabrication operations have been relocated from the NXP Fishkill to the NXP Nijmegen facility. The data sheet has been updated to align the specification with the characteristics of the product (silicon) fabricated at the NXP Nijmegen facility. The old and new DC Electrical Specifications tables with the changed areas shaded in yellow are included on the following pages of this notice. The updated data sheet is available on the Intersil web site at http://www.intersil.com/data/fn/fn7441.pdf. As of this notice, the data sheet updates and product qualification activities are complete.

Products affected:

EL9115ILZ	EL9115ILZ-T7	EL9115ILZ-T7S2714	EL9115ILZS2714
EL9115ILZ-T13	EL9115ILZ-T7R5504	EL9115ILZR5504	

The NXP Nijmegen facility is ISO 9001:2008 and ISO/TS 16949:2002 certified. The product and site qualification plans are designed using JEDEC and other applicable industry standards to confirm form, fit, function, or interchangeability of the product. A summary of the qualification results is included for reference. The remainder of the manufacturing operations will continue to be processed to previously established conditions and systems. Product affected by this change is identifiable via Intersil's internal traceability system.

Intersil will take all necessary actions to conform to agreed upon customer requirements and to ensure the continued high quality and reliability of Intersil products being supplied. Customers may expect to receive product from either the current or the newly qualified sites and screened to the updated data sheet beginning ninety days from the date of this notification or earlier with approval.

If you have concerns with this change notice, Intersil must hear from you promptly. Please contact the nearest Intersil Sales Office or call the Intersil Corporate line at 1-888-468-3774, in the United States, or 1-321-724-7143 outside of the United States.

Regards,

Jon Brewster

Jon Brewster
Intersil Corporation

PCN11102

CC: J. Touvell J. McNamara J. Yun P. Randhawa S. Hsiung K. Tucker

EL9115 Qualification Summary – PCN11102

Legend

Fail	Warning	Pass	QBE	Waived	NA

Reliability Test	EL9115 fab'ed using NXP Nijmegen HS6 Process	Comments
High Temperature Operating Life	SRN110188 Rev 0 0/78 125C 24hr completed 2011-06-23 disposition=A SRN110188 Rev 1 0/80 125C 168hr completed 2011-06-09 disposition=A	Testing Passed
Product Electrical Characterization	Performed by Product Engineering	
ESD Characterization	Performed by Product Engineering HBM = 3000V MM = 250V CDM = 1000V	
Latch-up Characterization	Performed by Product Engineering Latch Up Pass Level A Class II @85C	

Old Data Sheet Table – PCN11102

DC Electrical Specifications $V_{SA}+ = V_A+ = +5V$, $V_{SA}- = V_A- = -5V$, $T_A = +25°C$, exposed die plate = -5V, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
V+	Positive Supply Range		+4.5		+5.5	V
V-	Negative Supply Range		-4.5		-5.5	V
G_0	Gain Zero Delay	X2 = 5V, 150Ω load	1.81	1.89	2.04	
G_m	Gain Mid Delay		1.66	1.84	2.04	
G_f	Gain Full Delay		1.52	1.79	2.04	
DG_m0	Difference in Gain, 0 to Mid		-7.5	-2.5	2.5	%
DG_f0	Difference in Gain, 0 to Full		-13.5	-6.0	2.5	%
DG_fm	Difference in Gain, Mid to Full		-10.0	-2.6	4.0	%
V_{IN}	Input Voltage Range	Gain falls to 90% of nominal	-0.7		1.3	V
I_B	Input Bias Current			1	5	µA
R_{IN}	Input Resistance			10		MΩ
V_{OS_0}	Output Offset 0 Delay	X2 = +5V, 75 + 75Ω load	-200	-150	60	mV
V_{OS_M}	Output Offset Full Delay		-200	-140	60	mV
V_{OS_F}	Output Offset Mid Delay		-200	-130	60	mV
Z_{OUT}	Output Impedance	Chip enable = +5V	4.5	5	6.3	Ω
		Chip enable = 0V		1		MΩ
+PSRR	Rejection of Positive Supply	X2 = +5V into 75 + 75Ω load		-38		dB
-PSRR	Rejection of Negative Supply	X2 = +5V into 75 + 75Ω load		-53		dB
I_{SP}	Supply Current (Note 1)	Chip enable = +5V current on V_{SP}	75	87	115	mA
I_{SM}	Supply Current (Note 1)	Chip enable = +5V current in V_{SM}	-10.5	-8.6	-7	mA
I_{SMO}	Supply Current (Note 1)	Chip enable = +5V current in V_{SMO}	-13	-11.6	-10	mA
I_{SPO}	Supply Current (Note 1)	Chip enable = +5V current in V_{SPO}	10	11.8	15.5	mA
ΔI_{SP}	Supply Current (Note 1)	Increase in I_{SP} per unit step in delay		0.9		mA
$I_{SP\ OFF}$	Supply Current (Note 1)	Chip enable = 0V current in V_{SP}		1.6		mA
I_{OUT}	Output Drive Current	10Ω load, 0.5V drive, X2 = 5V	30			mA
L_{HI}	Logic High	Switch high threshold		1.25	1.6	V
L_{LO}	Logic Low	Switch low threshold	0.8	1.15		V

New Data Sheet Table – PCN11102

DC Electrical Specifications $V_{SA}+ = V_A+ = +5V$, $V_{SA}- = V_A- = -5V$, $T_A = +25°C$, exposed die plate = -5V, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
V+	Positive Supply Range		+4.5		+5.5	V
V-	Negative Supply Range		-4.5		-5.5	V
G_0	Gain Zero Delay	X2 = 5V, 150Ω load	1.81	1.9	2.04	
G_m	Gain Mid Delay		1.64	1.8	1.97	
G_f	Gain Full Delay		1.46	1.7	1.97	
DG_m0	Difference in Gain, 0 to Mid		-10	-4	2.3	%
DG_f0	Difference in Gain, 0 to Full		-17.5	-9	0.3	%
DG_fm	Difference in Gain, Mid to Full		-15	-5	4	%
V_{IN}	Input Voltage Range	Gain falls to 90% of nominal	-0.7		1.2	V
I_B	Input Bias Current			1	5	µA
R_{IN}	Input Resistance			10		MΩ
V_{OS_0}	Output Offset 0 Delay	X2 = +5V, 75 + 75Ω load	-90	0	90	mV
V_{OS_M}	Output Offset Full Delay		-90	0	90	mV
V_{OS_F}	Output Offset Mid Delay		-90	0	90	mV
Z_{OUT}	Output Impedance	Chip enable = +5V	4.5	5	6.3	Ω
		Chip enable = 0V		1		MΩ
+PSRR	Rejection of Positive Supply	X2 = +5V into 75 + 75Ω load		-38		dB
-PSRR	Rejection of Negative Supply	X2 = +5V into 75 + 75Ω load		-53		dB
I_{SP}	Supply Current (Note 5)	Chip enable = +5V current on V_{SP}	75	87	115	mA
I_{SM}	Supply Current (Note 5)	Chip enable = +5V current in V_{SM}	-15.25	-12.5	-9.75	mA
I_{SMO}	Supply Current (Note 5)	Chip enable = +5V current in V_{SMO}	-15.25	-13	-11	mA
I_{SPO}	Supply Current (Note 5)	Chip enable = +5V current in V_{SPO}	10	11.8	15.5	mA
ΔI_{SP}	Supply Current (Note 5)	Increase in I_{SP} per unit step in delay		0.9		mA
$I_{SP\ OFF}$	Supply Current (Note 5)	Chip enable = 0V current in V_{SP}		1.6		mA
I_{OUT}	Output Drive Current	10Ω load, 0.5V drive, X2 = 5V	40			mA
L_{HI}	Logic High	Switch high threshold		1.25	1.6	V
L_{LO}	Logic Low	Switch low threshold	0.8	1.15		V