

Integrated Device Technology, Inc. 6024 Silver Creek Valley Road, San Jose, CA - 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

	11102				
PCN #: W19	11-01(R1)	DATE: 2	27-May-2020	MEANS OF DISTIN	GUISHING CHANGED DEVICES:
Product Affected:	F1431BNBGk	K, F1431BNBGK8	3	□ Product Mark	
				Back Mark	
					Datecode 2018 and above
				□ Other	
Date Effective:	19-Mar-2020				
Contact:	PCN DESK			Attachment:	Yes No
E-mail:	idt-pcn@lm.rene	sas.com		Samples: N/A	
DESCRIPTION A	AND PURPOSE C	OF CHANGE:			
Die Technolog	gy				
Wafer Fabrica	tion Process) at the request of the customer. The
□ Assembly Proc	cess				omers that the MIM canacitor
Equipment					
□ Material			device robustn	ess. This change is to a	address the CGR (Capacitive Guard
□ Testing	C '4-				otible to peeling of nitride layer
Data Sheet	g Site		between metal	layers.	
\Box Other				a a	N
				Current	New
		MIMCAP Architecture		CGR	ТРМ
There is no expec	eted change to the p	roduct quality or	• •	rmance.	
				-	-
• • • •	*		ID1 does not re	eceive acknowledgement	ht within 30 days of this notice
	-	·	ured after the p	ocess change effective	date until the inventory
			area arter the pi	ocess change effective	date until the inventory
on the earlier ver	sion has been deple	eted.			
Customer:			_] Approval for sl	hipments prior to effective date.
Name/Date:			E-	Mail Address:	
Title:			Pl	none#/Fax#:	
CUSTOMER CO	OMMENTS:				
IDT ACKNOWI	LEDGMENT OF I	RECEIPT:			
	we: 19-Mar-2020 PCN DESK Attachment: Yes No idt-pcn@lm.renesas.com Samples: N/A OON AND PURPOSE OF CHANGE: Revision 1: This revised notice is to change the part number from process F1431NBGK(8) to F1431BNBGK(8) at the request of the customer. The effective date remains unchanged. The notification is to advise our customers that the MIM capacitor architecture has been re-designed by the foundry WaveTck to improve device robustness. This change is to advises to CGR (Capacitive Guard Ring) MIMCAP design that is susceptible to pecling of nitride layer between metal layers. et MIMCAP Availatettee CGR TY/QUALIFICATION SUMMARY: expected change to the product quality or reliability performance. TPM RACKNOWLEDGMENT OF RECEIPT: indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail roval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice sumed that this change is acceptable. is the right to ship either version manufactured after the process change effective date until the inventory erversion has been depleted.				
RECD. BY:				DATE:	



Product Qualification Report (Re-Spin)

Date: 11/19/2019

Product:	F1431ZJNBGK		
Fab Base:	GRF2014B C2018	Process Technology:	ED25_5V GaAs E/D-HEMT
Package Type:	NBG24	Fab Location:	WaveTek
Assembly Location:	Carsem	Qual Plan#:	Q19-11-005

Test Description	Conditions	Sample Size	Results (rej/SS)	Comments
Early Life Failure Rate	JESD22-A108, Ta 97°C, 5.0V, 48 hrs	320	0/320	Pass
ESD: Human Body Model	JESD22-A114 (JS-001) Classification ±2000V	3	0/3	Pass
ESD: Charged Device Model	JESD22-C101 Classification ±500V	3	0/3	Pass
Latch-Up	JESD78, T _A at 85°C	6	0/6	Pass
Electrical Characterization	Datasheet	3	Results reported in Datasheet	Complete

Package Qual					
Temperature Cycling ¹	JESD22-A104, -55°C to +125°C, 700 cycles	25	0/25, x3 lots	Pass	
Highly Accelerated Temperature and Humidity stress (Biased) ¹	JESD22-A110, +130°C, 85% RH, Vcc _{max} , 96 hrs	25	0/25, x3 lots	Pass	
High Temperature Storage Life ¹	JESD22-A103, +150°C, 1000 hrs	25	0/25, x3 lots	Pass	
Bond Pull Strength	M2011	5	0/5, x3 lots	Pass	
Bond Shear	JESD22-B116	5	0/5, x3 lots	Pass	
Physical Dimension	JESD22-B100 (Per applicable IDT Package Outline Drawing)	30	0/30, x3 lots	Pass	
Solderability Test MIL-STD-883 (Method 2003), J-STD-002D		5	0/5, x3 lots	Pass	

Note:

1. Preconditioning per JESD22-A113, MSL 1 (260°C)