Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: **U1306-01** DATE: **June 25, 2013**

Product Affected: 6V49205ANLGI
6V49205ANLGI8
6V49205APAGI
6V49205APAGI8

Date Effective: **July 25, 2013**

MEANS OF DISTINGUISHING CHANGED DEVICES:

- ■ Product Mark
- ☐ Back Mark
- ☐ Date Code
- ☐ Other

Change in Ordering Part Number. Refer to Attachment I.

Contact: Bimla Paul
Title: Product Quality Assurance
Phone #: (408) 574-6419
Fax #: (408) 284-8362
E-mail: Bimla.Paul@idt.com

Attachment: ■ Yes ☐ No

Samples: Contact your local sales representative for sample and datasheet requests.

DESCRIPTION AND PURPOSE OF CHANGE:

- ☐ Die Technology
- ☐ Wafer Fabrication Process
- ☐ Assembly Process
- ☐ Equipment
- ☐ Material
- ☐ Testing
- ☐ Manufacturing Site
- ☐ Data Sheet
- ■ Other - Die revision

This notification is to advise our customers of a silicon die revision. The current die revision A will be changed to revision B.

IDT requests customers to use "B" revision in their newer design/projects and switch existing design/projects to "B" revision as soon as possible.

RELIABILITY/QUALIFICATION SUMMARY:

There is no expected change to the product quality or reliability performance.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.
IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____ ☐ ***Approval for shipments prior to effective date.***

Name/Date: _____ E-Mail Address: _____

Title: _____ Phone # /Fax #: _____

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

ATTACHMENT I - PCN #: U1306-01

PCN Type: Die Revision Change

Data Sheet Change: Yes

Detail of Change:

This notification is to advise our customers of a silicon die revision. The current die revision A will be changed to revision B.

IDT requests customers to use "B" revision in their newer design/projects and switch existing design/projects to "B" revision as soon as possible.

Revision B has the following improvements and design enhancements/features:

1) Add latch on pin 11 to select PCI Express as 125MHz or 100MHz (Internal pull up - default 100MHz) Byte 6 bit 4.

2) Add latch on pin 44 to select DDRCLK output as 100MHz or 66.66MHZ (Internal pull up - default 66.66MHz) Byte 6 bit 5.

3) Improve phase noise on 125MHz.

4) Add additional spread selections for DDR/SYS_CCB (B0b7) Down spread -1%, -1.25%, -1.5%, -2%.

There is no change to thermal and MSL specification due to this die revision.

There will be a change in ordering part number and device top mark.

There is no change in die technology/process.

Table 1

Old Ordering Part Number	New Ordering Part Number
6V49205ANLGI	6V49205BNLGI
6V49205ANLGI8	6V49205BNLGI8
6V49205APAGI	6V49205BPAGI
6V49205APAGI8	6V49205BPAGI8

Integrated Device Technology, Inc.

Qualification Test Result Summary

Foundry: TSMC

Technology Information: CMOS 0.18um 3.3V

Qualification Test Result Summary – JESD47 Recommended Tests

Test /Conditions	Conditions	Sample Size	Rejects	Comments
High Temperature Operating Life (Dynamic)	JESD22-A108D, +125℃, Vccmax @ 1000 hours or equivalent	77 77 77	0 0 0	
Temperature Cycle	JESD22-A104D, -55℃ to +125℃, 700 cycles	25 25 25	0 0 0	
High Temperature Storage Bake	JESD22-A-103D, 150℃, 1000 hrs	25 25 25	0 0 0	
Highly Accelerated Stress Test (HAST)	EIA/JESD22-A110D, 130℃/85%R.H. Vcc max for 100 hours.	25 25 25	0 0 0	
Ball Shear Test	JESD22-B116A, Ball Shear Strength	5	0	

Note: For HAST and Temperature Cycle, samples have been subjected to pre-conditioning per JESD22-A113