Product Change Notice (PCN)

Subject: Add Alternate Manufacturing Locations for P9320S-3AHGI8
Publication Date: 2/19/2020
Effective Date: 5/19/2020

Revision Description:
Initial Release

Description of Change:
This PCN notice is to add Sigurd, Taiwan and Amkor, Taiwan as an alternate pre bump sort location and bump location respectively.

The current pre bump sort location and bump location are at KYEC, Taiwan and SFA, Korea respectively.

Refer the below table marked in blue font for the added manufacturing locations by combinations.

No	Fab Location	Pre Bump Sort Location	Bump Location	Post Bump Sort Location	Backend Location
1	TSMC Fab8	KYEC, Taiwan	SFA, Korea	SFA, Korea	SFA, Korea
2	TSMC Fab6	KYEC, Taiwan	SFA, Korea	SFA, Korea	SFA, Korea
3	TSMC Fab8	KYEC, Taiwan	SFA, Korea	Sigurd, Taiwan	Sigurd, Taiwan
4	TSMC Fab6	KYEC, Taiwan	SFA, Korea	Sigurd, Taiwan	Sigurd, Taiwan
5	TSMC Fab8	Sigurd, Taiwan	ATT, Taiwan	Sigurd, Taiwan	Sigurd, Taiwan
6	TSMC Fab6	Sigurd, Taiwan	ATT, Taiwan	Sigurd, Taiwan	Sigurd, Taiwan

Note: Combination 1 to 4 are the existing manufacturing locations, 5 & 6 are added manufacturing locations.

The materials details of the current bump location and the alternate bump location is shown in the below table.

Parameters	Existing Bump Location SFA, Korea	Alternate Bump Location ATT, Taiwan
RDL (µm)	TiW / Cu /Cu (0.1 / 0.15 / 5.5 ± 1.5)	TiW / Cu /Cu (0.1 / 0.15 / 5.5 ± 1.5)
UBM (µm)	Ti / Cu / Ni / Au (0.1 / 0.15 / 2 ± 0.5 / 0.5)	Ti / Cu / Ni / Au (0.1 / 0.15 / 2 ± 0.5 / 0.5)
POLYMIDE/ PASSIVATION 1 and 2	Polymide HD4100 Thickness 7 ± 2µm	Polymide HD4100 Thickness 7 ± 2µm
BACK SIDE COATING	Lintech LC2850 Thickness 25µm	Lintech LC2850 Thickness 25µm
SOLDER BALL (Bump)	SAC105	SAC105
SOLDER BALL DIAMETER (mm)	0.268 ± 0.025 (268 ± 25µm)	0.25 ± 0.025 (250 ± 25µm)

There is no change in the pre-bump sort processing flows. Load boards and test programs are the same at both the qualified facilities. The electrical test correlation has been completed and based on the test results we do not anticipate any impact on device performance. The testing is fully compatible and transferrable between the test facilities with no change to the test coverage.

Affected Product List: P9320S-3AHGI8

Reason for Change:
This change will allow the flexibility to ship from all the qualified facilities and will provide the increased capacity, flexibility and shorter lead time to meet market demand.

Impact on Fit, Form, Function, Quality & Reliability:
The change will have no impact on the form, fit, function, quality, reliability and environmental compliance of the products.

Product Identification:
Assembly lot# with prefix “AT” denote bump location at ATT, Taiwan wherein in this case, the pre bump sort location will be at Sigurd, Taiwan.

Qualification Status: Completed. Refer Appendix A. ATE correlation data available on request.
Sample Availability Date: Available upon request
Device Material Declaration: Available upon request

Note:

1. Acknowledgement must be received by Renesas within 30 days or Renesas will consider the change as approved.

2. If timely acknowledgement is provided by Customer, then Customer shall have 90 days from the date of receipt of this PCN to make any objections to this PCN. If Customer fails to make objections to this PCN within 90 days of the receipt of the PCN then Renesas will consider the PCN changes as approved.

3. If customer cannot accept the PCN then customer must provide Renesas with a last time buy demand and purchase order.

For additional information regarding this notice, please contact idt-pcn@lm.renesas.com

Integrated Device Technology, Inc.

Qualification Report
WLCSP

General Information

Qualification Type	**Facility/Package**	Package Type	**AHG80**
Assembly Location	**Amkor-Taiwan**	Package Family	**WLCSP**
Report Date	**February 12, 2020**	Packages Covered	**AHG79, AHG54, AWG40, AWG36**

Package Dimension

Package	Body Size	Pitch
DSBGA-80 (AHG80)	4.175 x 4.175 mm	0.40 mm

Standard Material

Dielectric Materials	RDL Metalization	UBM	Bump Material	Bump Diameter
Polyimide	TiW (0.1)/Cu(0.15)/Cu(5.5 ± 1.5)	Ti(0.1)/Cu(0.15)/Ni(2 ± 0.5)/Au(0.5)	SAC105	250 ± 25µm

Qualification Data

Package Level	**Reference Spec / Conditions**	**Results (rej/SS)**
Physical Dimension	Case Outline Drawing	0/20, x3 lots
Solder Ball Shear	QEC-Q100-010	0/5, x3 lots
UHAST	JESD22-A110 (130°C/85%RH, 100hrs, Ubiased)	0/77, x3 lots
Temperature Cycle Test	JESD22-A104 (-55°C to 125°C, 700cycles)	0/77, x3 lots
High Temperature Storage Test	JESD22-A103 (150°C, 1000hrs)	0/25, x3 lots

Board Level	**Reference Spec / Conditions**	**Results**
Temperature Cyling	IPC-9701, TC3 (-40°C <-> +125°C, 60 mins per cycle)	5% failure at 562 cycles
Drop Test	JESD22-B111, Cond B (1500 Gs, 0.5 msec duration, half-sine pulse).	10% failure at 628 drops