



Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA - 95054

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: **SR-0203-02** DATE: March 15, 2002
Product Affected: IDT7164 and IDT6116 Family

Date Effective: June 15, 2002

MEANS OF DISTINGUISHING CHANGED DEVICES:

- ☐ Product Mark
☐ Back Mark
☒ Date Code Top mark will have "4" following the
☐ Other die revision. Refer to page 1 of attachment

Contact: George Snell

Title: Quality Assurance Manager

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Attachment: ☒ Yes ☐ No

Samples: Available upon request

DESCRIPTION AND PURPOSE OF CHANGE:

- ☐ Die Technology
☒ Wafer Fabrication Process
☐ Assembly Process
☐ Equipment
☐ Material
☐ Testing
☒ Manufacturing Site
☐ Data Sheet
☐ Other

To consolidate Wafer Fab production from Salinas, California (Fab 2) to Hillsboro, Oregon (Fab 4). These qualified products will be transferred to IDT's Wafer Fab facility in Hillsboro, Oregon. These devices will be upgraded from Cmos 7 to Cmos 8. Cmos 8 is an existing qualified process at Fab 4.

RELIABILITY/QUALIFICATION SUMMARY:

Qualification testing will verify that there is no change to the product reliability. Qualification details are available upon request.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.

IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____

☐ **Approval for shipments prior to effective date.**

Name/Date: _____

E-Mail Address: _____

Title: _____

Phone# /Fax# : _____

CUSTOMER COMMENTS:

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____

DATE: _____



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PCN Type: Fab Site Change

Data Sheet Change None Expected

Detail of Change Transfer existing qualified products from Salinas, California Wafer Fab Facility (Fab 2) to Hillsboro, Oregon Wafer Fab Facility (Fab 4).

Part Name	Current Wafer Fab				Transfer Wafer Fab			
	Manufacturing Site	Technology	Wafer Size	Die Revision	Manufacturing Site	Technology	Wafer Size	Die Revision
7164L	Salinas, CA	Cmos 7	6 inch	L	Hillsboro, OR	Cmos 8	8 inch	L4
6116L	Salinas, CA	Cmos 7	6 inch	L	Hillsboro, OR	Cmos 8	8 inch	L4

Conversion schedule (Estimated)

Base Device

7164L4
6116L4

Production Shipments and Sample Availability

June 15, 2002
June 15, 2002



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Qualification Plan: QS-0202-04

Expected Completion Date

6/1/2002

Test Vehicle

Plan
Actual
Results

7164L	Sample / Accept	LOT #1
Operating Life Test: Dynamic @+135°C, Vcc=4V for 750 hours	116 / 0	
High Temp. Storage Life Test (Unbiased, 1000 hours @+150°C)	77 / 0	
Bake & Ballshear Test @ 200°C / 4 ball bonds per device	5 / 0	
Temperature Cycling: (-65°C to +150°C, 500 cycles)	45 / 0	
HAST: (Biased, 100 Hrs. @+130°C, +85%RH, 3 Atm.)	45 / 0	
Autoclave:(Unbiased, 2 Atm Saturated Steam, +121°C, 168 Hrs)	45 / 0	
ESD Human Body Model	9 / 0	
ESD Charged Device Model	6 / 0	
Latch up: (Tested to 1.5X Vcc)	10 / 0	

Product release is based on qualification of initial lot.

Characterization Data: Characterization will be completed as part of product qualification and data available upon request. Characterization will verify that there is no change to existing data sheet parameters.



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Base Part Number	Current Die Rev	New Die Rev	Interface	Vcc	Bus Width	Depth	Density
IDT6116 Devices:							
IDT6116LA	L	L4	Asynch	5V	x8	2K	16K
IDT6116SA	L	L4	Asynch	5V	x8	2K	16K
IDT7164 Devices:							
IDT7164L	L	L4	Asynch	5V	x8	8K	64K
IDT7164S	L	L4	Asynch	5V	x8	8K	64K