Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA - 95054

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: SM-0402-03 DATE: 03/03/04
Product Affected: IDT70V35S/L, IDT70V34S/L
IDT70V25S/L, IDT70V24S/L, IDT70T35L,
IDT70T24L, IDT70T34L, IDT70T25L
Date Effective: 6/2/2004

MEANS OF DISTINGUISHING CHANGED DEVICES:
■ Product Mark Die revision on Top Mark
☐ Back Mark
☐ Date Code
☐ Other

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Attachment:: ■ Yes ☐ No

Samples: Refer to page 2 for sample availability

DESCRIPTION AND PURPOSE OF CHANGE:
■ Die Technology
■ Wafer Fabrication Process
☐ Assembly Process
☐ Equipment
☐ Material
☐ Testing
☐ Manufacturing Site
☐ Data Sheet
☐ Other

This change is to upgrade to a new technology (CMOS 11.5) and to shrink the die. This change is to improve manufacurability and allow for expanded product offerings.

RELIABILITY/QUALIFICATION SUMMARY:
Device qualification is in progress and will verify that there is no change to the device reliability.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:
IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.
IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____ ☐ ***Approval for shipments prior to effective date.***

Name/Date: _____ E-Mail Address: _____

Title: _____ Phone# /Fax# : _____

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____

ATTACHMENT - PCN #: SM-0402-03

PCN Summary
PCN Type: Change for Die Shrink

Commodity Memory

Forecast or Execute Execute

Planned or Unplanned Planned

Data Sheet Change N/A

Detail of Change The base device for each part is detailed on the attached product detail sheet. The new base device for future products listed on this PCN will be IDT70V35 "T". This product redesign will allow for IDT to expand product offerings and upgrade technology.

Die Step Details

Die Revision (step)	U	T
Wafer Fab Technology	Cmos 9	Cmos 11.5
# Poly Layers	3	1
# Metal Layers	2	3
Minimum Feature Size	0.35 um	0.18 um
Die Dimensions (sq mils)	32k	9.6k

Sample Availability: Beginning 04/30/04

Production Shipments: Customer shipments for this die revision will start 06/02/04 unless specifically requested.

Product Family:
3.3V Asynchronous Dual-Port SRAMs (x16 & x18 options only)
2.5V Asynchronous Dual-Port SRAMs (x16 & x18 options only)

Product Configuration:
x16, x18 (64K, 72K, 128K, 144K) Asynchronous Dual-Port SRAMs

Device:
IDT70V24, IDT70V25, IDT70V34, IDT70V35
IDT70T24, IDT70T25, IDT70T34, IDT70T35

Packages:
BF-100, BZ-108, GU-84, PL-84, PN-100

ATTACHMENT - PCN #: SM-0402-03

IDT70V35T Family of Parts

Part Number	Old Rev.	New Rev.	Interface	Vcc	Bus	Depth	Density
IDT70V35S/L	U	T	Async	3.3	x18	8K	144K
IDT70V34S/L	U	T	Async	3.3	x18	4K	72K
IDT70V25S/L	U	T	Async	3.3	x16	8K	128K
IDT70V24S/L	U	T	Async	3.3	x16	4K	64K
IDT70T35L	U	T	Async	2.5	x18	8K	144K
IDT70T34L	U	T	Async	2.5	x18	4K	72K
IDT70T25L	U	T	Async	2.5	x16	8K	128K
IDT70T24L	U	T	Async	2.5	x16	4K	64K

Qualification Plan #: QS-0312-01
Test Vehicle: 70V25T BGA100

Status: In Progress

TEST DESCRIPTION	Required Sample Size / # Fails	Expected Completion
Operating Life Test: JESD22-A108 Dynamic @+135°C, Vcc=6V for 750 hours or Vcc=4V for 750 hours	232/0	4/15/2004
Highly Accelerated Stress Test: JEDEC STD 22, Method A110, * Biased, @+130°C, +85%RH, 3 Atm, 100 hours	45/0	4/15/2004
Autoclave: EIA/JESD22-A102 @ 2 ATM, Saturated* Steam @ 121°C, 168 hours	45/0	4/15/2004
Temperature Cycling: JESD22-A104, Condition C, * -65°C to +150°C, 500 cylces	45/0	4/15/2004
High Temp Storage: JESD22-A103 +150°C, 1000 hours	77/0	4/15/2004
ESD: Human Body Model Mil-Std-883, method 3015	3/0	4/15/2004
ESD: Charged device Model JEDEC 22-101	3/0	4/15/2004
Latch-up EIA/JESD STD-78	10/0	4/15/2004

* Preconditioning per JESD22-A113B Level 3