Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: **N1603-01** Date: April 11, 2016
Product Affected: 8V54816NLG(8)

Date Effective: July 11, 2016

MEANS OF DISTINGUISHING CHANGED DEVICES:
- ■ Product Mark Change in ordering part#
- ☐ Back Mark
- ☐ Date Code
- ☐ Other

Contact: TSD Clock Team
E-mail: clocks@idt.com

Attachment: ■ Yes ☐ No
Samples: Samples are available now.

DESCRIPTION AND PURPOSE OF CHANGE:

- ☐ Die Technology
- ☐ Wafer Fabrication Process
- ☐ Assembly Process
- ☐ Equipment
- ☐ Material
- ☐ Testing
- ☐ Manufacturing Site
- ■ Data Sheet
- ■ Other - Die Revision Change

This notice is to advise our customers that the IDT Part 8V54816ANLG(8) is an updated version of the 8V54816NLG(8) to improve the overall jitter performance.

There is a minor change to the top metal. The is no change to the die/package technology or manufacturing. The change in datasheet parameters is shown in page 7, 8 and 9.

We are requesting a last time buy of the previous version by July 11, 2016.

RELIABILITY/QUALIFICATION SUMMARY:

There is no change in die technology/process.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.
IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____ ☐ ***Approval for shipments prior to effective date.***

Name/Date: _____ E-Mail Address: _____

Title: _____ Phone # /Fax #: _____

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____

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ATTACHMENT 1 - PCN #: N1603-01

PCN Type: Die Revision Change / Datasheet

Data Sheet Change: Yes

Detail of Change: This notice is to advise our customers that the IDT Part 8V54816ANLG(8) is an updated version of the 8V54816NLG(8) to improve the overall jitter performance.

There is a minor change to the top metal. The is no change to the die/package technology or manufacturing. The change in datasheet parameters is shown in page 7, 8 and 9.

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Table 1

Old Ordering Part Number	New Ordering Part Number
8V54816NLG	8V54816ANLG
8V54816NLG8	8V54816ANLG8

Qualification Test Plan and Result:

Qual Vehicle: 8V54816ANLG

Test Description	Test Method (Latest specs in effect)	Test Results (SS / Rej)
ESD: Human Body Model @ 2500V	Each IO Pin Individually to I/O	3/0
ESD: Charged Device Model @ 1500V	JESD22-C101	3/0
Latch-up	JESD78	3/0

FROM

8V54816

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{DD}	Power Supply Current				242	270	mA
I_{DDOb}	Total Output Supply Current					266	mA
IDDO_inc	Output Current				12		mA

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IL}	InputLow Voltage	S_A0, S_A1		-0.3		0.4	V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
tsl(o)	Output Slew Rate	Measured at the Differential Waveform, ±200mV from the Center	2		4	V/ns
tjit	Buffer Additive Phase Jitter,	fOUT = 125MHz, Integration Range 12kHz – 20MHz		0.346		ps
odc	Output Duty Cycle	fIN <= 200Mhz	40	50	60	%
tR/tF	Output Rise/Fall time	20% to 80%		300	550	ps

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
tsl(o)	Total Phase Jitter, RMS	fout = 156.25Mhz		0.245	0.5	ps

TO

8V54816A

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{DD}	Power Supply Current			258	295	mA
I_{DDOb}	Total Output Supply Current	0 Ports Configured as Outputs		63		mA
		15 Ports Configured as output Outputs		258	295	mA
IDDO_inc	Output Current Contribution, per output port			13		mA

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IL}	InputLow Voltage	S_A0, S_A1		-0.3		0.8	V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
tsl(o)	Output Slew Rate	Measured at the Differential Waveform, ±200mV from the Center	0.9	2.4	4	V/ns
tjit	Buffer Additive Phase Jitter,	fOUT = 125MHz, Integration Range 12kHz – 20MHz		0.32	0.5	ps
odc	Output Duty Cycle	fIN <= 200Mhz	45	50	55	%
tR/tF	Output Rise/Fall time	20% to 80%		380	741	ps

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
tsl(o)	Total Phase Jitter, RMS	fout = 156.25Mhz		0.247	0.5	ps