



Integrated Device Technology, Inc.  
6024 Silver Creek Valley Road, San Jose, CA 95138

## PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: <b>N1506-01</b> Product Affected: 8735-01 / 8735I-01 / 8735-21 / 8735I-21 (Refer to Table 1 for the affected part#)  Date Effective: November 18, 2015	Date: August 18, 2015	<b>MEANS OF DISTINGUISHING CHANGED DEVICES:</b> <input checked="" type="checkbox"/> Product Mark    Change in ordering part# <input type="checkbox"/> Back Mark <input type="checkbox"/> Date Code <input type="checkbox"/> Other
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Contact: TSD Clock Team E-mail: <a href="mailto:clocks@idt.com">clocks@idt.com</a>	Attachment: <input checked="" type="checkbox"/> Yes <input type="checkbox"/> No Samples: Samples are available now.
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**DESCRIPTION AND PURPOSE OF CHANGE:**

<input type="checkbox"/> Die Technology <input type="checkbox"/> Wafer Fabrication Process <input type="checkbox"/> Assembly Process <input type="checkbox"/> Equipment <input type="checkbox"/> Material <input type="checkbox"/> Testing <input type="checkbox"/> Manufacturing Site <input checked="" type="checkbox"/> Data Sheet <input checked="" type="checkbox"/> Other - Die Revision Change	<p>This notice is to advise our customers that the IDT Part 8735BI-01 / 8735BI-21 is an updated version of the 8735-01 / 8735-21 / 8735I-01 / 8735I-21 to improve the VCO stability for an overall better performance.</p> <p>There is a minor change to the top metal. There is no change to the die/package technology or manufacturing. The change in datasheet parameters is shown in page 3 and page 4.</p> <p>We are requesting a last time buy of the previous version by November 18, 2015.</p>
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**RELIABILITY/QUALIFICATION SUMMARY:**

There is no change in die technology/process.

**CUSTOMER ACKNOWLEDGMENT OF RECEIPT:**

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.

IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____	<input type="checkbox"/> <i>Approval for shipments prior to effective date.</i>
Name/Date: _____	E-Mail Address: _____
Title: _____	Phone # /Fax #: _____

**CUSTOMER COMMENTS:** \_\_\_\_\_

\_\_\_\_\_

\_\_\_\_\_

**IDT ACKNOWLEDGMENT OF RECEIPT:**

RECD. BY: \_\_\_\_\_ DATE: \_\_\_\_\_



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## PRODUCT/PROCESS CHANGE NOTICE (PCN)

### ATTACHMENT 1 - PCN #: N1506-01

**PCN Type:** Die Revision Change / Datasheet

**Data Sheet Change:** Yes

**Detail of Change:** This notice is to advise our customers that the IDT Part 8735BI-01 / 8735BI-21 is an updated version of the 8735-01 / 8735-21 / 8735I-01 / 8735I-21 to improve the VCO stability for an overall better performance.

There is a minor change to the top metal. There is no change to the die/package technology or manufacturing. The change in datasheet parameters is shown in page 3 and page 4.

We are requesting a last time buy of the previous version by November 18, 2015.

**Table 1**

Old Ordering Part Number	New Ordering Part Number
8735AK-01LF	8735BKI-01LF
8735AK-01LFT	8735BKI-01LFT
8735AKI-01LF	8735BKI-01LF
8735AKI-01LF-INT	8735BKI-01LF
8735AKI-01LFT	8735BKI-01LFT
8735AKI-01LFT-INT	8735BKI-01LFT
8735AY-01LF	8735BYI-01LF
8735AY-01LFT	8735BYI-01LFT
8735AYI-01LF	8735BYI-01LF
8735AYI-01LFT	8735BYI-01LFT
8735AK-21LF	8735BKI-21LF
8735AK-21LFT	8735BKI-21LFT
8735AM-21LF	8735BMI-21LF
8735AM-21LFT	8735BMI-21LFT
8735AMI-21LF	8735BMI-21LF
8735AMI-21LFT	8735BMI-21LFT

**Qualification Test Plan and Result:**

Qual Vehicle: 8735BYI-01LF, 8735BMI-21LF

Test Description	Test Method (Latest specs in effect)	Test Results (SS / Rej)	
		8735BYI-01LF	8735BMI-21LF
ESD: Human Body Model @ 2000V	Each IO Pin Individually to I/O	3/0	3/0
ESD: Charged Device Model @ 1500V	JESD22-C101	3/0	3/0
Latch-up	JESD78	6/0	6/0

# Datasheet Comparisons

## FROM rev A

8735I-01 / INDUSTRIAL temperature range

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, VCC = VCCA = VCCO = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
IEE	Power Supply Current				150	mA
ICCA	Analog Supply Current				15	mA

TABLE 4D. LVPECL DC CHARACTERISTICS, VCC = VCCA = VCCO = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VOH	Output High Voltage; NOTE 1		V <sub>CCO</sub> - 1.4		V <sub>CCO</sub> - 0.9	V
VOL	Output Low Voltage; NOTE 1		V <sub>CCO</sub> - 2.0		V <sub>CCO</sub> - 1.7	V
VSWING	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

Table 6. AC Characteristics, VCC = VCCO = 3.3V ± 5%, VEE = 0V, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f <sub>OUT</sub>	Output Frequency				700	MHz
t <sub>PD</sub>	Propagation Delay; NOTE 1	PLL_SEL = 0V, f ≤ 700MHz	2.8		4.9	ns
t(∅)	Static Phase Offset; NOTE 2, 5	PLL_SEL = 3.3V	-100	50	200	ps
t <sub>sk(o)</sub>	Output Skew; NOTE 3, 5				55	ps
t <sub>jit(cc)</sub>	Cycle-to-Cycle Jitter; NOTE 5, 6				40	ps
t <sub>jit(q)</sub>	Phase Jitter; NOTE 4, 5, 6				±65	ps
t <sub>LOCK</sub>	PLL Lock Time				1	ms
t <sub>R</sub>	Output Rise Time	20% to 80% @ 50MHz	300		700	ps
t <sub>F</sub>	Output Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		47		53	%

## FROM rev A

8735-01 / COMMERCIAL temperature range

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, VCC = VCCA = VCCO = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
IEE	Power Supply Current				150	mA
ICCA	Analog Supply Current				15	mA

TABLE 4D. LVPECL DC CHARACTERISTICS, VCC = VCCA = VCCO = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VOH	Output High Voltage; NOTE 1		V <sub>CCO</sub> - 1.4		V <sub>CCO</sub> - 0.9	V
VOL	Output Low Voltage; NOTE 1		V <sub>CCO</sub> - 2.0		V <sub>CCO</sub> - 1.7	V
VSWING	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

TABLE 6. AC CHARACTERISTICS, VCC = VCCA = VCCO = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f <sub>OUT</sub>	Output Frequency				700	MHz
t <sub>PD</sub>	Propagation Delay; NOTE 1	PLL_SEL = 0V, f ≤ 700MHz	3.4		4.2	ns
t(∅)	Static Phase Offset; NOTE 2, 5	PLL_SEL = 3.3V	-50	50	150	ps
t <sub>sk(o)</sub>	Output Skew; NOTE 3, 5				25	ps
t <sub>jit(cc)</sub>	Cycle-to-Cycle Jitter; NOTE 5, 6				25	ps
t <sub>jit(q)</sub>	Phase Jitter; NOTE 4, 5, 6				±50	ps
t <sub>LOCK</sub>	PLL Lock Time				1	ms
t <sub>R</sub>	Output Rise Time	20% to 80% @ 50MHz	300		700	ps
t <sub>F</sub>	Output Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		47		53	%

## TO rev B

8735BI-01 / INDUSTRIAL Temperature Range

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, VCC = VCCA = VCCO = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
IEE	Power Supply Current				155	mA
ICCA	Analog Supply Current				17	mA

TABLE 4D. LVPECL DC CHARACTERISTICS, VCC = VCCA = VCCO = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VOH	Output High Voltage; NOTE 1		V <sub>CCO</sub> - 1.4		V <sub>CCO</sub> - 0.9	V
VOL	Output Low Voltage; NOTE 1		V <sub>CCO</sub> - 2.1		V <sub>CCO</sub> - 1.7	V
VSWING	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

Table 6. AC Characteristics, VCC = VCCO = 3.3V ± 5%, VEE = 0V, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f <sub>OUT</sub>	Output Frequency				700	MHz
t <sub>PD</sub>	Propagation Delay; NOTE 1	PLL_SEL = 0V, f <sub>OUT</sub> ≤ 700MHz	2.8		4.9	ns
t(∅)	Static Phase Offset; NOTE 2, 4	PLL_SEL = 3.3V	-100		200	ps
t <sub>sk(o)</sub>	Output Skew; NOTE 3, 4				55	ps
t <sub>jit(cc)</sub>	Cycle-to-Cycle Jitter; NOTE 4, 5				50	ps
t <sub>LOCK</sub>	PLL Lock Time				1	ms
t <sub>R</sub> / t <sub>F</sub>	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle	f <sub>OUT</sub> ≤ 250MHz	47		53	%

## TO rev B

8735BI-01 / INDUSTRIAL Temperature Range

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, VCC = VCCA = VCCO = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
IEE	Power Supply Current				155	mA
ICCA	Analog Supply Current				17	mA

TABLE 4D. LVPECL DC CHARACTERISTICS, VCC = VCCA = VCCO = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VOH	Output High Voltage; NOTE 1		V <sub>CCO</sub> - 1.4		V <sub>CCO</sub> - 0.9	V
VOL	Output Low Voltage; NOTE 1		V <sub>CCO</sub> - 2.1		V <sub>CCO</sub> - 1.7	V
VSWING	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

Table 6. AC Characteristics, VCC = VCCO = 3.3V ± 5%, VEE = 0V, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f <sub>OUT</sub>	Output Frequency				700	MHz
t <sub>PD</sub>	Propagation Delay; NOTE 1	PLL_SEL = 0V, f <sub>OUT</sub> ≤ 700MHz	2.8		4.9	ns
t(∅)	Static Phase Offset; NOTE 2, 4	PLL_SEL = 3.3V	-100		200	ps
t <sub>sk(o)</sub>	Output Skew; NOTE 3, 4				55	ps
t <sub>jit(cc)</sub>	Cycle-to-Cycle Jitter; NOTE 4, 5				50	ps
t <sub>LOCK</sub>	PLL Lock Time				1	ms
t <sub>R</sub> / t <sub>F</sub>	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle	f <sub>OUT</sub> ≤ 250MHz	47		53	%

# Datasheet Comparisons

## FROM rev A

### 87351-21 / INDUSTRIAL temperature range

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, VCC = VCCA = VCCO = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
IEE	Power Supply Current				150	mA
ICCA	Analog Supply Current				15	mA

TABLE 4D. LVPECL DC CHARACTERISTICS, VCC = VCCA = VCCO = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V <sub>OH</sub>	Output High Voltage; NOTE 1		V <sub>CCO</sub> - 1.4		V <sub>CCO</sub> - 0.9	V
V <sub>OL</sub>	Output Low Voltage; NOTE 1		V <sub>CCO</sub> - 2.0		V <sub>CCO</sub> - 1.7	V
V <sub>SWING</sub>	Peak-to-Peak Output		0.6		1.0	V

Table 6. AC Characteristics, VCC = VCCO = 3.3V ± 5%, VEE = 0V, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f <sub>MAX</sub>	Output Frequency				700	MHz
t <sub>PD</sub>	Propagation Delay; NOTE 1	PLL_SEL = 0V, f □ 700MHz	2.8		4.9	ns
tsk(o)	Output Skew; NOTE 2, 3	PLL_SEL = 0V			35	ps
tsk(∅)	Static Phase Offset; NOTE 3, 4	PLL_SEL = 3.3V	100	50	200	ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 3, 5				40	ps
tjit(□)	Phase Jitter; NOTE 3, 5, 6				±65	ps
tL	PLL Lock Time				1	ms
tR / tF	Output Rise/Fall Time; NOTE 7	20% to 80% @ 50MHz	200		700	ps
odc	Output Duty Cycle		47		53	%

## FROM rev A

### 87351-21 / COMMERCIAL temperature range

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, VCC = VCCA = VCCO = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
IEE	Power Supply Current				150	mA
ICCA	Analog Supply Current				15	mA

TABLE 4D. LVPECL DC CHARACTERISTICS, VCC = VCCA = VCCO = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V <sub>OH</sub>	Output High Voltage; NOTE 1		V <sub>CCO</sub> - 1.4		V <sub>CCO</sub> - 0.9	V
V <sub>OL</sub>	Output Low Voltage; NOTE 1		V <sub>CCO</sub> - 2.0		V <sub>CCO</sub> - 1.7	V
V <sub>SWING</sub>	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

TABLE 6. AC CHARACTERISTICS, VCC = VCCA = VCCO = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f <sub>MAX</sub>	Output Frequency				700	MHz
t <sub>PD</sub>	Propagation Delay; NOTE 1	PLL_SEL = 0V, f □ 700MHz	3.0		4.2	ns
tsk(o)	Output Skew; NOTE 2, 3	PLL_SEL = 0V			20	ps
tsk(∅)	Static Phase Offset; NOTE 3, 4	PLL_SEL = 3.3V	-50	50	150	ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 3, 5				25	ps
tjit(□)	Phase Jitter; NOTE 3, 5, 6				±50	ps
tL	PLL Lock Time				1	ms
tR / tF	Output Rise/Fall Time; NOTE 7	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		47		53	%

## TO rev B

### 8735BI-21 / INDUSTRIAL Temperature Range

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, VCC = VCCA = VCCO = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
IEE	Power Supply Current				155	mA
ICCA	Analog Supply Current				17	mA

TABLE 4D. LVPECL DC CHARACTERISTICS, VCC = VCCA = VCCO = 3.3V±5%, TA = -40°C TO 85°C

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V <sub>OH</sub>	Output High Voltage; NOTE 1		V <sub>CCO</sub> - 1.4		V <sub>CCO</sub> - 0.9	V
V <sub>OL</sub>	Output Low Voltage; NOTE 1		V <sub>CCO</sub> - 2.1		V <sub>CCO</sub> - 1.7	V
V <sub>SWING</sub>	Peak-to-Peak Output		0.6		1.0	V

Table 6. AC Characteristics, VCC = VCCO = 3.3V ± 5%, VEE = 0V, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f <sub>OUT</sub>	Output Frequency				700	MHz
t <sub>PD</sub>	Propagation Delay2	PLL_SEL = 0V, f □ 700MHz	2.8		4.9	ns
tsk(o)	Output Skew3, 4	PLL_SEL = 0V			35	ps
t(∅)	Static Phase Offset4, 5	PLL_SEL = 3.3V	-100		200	ps
tjit(cc)	Cycle-to-Cycle Jitter4, 6				50	ps
tjit(□)	Phase Jitter4, 6, 7				±80	ps
tL	PLL Lock Time				1	ms
tR / tF	Output Rise/Fall Time	20% to 80% @ 50MHz	200		700	ps
odc	Output Duty Cycle	f <sub>OUT</sub> □ 250MHz	47		53	%

## TO rev B

### 8735BI-21 / INDUSTRIAL Temperature Range

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, VCC = VCCA = VCCO = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
IEE	Power Supply Current				155	mA
ICCA	Analog Supply Current				17	mA

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Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
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V <sub>OL</sub>	Output Low Voltage; NOTE 1		V <sub>CCO</sub> - 2.1		V <sub>CCO</sub> - 1.7	V
V <sub>SWING</sub>	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

Table 6. AC Characteristics, VCC = VCCO = 3.3V ± 5%, VEE = 0V, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f <sub>OUT</sub>	Output Frequency				700	MHz
t <sub>PD</sub>	Propagation Delay2	PLL_SEL = 0V, f □ 700MHz	2.8		4.9	ns
tsk(o)	Output Skew3, 4	PLL_SEL = 0V			35	ps
t(∅)	Static Phase Offset4, 5	PLL_SEL = 3.3V	-100		200	ps
tjit(cc)	Cycle-to-Cycle Jitter4, 6				50	ps
tjit(□)	Phase Jitter4, 6, 7				±80	ps
tL	PLL Lock Time				1	ms
tR / tF	Output Rise/Fall Time	20% to 80% @ 50MHz	200		700	ps
odc	Output Duty Cycle	f <sub>OUT</sub> □ 250MHz	47		53	%

NOTE 2: Measured from the differential input crosspoint to the differential output crosspoint.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crosspoint.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 5: Defined as the time difference between the input reference clock and the averaged feedback input signal across all conditions, when the PLL is locked and the input reference frequency is stable.

NOTE 6: Characterized at VCO frequency of 622MHz.

NOTE 7: Phase jitter is dependent on the input source used.