



Integrated Device Technology, Inc.  
2975 Stender Way, Santa Clara, CA - 95054

## PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: L0007-04      DATE: 7/31/2000  
Product Affected: 74LVC16244, 74LVC16245  
74LVCH162244  
Manufacturing Location Affected: IDT Salinas Fab  
Date Effective: 10/31/2000

**MEANS OF DISTINGUISHING CHANGED DEVICES:**

- Product Mark
- Back Mark
- Date Code      Prefix from "X" to "XG"
- Other

Contact: Bimla Paul  
Title: Product Assurance Manager  
Phone #: 408-654-6419  
Fax #: 408-492-8362  
E-mail: bima.paul@idt.com

Attachment:  Yes       No

Samples:

**DESCRIPTION AND PURPOSE OF CHANGE:**

- Die Technology
- Wafer Fabrication Process      This change has been implemented to add TSMC (Taiwan) as an alternate fab to IDT fab (Salinas).
- Assembly Process
- Equipment
- Material
- Testing
- Manufacturing Site
- Data Sheet
- Other

**RELIABILITY/QUALIFICATION SUMMARY:**

Available upon request.

**CUSTOMER ACKNOWLEDGMENT OF RECEIPT:**

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.

IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: \_\_\_\_\_       *Approval for shipments prior to effective date.*  
Name/Date: \_\_\_\_\_      E-Mail Address: \_\_\_\_\_  
Title: \_\_\_\_\_      Phone# /Fax# : \_\_\_\_\_

**CUSTOMER COMMENTS:** \_\_\_\_\_

**IDT ACKNOWLEDGMENT OF RECEIPT:**

RECD. BY: \_\_\_\_\_      DATE: \_\_\_\_\_



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#### PCN Summary

**PCN Type:** Fab Site Change

**Commodity** Logic

**Forecast or Execute** Execute

**Planned or Unplanned** Planned

**Data Sheet Change** No Change

#### Detail of Change

This process change has been implemented to add TSMC Fab 9, 0.5µm process for 74LVC16244, 74LVC16245, 74LVCH162244.

#### Process / Design Changes

	<u>Current Die Rev - X</u>	<u>New Die Rev - XG</u>
Wafer Fab Technology	CEMOS 8.0	0.5µm
Poly Gate	0.5µm	0.5µm
Minimum Gate Oxide	140Å	115Å
Wafer Size	6"	8"
Fab Facility	Fab 2 (Salinas)	TSMC Fab 9

#### Conversion schedule (Estimated)

	<b>Sample Availability</b>	<b>Production Shipments</b>
74LVC16244	September, 2000	October 31, 2000
74LVC16245	Available	October 31, 2000
74LVCH162244	September, 2000	October 31, 2000



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## PRODUCT/PROCESS CHANGE NOTICE (PCN)

### ATTACHMENT - PCN #: L0007-04

Qualification Plan      QLG-00-07

Test Vehicle:      74LVC16245

Expected Completion Date:

October 31, 2000

Test	Lot SS/ Acc #	Lot # 1	Lot # 2	Lot # 3
<b>Bond Pull</b> EIA/JESD22-B116	5/0			
<b>Die Shear</b> Mil-Std-883, Method 2019	3/0			
<b>Ball Shear</b> EIA/JESD22-B116	5/0			
<b>Operating Life Test (Dynamic)</b> Mil-Std-883, Method 1005	77/0			
<b>85/85(THB) or HAST</b> EIA/JESD22-A110	45/0			
<b>Pressure Pot</b> EIA/JESD22-A102	45/0			
<b>Thermal Shock</b> Mil-Std-883, Method 1011	45/0			
<b>Temperature Cycling</b> Mil-Std-883, Method 1010	45/0			
<b>ESD: HBM</b> Mil-Std-883, Method 3015	3/0			
<b>ESD: CDM</b>	3/0			
<b>Latch-Up Immunity</b> EIA/JESD78	10/0			
<b>Electrical Characterization</b> Per Applicable Datasheet	10/0			