



Integrated Device Technology, Inc.  
2975 Stender Way, Santa Clara, CA - 95054

## PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: **I-0210-06**  
Product Affected:  
IDT79RC32T351, IDT79RC32T355  
  
Date Effective: February 12, 2003

DATE: November 12, 2002

**MEANS OF DISTINGUISHING CHANGED DEVICES:**

- Product Mark
- Back Mark
- Date Code      Prefix change from ZC to ZD
- Other

Contact: Bimla Paul  
Title: Product Assurance Manager  
Phone #: 408-654-6419  
Fax #: 408-492-8362  
E-mail: bima.paul@idt.com

Attachment:  Yes       No

Samples: Available upon request

**DESCRIPTION AND PURPOSE OF CHANGE:**

- Die Technology
- Wafer Fabrication Process
- Assembly Process
- Equipment      Die Revision change from "ZC"(CMOS 11.5) to "ZD"(CMOS 11.5) to enhance the device performance.
- Material
- Testing
- Manufacturing Site      This change affects all speed grades and package options. There is no change in die technology/process.
- Data Sheet
- Other

**RELIABILITY/QUALIFICATION SUMMARY:**

Qualification data is attached.

**CUSTOMER ACKNOWLEDGMENT OF RECEIPT:**

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.

**IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.**

Customer: \_\_\_\_\_  **Approval for shipments prior to effective date.**  
Name/Date: \_\_\_\_\_ E-Mail Address: \_\_\_\_\_  
Title: \_\_\_\_\_ Phone# /Fax# : \_\_\_\_\_

**CUSTOMER COMMENTS:** \_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

**IDT ACKNOWLEDGMENT OF RECEIPT:**

RECD. BY: \_\_\_\_\_ DATE: \_\_\_\_\_



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### ATTACHMENT - PCN #: I-0210-06

**PCN Type:** Die Revision

**Data Sheet Change** N/A

**Detail of Change** The new die revision will address the known errata items as follows:

1. To eliminate DMA controller malfunctions due to receipt by the Ethernet block of an odd number of 4-bit nibbles in a packet. (Reference Item #17 of RC32355 errata, dated October 8, 2002.)
2. To eliminate DMA channel hang if there is a "late collision" which lands in a four byte window near the end of a packet. (Reference Item #18 of RC32355 errata, dated October 8, 2002.)
3. To eliminate I2C Controller from re-issuing last command into the I2CMCMD register. (Reference Item #19 of RC32355 errata, dated October 8, 2002.)

This change affects all speed grades and package options. There is no change in die technology/ process.

#### Conversion schedule (Estimated)

Base Device	Sample Availability	Production Shipments
IDT79RC32T355	Available	February 12, 2003
IDT79RC32T351	Available	February 12, 2003



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## PRODUCT/PROCESS CHANGE NOTICE (PCN)

### ATTACHMENT - PCN #: I-0210-06

Qualification Plan: QI-02-05

Test Vehicle: 79RC32T355

	Required sample/# fails	Test Data
Operating Life Test (Dynamic) Mil-Std -883 Method 1005 (1000 Hrs @125°C, Vcc = 3.3V)	77/0	77/0
Temperature cycling (Mil-Std-883, Method 1010) (-65°C to +150°C, 500cyc)	45/0	45/0
ESD: Human Body Model Mil-Std 883, Method 3015	3/0	3/0
ESD: Charge Device Model JESD22-C101	3/0	3/0
Latch-up, JESD 78	10/0	10/0

#### Characterization Data:

Characterization Data is available upon request.

Characterization will verify that there is no change to existing data sheet parameters.