# Product Change Notice (PCN)

**Subject:** RZ/V2N Product Mask Version Change
**Publication Date:** 6/25/2025
**Effective Date:** 12/22/2025

## Revision Description:
Initial release

## Description of Change:
  The mask revision will be implemented for the DDR Memory Controller issue informed by the technical update (TN-RZ*-A0144A/E). The revised products will be available from Dec 2025.

| Before Mask Revision | After Mask Revision |
|---|---|
| In rare cases, abnormal read data may be returned when MIPI DSI among the bus masters connected Port 1 access DDR memory. | Read to DDR memory from all bus masters work normally. |

Production of products with the previous mask version is planned to be discontinued. We kindly request that the customer transition to the revised products. Please review the changes and, based on your judgement, make the necessary software modifications and evaluations.

## Affected Product List:

| Product Series | Booking Part Number | | Mask Version | |
|---|---|---|---|---|
| | Before Mask Revision | After Mask Revision | Before | After |
| RZ/V2N | R9A09G056N41GBG#AC0 | R9A09G056N41GBG#AC1 | V1 | V2 |
| | R9A09G056N41GBG#BC0 | R9A09G056N41GBG#BC1 | V1 | V2 |
| | R9A09G056N42GBG#AC0 | R9A09G056N42GBG#AC1 | V1 | V2 |
| | R9A09G056N42GBG#BC0 | R9A09G056N42GBG#BC1 | V1 | V2 |
| | R9A09G056N43GBG#AC0 | R9A09G056N43GBG#AC1 | V1 | V2 |
| | R9A09G056N43GBG#BC0 | R9A09G056N43GBG#BC1 | V1 | V2 |
| | R9A09G056N44GBG#AC0 | R9A09G056N44GBG#AC1 | V1 | V2 |
| | R9A09G056N44GBG#BC0 | R9A09G056N44GBG#BC1 | V1 | V2 |
| | R9A09G056N45GBG#AC0 | R9A09G056N45GBG#AC1 | V1 | V2 |
| | R9A09G056N45GBG#BC0 | R9A09G056N45GBG#BC1 | V1 | V2 |
| | R9A09G056N46GBG#AC0 | R9A09G056N46GBG#AC1 | V1 | V2 |
| | R9A09G056N46GBG#BC0 | R9A09G056N46GBG#BC1 | V1 | V2 |
| | R9A09G056N47GBG#AC0 | R9A09G056N47GBG#AC1 | V1 | V2 |
| | R9A09G056N47GBG#BC0 | R9A09G056N47GBG#BC1 | V1 | V2 |
| | R9A09G056N48GBG#AC0 | R9A09G056N48GBG#AC1 | V1 | V2 |
| | R9A09G056N48GBG#BC0 | R9A09G056N48GBG#BC1 | V1 | V2 |

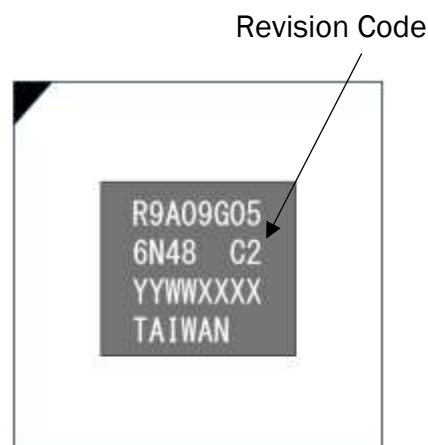## Reason for Change:
Fixing the DDR Memory Controller issue.

## Impact on Fit, Form, Function, Quality & Reliability:
Fit, Form, Quality & Reliability: None
Function: The functions described in the "Description of Change" section are modified.

**Product Identification:**

Revised products can be identified by the revision code 'C2' marked on the package or by reading the value from the LSI Device ID register. Additionally, for the revised products, the last digit of the booking part number will be changed from 0 to 1.

Revision Code



LSI Device ID register (DEV_ID[31:28])

| Before Mask Revision | After Mask Revision |
|---|---|
| 0x0 | 0x1 |

**Qualification Status:** N/A
**Sample Availability Date:** 9/8/2025
**Device Material Declaration:** N/A

Note:

1. Acknowledgement must be received by Renesas within 30 days or Renesas will consider the change as approved.

2. If timely acknowledgement is provided by Customer, then Customer shall have 90 days from the date of receipt of this PCN to make any objections to this PCN. If Customer fails to make objections to this PCN within 90 days of the receipt of the PCN then Renesas will consider the PCN changes as approved.

3. If customer cannot accept the PCN then customer must provide Renesas with a last time buy demand and purchase order.

For additional information regarding this notice, please contact your Renesas sales representative.