IDT®
Using the Tsi310™ to Optimize I/O Adapter Card Designs

80B6000_WP002_04

September 19, 2009

6024 Silver Creek Valley Road San Jose, California 95138
Telephone: (408) 284-8200 • FAX: (408) 284-3572
Printed in U.S.A.

1. Using the Tsi310 to Optimize I/O Adapter Card Designs

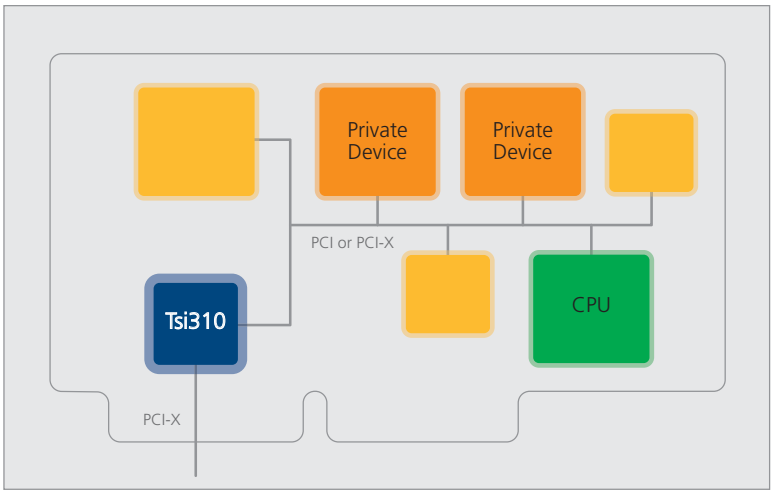
1.1 Optional Base Address Register

Tsi310's Optional Base Address Register (offset 0x10) allows an I/O adapter to allocate memory for private devices located on Tsi310's secondary bus (Figure 1). As a result, this feature allows the I/O adapter's microprocessor to initialize and manage these devices without interference from the host computer system.

However, the nature of the private device feature precludes the assignment of system memory address space to the private devices. The system initialization algorithms for PCI and PCI-X computer systems allocate memory regions to devices discovered during the initialization process; private devices are hidden from the host initialization agent, which is typically the BIOS.

Tsi310's Optional Base Address Register can be used to acquire system memory address space for private devices attached to the bridge's secondary bus. The PCI specification allows for a bridge to use a base address register (BAR) to claim a region in system memory for its own use. When enabled using a strapping pin, the optional BAR creates a false bridge memory requirement of 1 Mbyte that is allocated and mapped during system initialization. The Tsi310 does not need this memory region for its own use; it simply passes accesses to this region to the devices on its secondary bus.

Figure 1: Tsi310's Optional Base Address Register Allows an I/O Adapter to Allocate Memory for Private Devices Located on Tsi310's Secondary Bus



1.2 Access to Tsi310's Configuration Registers from the Secondary PCI/PCI-X Bus

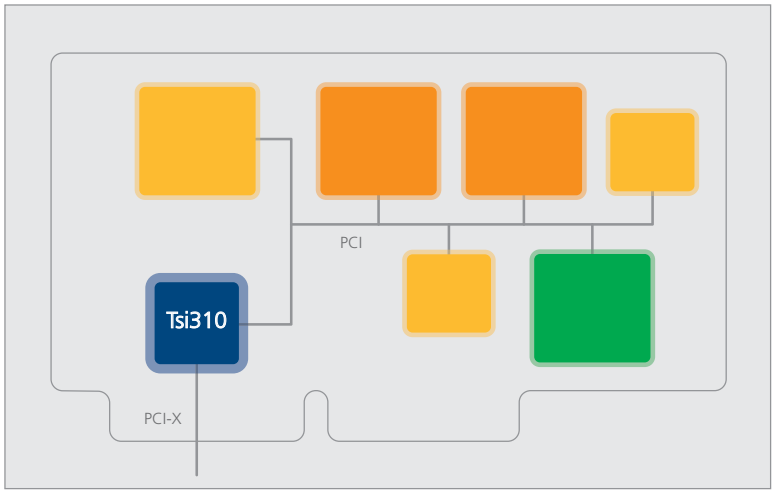
A PCI-X transparent bridge is not required to provide access to its Configuration registers from devices on its secondary bus. The Tsi310, however, supports this capability to enhance the design of I/O adapters that require a microprocessor on the secondary bus. Some examples of how this feature may be used by the adapter card's microprocessor are:

- Tsi310's Optional BAR register can be queried to discover the address range to be used for the private devices included on the I/O adapter.
- Tsi310's Opaque memory region can be moved and resized to suit the specific needs of the I/O adapter.
- Tsi310's Data Buffering Control Registers can be tuned for the specific application of the I/O adapter.
- The arbitration priorities of the devices on the secondary bus can be modified.

1.3 Short-Term Caching of PCI Read Data

The Tsi310 has an optional PCI read-data caching feature, called short-term caching, that can improve performance when it connects a PCI subsystem to a PCI-X or PCI system (Figure 2). When short-term caching is used, data that have been fetched, or are in the process of being fetched, are not immediately discarded when the transaction is stopped by the requesting device. Any data received due to outstanding prefetch requests made by the Tsi310 are buffered to support data consumption by the PCI device. If the stopped PCI read request is not resumed within approximately 64 PCI bus cycles, the Tsi310 discards the cached data and any incoming prefetch data for the PCI read request.

Figure 2: Optional PCI Read-Data Caching Feature Improves Performance When It Connects a PCI Subsystem to a PCI-X or PCI System



1.3.1 Short-term Caching and Split Reads

One of the benefits of the PCI-X architecture over the PCI architecture is its support for split-read transactions. In a split-read transaction, the requesting device first identifies itself, determines the address of the required data and how much data it needs, and then waits the data.

In contrast with a PCI read, the requesting device specifies the address of the desired data and indicates only a small portion of the data that it required. If the data is not immediately available, the request is repeated until the target is able to deliver. If the target fetches more data than the requesting device consumes, the data must be discarded. Also, if the target runs out of data because of a slow response to its prefetch requests, the transaction with the requester is stopped and the incoming prefetch data intended for that transaction is discarded to assure memory coherency.

1.3.2 Notes

- When short-term caching is used the Tsi310 is non-compliant with the PCI specification.
- A system with both PCI and PCI-X buses does not fully benefit from the split-read transaction. When a PCI bus is subordinate to a PCI-X bus — for example, when a bridge has a primary PCI-X bus and a secondary PCI — PCI read performance may be worse than in a PCI-only system. This assumes, however, that the positive effects of increased bus frequencies available with PCI-X are not considered.

CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
email: ssdhelp@idt.com
phone: 408-284-8208
document: 80B6000_WP002_04