To our customers,

## Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

# Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   “Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

Information


# μPD98405 Q&A

## (NEASCOT-S20™)

## 155M ATM INTEGRATED SAR CONTROLLER

Document No. S14628EJ1V0IFJ1 (1st edition)
Date Published October 2000 N CP(K)

**[MEMO]**

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

**NEASCOT-S20 and EEPROM are trademarks of NEC Corporation.**

- **The information in this document is current as of February, 2000. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**
- No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this document.
- NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC semiconductor products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.
- NEC semiconductor products are classified into the following three quality grades:
  "Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.

  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

  The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.

  (Note)

  (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.

  (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).

M8E 00.4

# INTRODUCTION

**Readers**

This manual is intended for engineers who wish to understand the functions of the μPD98405 and design application systems using it.

**Purpose**

The purpose of this manual is to answer questions asked by users of this product. It is prepared for the purpose of reference in cases where there are points that are unclear to users.

**How to Read This Manual**

Refer to the table of contents for the item that is unclear.
When reading this information, you must have a general knowledge of logic circuits and microcomputers.
When using this manual, be sure to refer to the latest user's manual and data sheet.

**Related Documents**

- Data sheet : S12689E
- User's manual : S12250E

**Conventions**

| | | |
|---|---|---|
| Data significance | : | Left: high-order digit, right: low-order digit |
| Active low | : | xxx_B (_B following pin or signal name) |
| Memory map address | : | Top: high-order, bottom: low-order |
| Numeric notation | : | Binary .....XXXX or XXXXB |
| | | Decimal .....XXXX |
| | | Hexadecimal.....XXXXh |

**[MEMO]**

## CONTENTS

# CHAPTER 1 PINS

**Q.1.1**

How is the operation of the PHRST_B pin performed?

**A.1.1**

The PHRST_B pin goes low at the same time as the RST_B pin goes low, and holds low level for a min. 17 clock (SCLK input) period after the RST_B pin has gone high.

**Q.1.2**

Is the PHRST_B pin valid during internal PHY mode?

**A.1.2**

Yes. The PHRST_B pin outputs low level when low level is input to the RST_B pin or when software reset is applied.

**Q.1.3**

Is it necessary to supply high-quality power to such power supply pins as $AV_{DD3}$, $HV_{DD3}$, or $RV_{DD3}$ when not using the internal PHY?

**A.1.3**

No. Supply +3.3 V power in the same manner as supplyed to the digital block ($V_{DD3}$).

**Q.2.1**

How the cache line size of the PCI configuration register should be set?

**A.2.1**

The μPD98405 supports 4, 8, or 16 words only as the cache line size. Therefore, setting 4, 8, or 16 is valid for the cache line size. If any other values are set, the μPD98405 does not consider the cache boundary when performing transfer.

**Q.2.2**

Which PCI command is issued by the μPD98405 during master?

**A.2.2**

Refer to μPD98405 user's manual section **4.2.4 Master transactions**. Regarding the read command, however, which command is issued differs as follows depending on the settings for the cache line size.

When cache line size is set to 4, 8, or 16: Commands described in μPD98405 user's manual section **4.2.4 (1) (a) Read transactions** are issued.

When cache line size is set to a value other than 4, 8, or 16: the μPD98405 always issues memory read command. Exercise caution when using on a system that performs processing identifying the type of read command.

**Q.2.3**

How should the latency timer of the PCI configuration register be set?

**A.2.3**

Setting of the latency timer becomes valid when the low-order 3 bits of the set value are masked. That is, setting of the latency timer should be 0, 8, 16, to 248.

**Q.2.4**

What is the function of the retry timer of the PCI configuration register?

**A.2.4**

The μPD98405 counts retry timeout, disconnect timeout, and latency timeout as the retry timer count. If all of these transfer abort counts exceed the retry timer set value, the FERR bit of the GSR register is set and the operation is stopped.

**Q.2.5**

What results when the μPD98405 receives an invalid command during target?

**A.2.5**

The μPD98405 does not respond to the transfer (does not assert DEVSEL_B active).
Invalid commands are all those not listed below:

Memory Read
Memory Read Line
Memory Read Multiple
Memory Write
Memory Write And Invalidate
I/O Read
I/O Write
Configuration Read
Configuration Write

**Q.2.6**

Are the registers of the μPD98405 mapped to I/O space or memory space?

**A.2.6**

Both I/O space and memory space can be used. They can also be used simultaneously.

**Q.2.7**

Does the μPD98405 support master operation of arbitration parking such as AD line driving if selected by arbiter when there is no master to request transfer on the PCI bus?

**A.2.7**

Yes.

**Q.2.8**

When using a 32-bit PCI, how should the ACK64_B and REQ64_B pins be processed?

**A.2.8**

Pull up the ACK64_B and REQ64_B pins externally.

**Q.2.9**

Is it possible to use big endian in PCI mode?

**A.2.9**

No. Only little endian can be used in PCI mode. Big or little endian can be selected in general-purpose bus mode.

**Q.2.10**

What is the value of Revision ID of the PCI configuration register?

**A.2.10**

The Revision ID is 01h, which is common to all the versions. The values of the VER register, a μPD98405 internal register, differ depending on the version. The version of the device can be recognized using the VER register.

**Q.2.11**

Why is not possible to write 0 to status bits 31 through 27 and 24 of the PCI configuration register?

**A.2.11**

Write operation to the Status register conforms to the PCI standard. When 0 is written to the bit, the bit holds the value, and when 1 is written to the bit, the bit is cleared to 0.

**Q.2.12**

What are the settings related to the burst size when the μPD98405 performs transfer as a master?

**A.2.12**

Settings of the AD bit of the GMR register, cache line size and latency timer of the configuration register are related.

**Q.2.13**

How long does it take to check EEPROM™ connection and automatic loading?

**A.2.13**

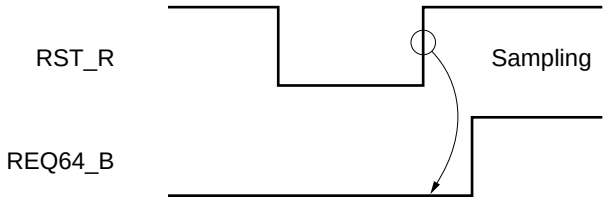
Connection check takes about 600 clocks (CLK input) and automatic loading takes about 2400 clocks (CLK input).

**Q.2.14**

How is the 64-bit PCI recognized?

**A.2.14**

The μPD98405 samples the REQ64_B signal at the end of reset (rise of RST_B). When REQ64_B is low, the μPD98405 recognizes it as the 64-bit PCI, and performs 64-bit PCI transfer.




**Q.2.15**

How is setting performed when using the 64-bit PCI?

**A.2.15**

As described in A.2.14, 64-bit transfer is enabled when 64-bit PCI is recognized and E64 bit of GMR register is set to 1. To use 64-bit addressing, set the PBAH register to any value other than 0.

**Q.2.16**

What is the count of Fast back-to-back?

**A.2.16**

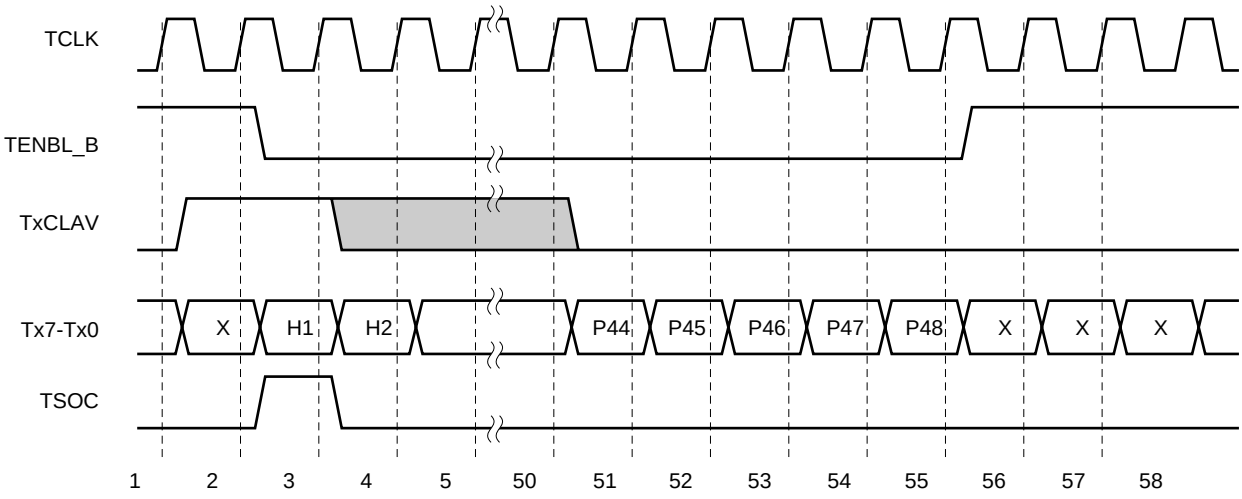
The maximum count of Fast back-to-back is set in the BBL field of the GMR register. When BBL is set to 1, the maximum count of Fast back-to-back is one, and two transfers are executed in Fast back-to-back. The maximum number of BBL is seven. When BBL is set to 0, transfer is disabled and Fast back-to-back is not executed.

**Q.3.1**

When should the TCLAV signal be deasserted?

**A.3.1**

Deassert it between H2 (second byte of a cell header) and P44 (44th byte of a payload). Do not deassert it at H1.




**Q.3.2**

What is the phase difference between TCLK and RCLK?

**A.3.2**

The phase difference between TCLK and RCLK is not officially specified.

**Q.3.3**

What are the frequencies of TCLK and RCLK and what is their delay from SCLK?

**A.3.3**

TCLK and RCLK output a clock at the same timing as SCLK input. At this time, the delay is as follows:

SCLK → TCLK delay: 15 ns MAX.
SCLK → RCLK delay: 15 ns MAX.

**Q.3.4**

The clocks (TCLK and RCLK) of the UTOPIA output a clock at the same timing as SCLK input. Can any other clocks be used?

**A.3.4**

No.

**Q.3.5**

Can the RCLAV signal be deasserted in the middle of transferring a cell during cell-level handshaking?

**A.3.5**

Yes. The μPD98405 does not load the data of Rx7 through Rx0 while the RCALV signal is deasserted. If the RCLAV signal is deasserted again, it starts loading Rx7 through Rx0 as valid data.

**Q.3.6**

Does the RENBL_B signal perform the same operation in No Drop mode (GMR register DR = 1) as in octet- and cell-level handshake mode?

**A.3.6**

Yes. For details of the operation, refer to **4.3.1 UTOPIA interface** of the ***μ*PD98405 User's Manual**.

**Q.3.7**

What is the status of the Tx7 through Tx0 pins while the TENBL_B signal is inactive (high level)?

**A.3.7**

The Tx7 through Tx0 pins output 0.

**Q.3.8**

An external PHY device is connected to the UTOPIA interface and PHY is controlled by an external interface. At this time, is it necessary to use the PHY control interface of the μPD98405?

**A.3.8**

It is all right if the PHY control interface of the μPD98405 is not used. In this case, the PHINT_B pin must be externally pulled up. The other pins may be opened.

## CHAPTER 4 CONTROL MEMORY

**Q.4.1**

Is the control memory automatically initialized without problems even if the maximum size of the control memory is not mounted?

**A.4.1**

Yes. For details of automatic initialization, refer to **5.2 Setting the Control Memory** in the ***μ*PD98405 User's Manual**.

**Q.4.2**

If only a few VCs are used, is it possible to reduce the capacity of the control memory?

**A.4.2**

The capacity of the control memory can be reduced in accordance with the number of VCs used. For how to determined the capacity, refer to **5.2 Setting the Control Memory** in the ***μ*PD98405 User's Manual**.

**Q.4.3**

What are the conditions of the SRAM to be used as the control memory?

**A.4.3**

An SRAM that satisfies the following conditions can be used:

- +3.3 V or +5 V product
- Operating speed: 15 ns (when SCLK = 25 MHz); operating speed is dependent on SCLK input.
- A total of 32 bits wide; enabling control in 8-bit units is necessary.

**Q.4.4**

How can the host CPU access the control memory?

**A.4.4**

The host CPU can access the control memory via *μ*PD98405. The host CPU can read or write the control memory by issuing an Indirect_Access command.

**Q.4.5**

How long does it take to initialize the control memory after reset?

**A.4.5**

It takes 32K clocks (SCLK input). The time required to automatically initialize the control memory is not dependent on the size of the control memory but is fixed to 32K clocks.

**Q.4.6**

Are the contents of the control memory cleared to 0 when the control memory is automatically initialized after reset?

**A.4.6**

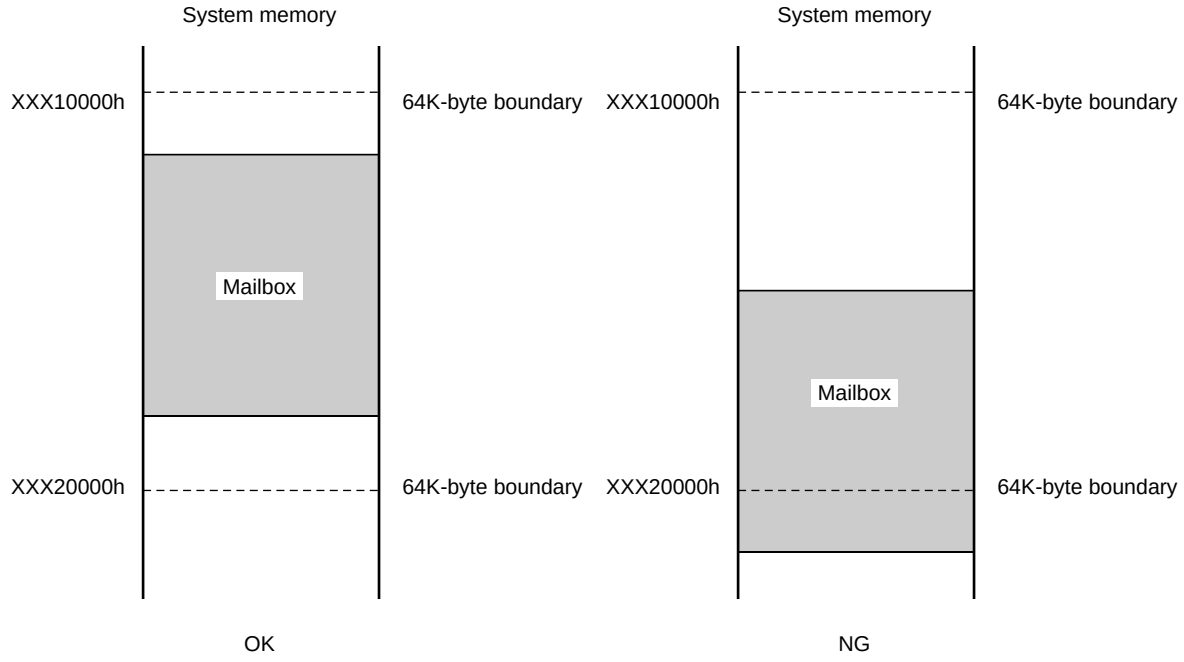
The μPD98405 only writes block numbers when the control memory is automatically initialized. Other areas are not cleared to 0. To initialize the control memory, therefore, execute software reset after the host has cleared all the areas to 0, so that automatic initialization (writing block numbers) is executed.

**Q.5.1**

Can a mailbox be set straddling over a 64K-byte area?

**A.5.1**

No, it cannot. A mailbox must be fit into an area of 64K bytes that is set by the MSH register (the high-order 16 bits of a mailbox start address). If the mailbox is used at the maximum size (about 64K bytes), the MSL register must be cleared to 0.




**Q.5.2**

When does the mailbox become full and how is transmission/reception stopped?

**A.5.2**

The mailbox becomes full (including notification) when the corresponding indication has been correctly written to the mailbox. Transmission/reception is stopped when an attempt is made to write the next indication to the mailbox that is full.

## CHAPTER 6 TRANSMISSION SCHEDULER

**Q.6.1**

What is the relation between setting of the scheduler register (I, M, and P parameters) and the actual transmission rate?

**A.6.1**

The scheduler register (I, M, and P parameters) is set in cell units. The average rate is set by the I/M of valid cell transmission of I cells per M cell. As the peak rate, the valid cell interval is set as the P cell interval. The actual transmission rate set by the scheduler register is dependent on the speed (line speed) of the PHY device connected at the line side. The relation between the line speed and transmission rate can be expressed as follows:

Average rate = I/M x Line speed
Peak rate = Line speed/(P + 1)

Here is an example of setting where the line speed is 155.52 Mbps.

**Example** Line speed: 155.52 Mbps, Average rate: 38.88 Mbps, Peak rate: 51.84 Mbps
I/M = 38.88/155.52 = 1/4
P = (155.52/51.84) – 1 = 2

**Q.6.2**

Is the same cell scheduling operation performed at I/M = 1/10 and I/M = 10/100?

**A.6.2**

Yes.

**Q.6.3**

Is it possible to make the priorities of two or more shapers the same?

**A.6.3**

Yes. The priorities of the shapers can be made the same by setting the same value to the PRIORITY field of the scheduler register of each shaper. If a cell transmission timing conflict between the shapers of the same priority occurs, cells are sequentially transmitted to the shapers by using a round-robin algorithm.

**Q.6.4**

Is it possible to control the band between VCs (for example, to widen the cell transmission interval between VC1 and VC2)?

**A.6.4**

Yes. Forcibly narrow the band by using an unassigned cell generator. If the priority of the unassigned cell generator is set to the highest level, all data cell intervals are extended by the band used for the unassigned cell generator.

Example of transmitting cell:

VC1, VC2, and VC3 use shaper 1.

Setting of shaper 1: I/M = 1/9, P = 0, C = 2

Normal cell transmission

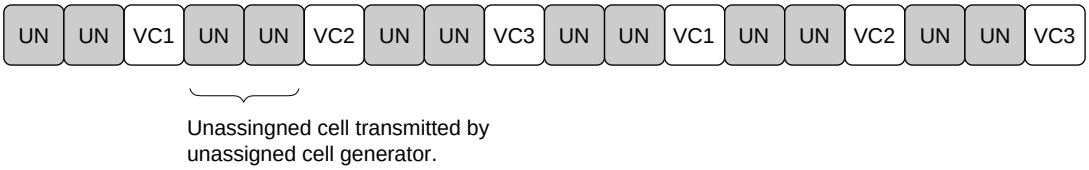
VC1, 2, 3: Data cell

UN: Unassigned cell


Cell transmission when unassigned cell generator is used

Shaper 0 is set to unassigned cell generator.

Setting of shaper 0: I/M = 2/3, P = 0, C = 2




**Q.6.5**

What is the band of each VC linked to a shaper in the aggregate mode?

**A.6.5**

Each active VC that is transmitting a cell equally divides the band of the shaper and uses the divided band. For example, if 3 VCs (VC1, VC2, and VC3) are registered to a shaper in aggregate mode (setting of shaper: I/M = 11/1, P = 0, C = 2), while all the 3 VCs are transmitting a cell, the band of each VC is 1/3 of the shaper setting.

VC1 = 1/3, VC2 = 1/3, VC3 = 1/3

While VC1 and VC2 are transmitting a cell, the band of each VC is as follows:

VC1 = 1/2, VC2 = 1/2, VC3 = 0

**Q.6.6**

How long is one cell time for cell transmission scheduling?

**A.6.6**

The μPD98405 performs cell transmission scheduling by using 36 SCLK input clocks as one unit. Therefore, it determines the next cell to be transmitted every 36 clocks.

**Q.6.7**

What is the relation between cell transmission scheduling and DMA operation?

**A.6.7**

The μPD98405 determines the cell to be transmitted every 36 clocks by using the scheduler. After the cell to be transmitted has been determined, a DMA operation to read cell data is executed. If the transmit FIFO has become full, a DMA operation to read cell data is stopped.

**Q.6.8**

Does the host CPU have to set the A bit of the scheduler register?

**A.6.8**

The A bit of the scheduler register is managed or changed by the μPD98405. It is not necessary for the host CPU to rewrite this bit. The host CPU must set the A bit only when a shaper is used as an unassigned cell generator.

## CHAPTER 7 TRANSMISSION

**Q.7.1**

Is it possible for the transmit FIFO to overflow and for cells to be discarded?

**A.7.1**

No. If the transmit FIFO has become full because the UTOPIA interface cannot transmit cells any more, cell data is not read. If the transmit FIFO has a vacancy, reading data is resumed.

**Q.7.2**

Is the size of the transmit queue of each VC consisting of a transmit packet descriptor limited?

**A.7.2**

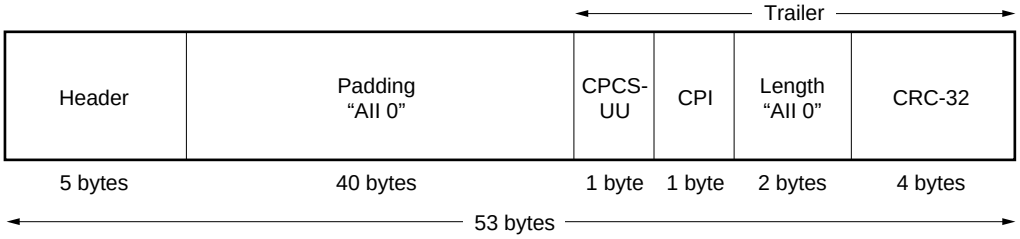
No.

**Q.7.3**

How is transmission performed if it is set by the transmit packet descriptor for AAL5 that SIZE = 0?

**A.7.3**

Transmission is performed normally. Only one last cell of padding + trailer is transmitted. Because the length field of the trailer is 0, this cell is the last cell aborted by the user.

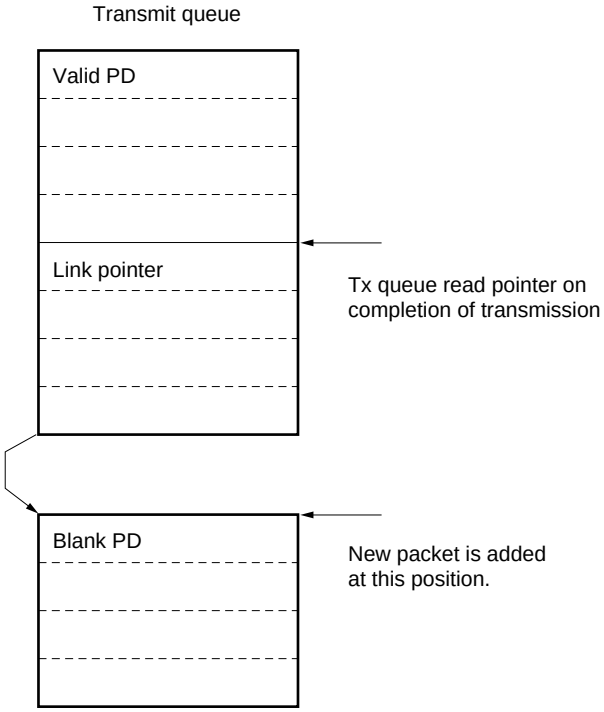


**Q.7.4**

If a transmit queue consists in the sequence of a valid packet descriptor → link pointer → blank packet descriptor, to what does Tx queue read pointer of the transmit VC table point on completion of transmission?

**A.7.4**

Tx queue pointer points to the position of a link pointer. To start transmission by adding a packet in this case, issue an additional Tx_Ready command to the position of the blank packet descriptor.




**Q.7.5**

Can a packet be added during transmission when the transmit VC is active?

**A.7.5**

Yes. Add a new packet at the position of the blank packet descriptor of that transmit queue and issue the Tx_Ready command.

**Q.7.6**

When are the contents of packet descriptor Word0 stored in transmit VC table Word0?

**A.7.6**

After the Tx_Ready command has been issued, the μPD98405 reads the packet descriptor and stores the contents of packet descriptor Word0 in the transmit VC table Word0, and then reads data.

**Q.7.7**

Is the number of VCs linked to a shaper limited?

**A.7.7**

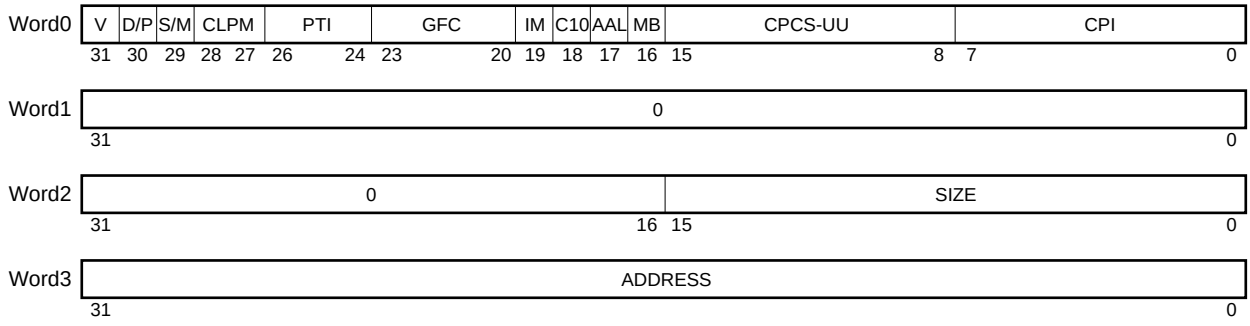
No. It is also possible to link all the VCs used to one shaper.

**Q.7.8**

Is there any problem if the value of the vacant field (Word1, Word2 bits 31 through 16) of the transmit packet descriptor is not 0? Are the values on the system memory rewritten?

**A.7.8**

The vacant field (Word1, Word2 bits 31 through 16) may be a value other than 0. The μPD98405 reads four words of packet descriptors and internally ignores the information in the vacant field. The values on the system memory are not rewritten.

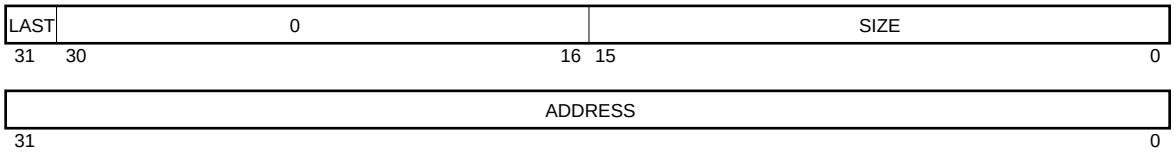


**Q.7.9**

Is there any problem if the value of the vacant field (Word0, bits 30 through 16) of the transmit buffer descriptor is not 0? Are the values on the system memory rewritten?

**A.7.9**

The vacant field (Word0, bits 30 through 16) may be a value other than 0. The μPD98405 reads two words of buffer descriptors and internally ignores the information in the vacant field. The values on the system memory are not rewritten.




**Q.7.10**

What does the Packet queue pointer field for transmission indication indicate?

**A.7.10**

The Packet queue pointer field indicates the address of the packet descriptor of the packet next to the one at which transmission has been completed. Note that it does not indicate the packet descriptor address of the packet at which transmission has been completed. Only the low-order 15 bits of its address are reported.

**Q.7.11**

How can the OAM F5 cell be transmitted?

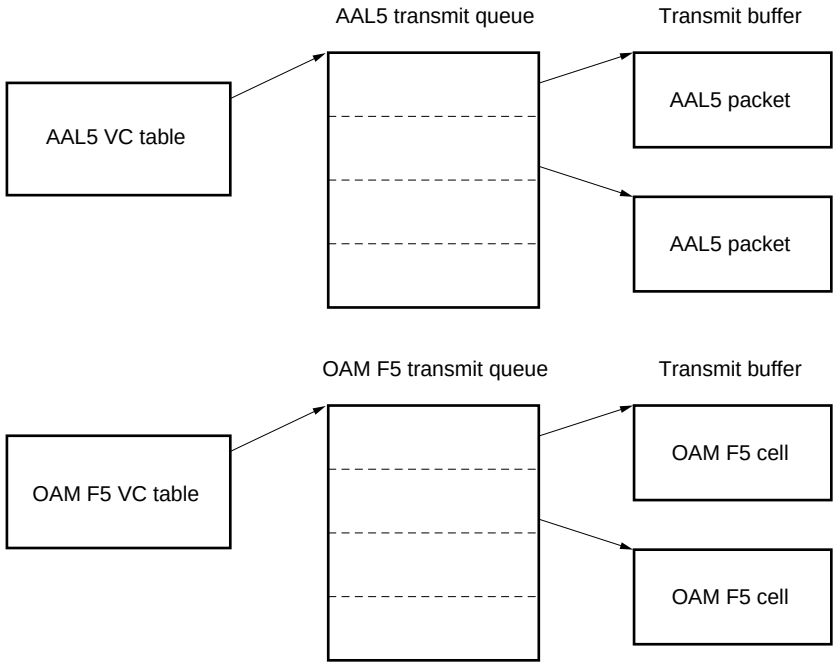
**A.7.11**

It can be transmitted in the following two ways:

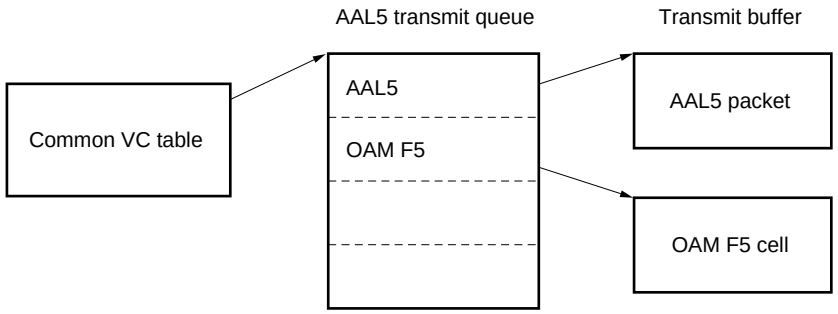
(1) Open two transmit VCs and set the same VPI/VCI values to them. These VCs can be transmitted at the same time with one for an AAL5 packet and the other for an OAM F5 cell. At this time, cell scheduling is determined depending on the setting of the shaper to which each VC is linked.

(2) Use one transmit VC and the packet descriptor of its transmit queue for an AAL5 packet and for an OAM F5 cell. In this case, the AAL5 packet and OAM F5 cell are alternately transmitted.

(1)




(2)



**Q.8.1**

What will happen if a cell of the VPI/VCI value not enabled by the receive lookup table has been received, and is it indicated?

**A.8.1**

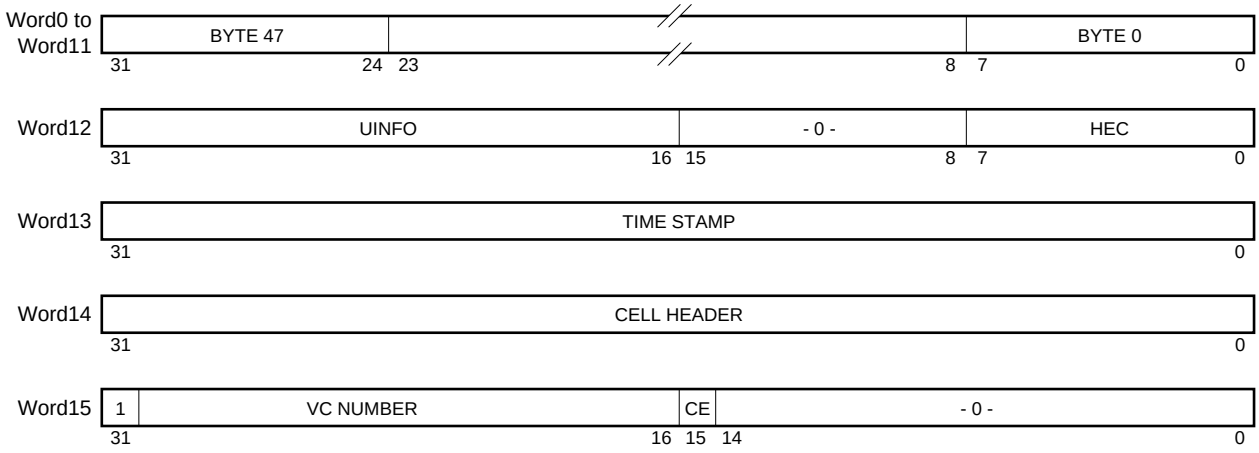
If a cell of the VPI/VCI value not enabled to be received is received, that cell is internally discarded. At this time, no indication, such as an interrupt, is made. The invalid VPI/VCI cell counter (RUEC register) is incremented.

**Q.8.2**

How is a CRC-10 error reported when a Raw cell is received? Is it possible to disable error check?

**A.8.2**

A CRC-10 error is reported by the CE bit in the Raw cell data when a Raw cell is received. At this time, no indication, such as an interrupt, is made. CRC-10 error check is always enabled. When CRC-10 error check is not used, ignore the CE bit in the Raw cell data.



**Q.8.3**

Is the number of batches in the receive pool limited?

**A.8.3**

Yes. Up to 64K, equal to the number of bits in the Remaining number of batches field of a receive pool descriptor.

**Q.8.4**

Is it possible to temporarily stop reception for each VC?

**A.8.4**

Yes. To stop reception, clear the enable bit of the receive lookup table for each VC. To resume reception, set the enable bit.

**Q.8.5**

Is there a case in which a receive batch is consumed even if receive indication including error information is reported?

**A.8.5**

Yes. The batches consumed until the error occurs can be recognized from the Packet size and Packet start address fields in the receive indication. If a receive FIFO overrun error occurs while the first cell of a packet is received, all the cells of that packet are internally discarded and no receive batch is consumed at this time. This is reported as Packet size = 0.

**Q.8.6**

Is only the user data of AAL5 CPCS-PDU stored in the receive buffer when an AAL5 packet is received?

**A.8.6**

The entire AAL5 CPCS-PDU including the user data, padding, and trailer is stored in the receive buffer.

**Q.8.7**

How should the T1 time register (T1R) be set to detect a T1 error?

**A.8.7**

The setting of the T1R register should be system clock time (SCLK input) × 64K. For example, where T1R = 5, the time required to detect a T1 error is 320K clocks (about 13.1 ms where SCLK = 25 MHz).

**Q.8.8**

Can the receive pool for Raw cell be shared with the receive pool for AAL5?

**A.8.8**

No. Separately set the receive pools for Raw cell and ALL5.

**Q.8.9**

Pools 0 to 7 are allocated as a receive pool for Raw cell. Can all the pools 0 through 7 be used for receiving Raw cells? Or, can only one of the pools 0 through 7 be used?

**A.8.9**

All the pools 0 through 7 can be used for receiving Raw cells.

**Q.8.10**

What is the Alert level of a receive pool descriptor? Are the setting and interrupt of Alert level valid for a Raw cell pool?

**A.8.10**

The setting and interrupt of Alert level are valid for the Raw cell pool. With the μPD98401A, they are invalid for the Raw cell pool.

**Q.8.11**

Why can't the VFM bit of the VRR register be accessed?

**A.8.11**

The VFM bit is newly provided to version 3.1 or above (VER register = 0103h) of the μPD98405. This bit is not provided to version 3.0 or below (VER register = 0102h) and bit 30 of the VRR register is a read-only bit and its value is 0. With version 3.0, the function of this bit is always to enable the VPI/VCI filtering function.

**Q.8.12**

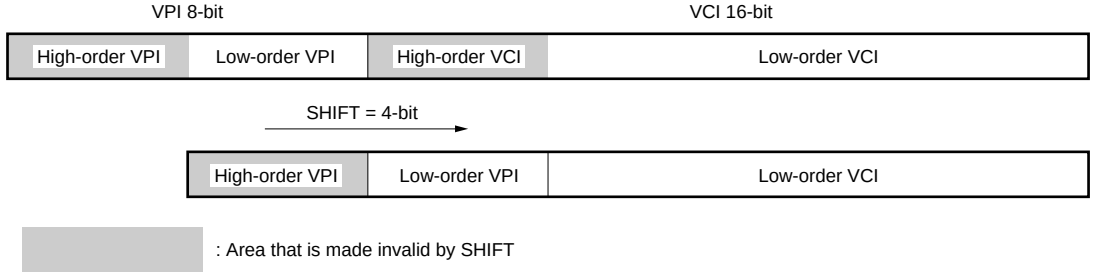
How is a receive cell discarded when the VPI/VCI filtering function (VFM bit = 0) is enabled by using the VRR register?

**A.8.12**

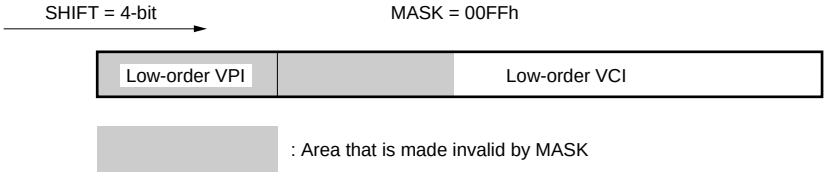
If a field that is made invalid by SHIFT received a cell having a VPI/VCI value other than 0, the μPD98405 discards that cell, and increments the RUEC register.

Even if a field that is made invalid by MASK received a cell having a VPI/VCI value other than 0, the μPD98405 does not discard that cell.

**Area that is made invalid by SHIFT (when SHIFT = 4)**




**Area that is made invalid by MASK (when MASK = 00FFh)**



**Q.8.13**

How should the UINFO field of the receive VC table and receive indication be used?

**A.8.13**

The value set in the UINFO field of the receive VC table is stored in the UINFO field of receive indication as is. The user may or may not use the UINFO field for any application as user information.

**Q.8.14**

What is the Packet size field of receive indication?

**A.8.14**

The Packet size field indicates the size of a receive packet. The packet size can be specified to be in cell units or byte units. If an error occurs, however, receive indication always reports the Packet size field in cell units. At this time, the packet size is the number of cells received and stored in the receive buffer until the error occurs.

## CHAPTER 9 TRANSMISSION/RECEPTION

**Q.9.1**

Can the contents of the transmit/receive VC table be changed during transmission or reception?

**A.9.1**

The contents of the VC table cannot be changed during transmission or reception, except Word12 of the receive table.

**Q.9.2**

How many bits can VPI/VCI support?

**A.9.2**

The transmission side can set and transmit any 24-bit VPI/VCI value. The reception side reduces the 24-bit VPI/VCI value to 16 bits.

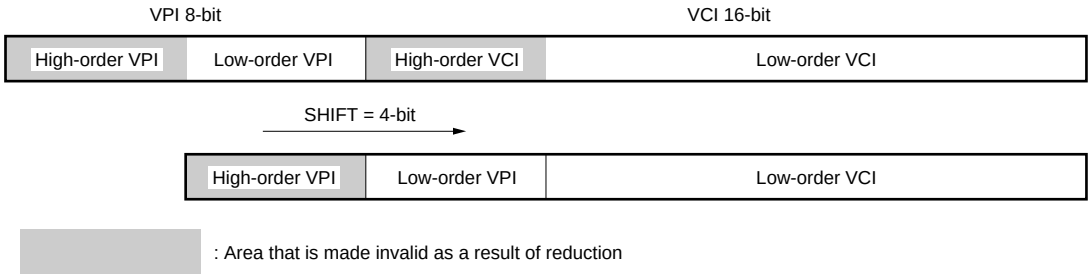
This reduction is done as follows:

VPI is shifted to the VCI side by using the SHIFT value of the VRR register and a 16-bit VPI/VCI value is generated.

If SHIFT = 0, the 16-bit VCI value is supported.

VPI/VCI reduction

If SHIFT = 4




**Q.9.3**

To what part is CRC-32 operation applied?

**A.9.3**

CRC-32 operation is applied to the entire CPCS-PDU frame of User data, Padding, CPCS-UU, CPI, and Length.

**Q.9.4**

Is the receive indication issued even when a Raw cell is received?

**A.9.4**

The receive indication is not issued when a Raw cell is received. When a Raw cell is received, it is stored in the receive buffer as Raw cell data and is reported only by the Raw cell receive interrupt (RCR7 through RCR0 bits of GSR register).

At the transmission side, the transmit indication is issued even when a Raw cell is transmitted.

## CHAPTER 10 COMMAND

**Q.10.1**

What will happen if the Tx_Ready command is issued to a VC that is transmitting a packet (active VC)?

**A.10.1**

The Tx_Ready command is ignored. However, the command is accepted and, if the command FIFO is not used, the Busy bit of the CMR register is set for a specified time.

**Q.10.2**

What will happen if the Close_Channel command is issued with an incorrect setting for transmit or receive VC specified by the R/T bit of the command?

**A.10.2**

The μPD98405 may malfunction if the setting of the R/T bit is incorrect because it performs close processing corresponding to a transmit or receive VC.

**Q.10.3**

When accessing the control memory by using the Indirect_Access command, can two or more addresses be accessed by issuing the command only once?

**A.10.3**

No. When the command is issued once, only one address can be read or written.

**Q.10.4**

What should the setting of the TGT field be when the internal PHY register or external PHY device is accessed by using the Indirect_Access command?

**A.10.4**

The internal PHY register or external PHY device can be accessed regardless of whether TGT = "11" or "10". This does not mean that the internal PHY register can be accessed only when TGT = "11" and that the external PHY device can be accessed only when TGT = "10".

**Q.10.5**

How is the NOP command used?

**A.10.5**

The NOP command is issued two times to close a receive VC after the receive lookup table has been disabled, in the following sequence:

(1) Disable the receive lookup table.
(2) Issue the NOP command two times.
(3) Issue the receive Deactivate_Channel command.
(4) Issue the receive Close_Channel command.

# CHAPTER 11 LOOPBACK

**Q.11.1**

Is the MIB counter valid even in loopback mode?

**A.11.1**

Yes. The MIB counter counts the number of transmit cells and the number of cells received by loopback.

**Q.11.2**

Is valid data output to the PHY side (UTOPIA interface) in SAR loopback mode?

**A.11.2**

No. The data is invalid and the TENBL_B of the UTOPIA interface is deasserted (high level).

**Q.11.3**

Does the pin status of the UTOPIA interface affect the transmit/receive operation of the μPD98405 in SAR loopback mode?

**A.11.3**

No. Even if TCALV/RCLAV of the UTOPIA interface is invalid, for example, the μPD98405 correctly executes transmission/reception.

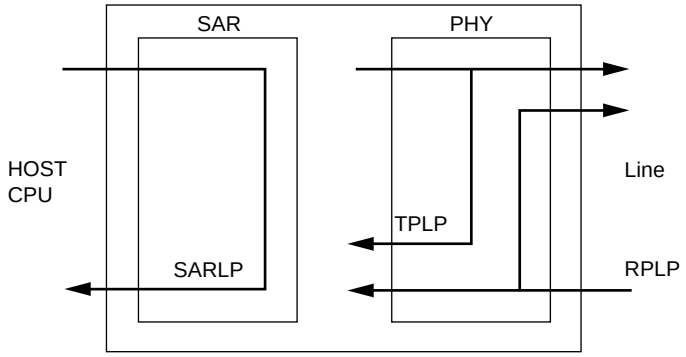
**Q.11.4**

Can SAR loopback mode and RPLP mode of PHY loopback be set and used at the same time?

**A.11.4**

Yes.

SAR loopback mode and TPLP mode of PHY loopback cannot be used at the same time.




**Q.11.5**

Is the loopback operation affected if data is received from the receive line side (if an optical cable is connected) in the TPLP mode of PHY loopback? If the optical cable is not connected, does a line fault, such as LOS, occur?

**A.11.5**

The data received from the receive line side is not affected in the TPLP mode. A line fault does not occur regardless of whether the receive line is connected or disconnected.

**Q.12.1**

Can the receive clock extracted by receive clock recovery be used as a reference clock at the transmission side? Can network synchronization be supported?

**A.12.1**

The reference clock of the transmit synthesizer is only REFCLK input (19.44 MHz). Network synchronization for synchronizing the transmission side with the receive clock cannot be supported.

## CHAPTER 13 REGISTER

**Q.13.1**

What is the function of the ADDR register?

**A.13.1**

This is a test register that stores the address of the last DMA transfer executed in general-purpose bus mode. This register is invalid in PCI bus mode.

**Q.13.2**

How should the ECCR and ERDR register be initialized?

**A.13.2**

The ECCR and ERDR registers are not initialized after software reset. They are initialized after hardware reset, and their default values are: ECCR = 0 and ERDR = undefined.

**Q.13.3**

The corresponding bits of the PCPR1 and PCPR2 registers are automatically reset or set each time each window register has been read. Can the low-order bits of a counter be read by writing, for example, 0 to each bit of the PCPR1 and PCPR2 registers?

**A.13.3**

Yes. The desired bits of the counter can be read by forcibly writing 0 or 1 to the corresponding bit of the PCPR1 and PCPR2 registers.

**Q.13.4**

Can the area of the ABR lookup table be eliminated by setting the ALA register to the TOS register when the ABR function is not used?

**A.13.4**

Yes. The ABR lookup table area is not necessary when the ABR function is not used.

**Q.13.5**

Is the clearing condition of the PI bit of the GSR register related to setting of the PHY interrupt mode (MDR2 register)?

**A.13.5**

No. The PI bit of the GSR register is always cleared when it is read.

**Q.13.6**

Can transmission/reception be temporarily halted by clearing the SE and RE bit of the GMR register during transmission/reception?

**A.13.6**

Yes. If the SE and RE bits are set again, transmission/reception is resumed. While the SE and RE bits are cleared, however, transmission is stopped. While transmission is stopped, the rate cannot be adjusted as set. At the reception side, the cells received during this time are internally discarded.

**Q.13.7**

What is the value of the VER register?

**A.13.7**

Ver. 3.0: VER = 0102h
Ver. 3.1: VER = 0103h

For the other versions, consult NEC.

**Q.13.8**

Should the TBW and AUB registers be set even when ABR is not used, and does this setting affect the entire band of VBR?

**A.13.8**

The TBW and AUB registers do not have to be set when ABR is not used. This setting does not affect the entire band of VBR.

**Q.14.1**

How can the JTAG function be reset when JTAG is not used?

**A.14.1**

JTAG can be reset by using or not using the JRST_B pin.

**When not using the JRST_B pin:**

The JTAG function can be reset by using the JMS and JCK pins while the JRST_B pin is pulled up.
Input the clock five times to the JCK pin while the JMS pin is pulled up.

**When using the JRST_B pin:**

The JTAG function can be reset by inputting a low level to the JRST_B pin while the JRST_B and JMS pins are pulled up. At this time, the low-level width must be one clock cycle of SCLK input or more. If the JRST_B pin is kept low (pull down, etc.), the JTAG function is reset, regardless of the status of the JMS pin.

# CHAPTER 15 AC/DC CHARACTERISTICS

**Q.15.1**

How much is the current consumption if the internal PHY function is not used?

**A.15.1**

The current consumption is not specified under special conditions such as when the internal PHY function is not used. Only the current consumption during normal operation is shown in the μPD98405 Data Sheet. The current consumption when the internal PHY function is not used is almost the same as under the normal condition.

**Q.15.2**

When +5 V is supplied to the $V_{DD5}$ pin, how much is the current consumption of the power supply?

**A.15.2**

The +5 V power supply is used only to supply 5 V to the PCI bus interface and does not affect the internal operation. Therefore, even if +5 V is supplied to the $V_{DD5}$ pin, the power consumption is the normal current consumption (refer to **μPD98405 Data Sheet**) × 3.3 V.

**Q.15.3**

Can a 5 V device be directly connected to the control memory and UTOPIA interface? At that time, does the processing of the $V_{DD5}$ pin influence this connection?

**A.15.3**

A 5 V device can be directly connected to the control memory and UTOPIA Interface. The power supplied to the $V_{DD5}$ pin at this time has nothing to do with the device. Supply +5 V to the $V_{DD5}$ pin only when a 5 V PCI interface is used.

## CHAPTER 16 OTHERS

**Q.16.1**

Access is prohibited for 20 clocks (SCLK input) after reset. Does this mean that access is prohibited only after hardware reset?

**A.16.1**

Access is prohibited for 20 clocks after both hardware and software reset.

**Q.16.2**

Are there any differences in initialization of the device between hardware reset (input of a low level to the RST_B pin) and software reset (writing the SWR register)?

**A.16.2**

Basically, the initialization operation is the same but there is the following difference.

After software reset, the PCI configuration register, and ECCR and ERDR registers are not initialized. In addition, EEPROM connection is not checked.

**[MEMO]**

Phase-out/Discontinued

NEC

# Facsimile Message

From:

Name

Company

Tel. FAX

Address

Although NEC has taken all possible steps to ensure that the documentation supplied to our customers is complete, bug free and up-to-date, we readily accept that errors may occur. Despite all the care and precautions we've taken, you may encounter problems in the documentation. Please complete this form whenever you'd like to report errors or suggest improvements to us.

*Thank you for your kind support.*

**North America**
NEC Electronics Inc.
Corporate Communications Dept.
Fax: 1-800-729-9288
1-408-588-6130

**Europe**
NEC Electronics (Europe) GmbH
Technical Documentation Dept.
Fax: +49-211-6503-274

**South America**
NEC do Brasil S.A.
Fax: +55-11-6462-6829

**Hong Kong, Philippines, Oceania**
NEC Electronics Hong Kong Ltd.
Fax: +852-2886-9022/9044

**Korea**
NEC Electronics Hong Kong Ltd.
Seoul Branch
Fax: 02-528-4411

**Taiwan**
NEC Electronics Taiwan Ltd.
Fax: 02-2719-5951

**Asian Nations except Philippines**
NEC Electronics Singapore Pte. Ltd.
Fax: +65-250-3583

**Japan**
NEC Semiconductor Technical Hotline
Fax: 044-435-9608

I would like to report the following error/make the following suggestion:

Document title: _____

Document number: _____ Page number: _____

If possible, please fax the referenced page or drawing.

| Document Rating | Excellent | Good | Acceptable | Poor |
|---|---|---|---|---|
| Clarity | ❑ | ❑ | ❑ | ❑ |
| Technical Accuracy | ❑ | ❑ | ❑ | ❑ |
| Organization | ❑ | ❑ | ❑ | ❑ |