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Renesas Electronics Corporation

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SPECIAL-FUNCTION REGISTER TABLE

(Applied products★: μPD78355, 78356, 78P356)

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SPECIAL-FUNCTION REGISTER (SFR) LIST (1/3)

Address	Special function register (SFR) name	Symbol	R/W	Access Unit (Bit)			State after RESET
				1-bit	8-bit	16-bit	
FF00H	Port 0	P0	R/W	○	○	–	Undefined
FF01H	Port 1	P1		○	○	–	
FF02H	Port 2	P2	Note 1 R/W	○	○	–	
FF03H	Port 3	P3	R/W	○	○	–	
FF04H	Port 4Note 2	P4		○	○	–	
FF05H	Port 5Note 2	P5		○	○	–	
FF07H	Port 7	P7	R	○	○	–	
FF08H	Port 8	P8	R/W	○	○	–	
FF09H	Port 9	P9		○	○	–	
FF0AH	Port 10	P10		○	○	–	
FF10H	Capture/compare register 00	CC00		–	–	○	
FF11H							
FF12H	Capture/compare register 01	CC01		–	–	○	
FF13H							
FF14H	Capture/compare register 02	CC02		–	–	○	
FF15H							
FF16H	Capture/compare register 30	CC30		–	–	○	
FF17H							
FF18H	Capture/compare register 31	CC31		–	–	○	
FF19H							
FF1AH	Compare register 00	CM00		–	–	○	
FF1BH							
FF1CH	Compare register 01	CM01		–	–	○	
FF1DH							
FF1EH	Compare register 02	CM02		–	–	○	
FF1FH							
FF20H	Port 0 mode register	PM0		○	○	–	FFH
FF21H	Port 1 mode register	PM1		○	○	–	
FF22H	Port 2 mode register	PM2	Note 3 R/W	○	○	–	
FF23H	Port 3 mode register	PM3	R/W	○	○	–	
FF25H	Port 5 mode registerNote 2	PM5		○	○	–	
FF28H	Port 8 mode register	PM8		○	○	–	
FF29H	Port 9 mode register	PM9		○	○	–	0FH
FF2AH	Port 10 mode register	PM10		○	○	–	FFH
FF30H	Timer register 0	TM0	R	–	–	○	0000H
FF31H							

Address	Special function register (SFR) name	Symbol	R/W	Access Unit (Bit)			State after RESET
				1-bit	8-bit	16-bit	
FF32H	Timer register 1	TM1	R	–	–	○	0000H
FF33H							
FF34H	Timer register 2	TM2		–	–	○	
FF35H							
FF36H	Timer register 3	TM3		–	–	○	
FF37H							
FF38H	Timer register 4	TM4		–	–	○	
FF39H							
FF3AH	Presettable up/down count register	UDC	R/W	–	–	○	
FF3BH							
FF3CH	External interrupt mode register 0	INTM0		○	○	–	00H
FF3DH	External interrupt mode register 1	INTM1		○	○	–	
FF40H	Port 0 mode control register	PMC0		○	○	–	
FF42H	Port 2 mode control register	PMC2	Note 3 R/W	○	○	–	01H
FF43H	Port 3 mode control register	PMC3	R/W	○	○	–	00H
FF44H	Pull-up resistor option register L	PUOL		○	○	–	
FF45H	Pull-up resistor option register H	PUOH		○	○	–	
FF48H	Port 8 mode control register	PMC8		○	○	–	
FF4AH	Port 10 mode control register	PMC10		○	○	–	
FF50H	Compare register 03	CM03		–	–	○	Undefined
FF51H							
FF52H	Compare register 10	CM10		–	–	○	
FF53H							
FF54H	Compare register 11	CM11		–	–	○	
FF55H							
FF56H	Compare register 20	CM20		–	–	○	
FF57H							
FF58H	Compare register 21	CM21		–	–	○	
FF59H							
FF5AH	Compare register 40	CM40		–	–	○	
FF5BH							

Notes 1. Bit 0 is read only.

2. Not available in the μPD78355.

3. Bit 0 is fixed to "1".

In this document, some bit numbers of register format are circled. These bit names are defined as reserved word in RA78K/III, and defined in the header file "sfrbit. h" of CC78K/III.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

The mark ★ shows revised points.

Phase-out/Discontinued

SPECIAL-FUNCTION REGISTER (SFR) LIST

Address	Special function register (SFR) name	Symbol	R/W	Access Unit (Bit)			State after RESET
				1-bit	8-bit	16-bit	
FF5CH	Up/down counter compare register 0	CMUD0	R/W	–	–	○	Undefined
FF5DH							
FF5EH	Up/down counter compare register 1	CMUD1		–	–	○	
FF5FH							
FF60H	Real-time output port register L	RTPL		○	○	–	
FF61H	Real-time output port register H	RTPH		○	○	–	
FF62H	Port read control register	PRDC		○	○	–	00H
FF63H	Real-time output port mode register	RTPM		○	○	–	
FF68H	A/D converter mode register 0	ADM0		○	○	–	
FF69H	A/D converter mode register 1	ADM1		○	○	–	07H
FF6AH	D/A conversion setting register 0	DACS0		○	○	–	00H
FF6BH	D/A conversion setting register 1	DACS1		○	○	–	
FF6AH	D/A conversion setting register	DACS		–	–	○	0000H
FF6BH							
FF70H	Timer unit mode register 0	TUM0		○	○	–	00H
FF71H	Timer unit mode register 1	TUM1		○	○	–	
FF72H	Timer unit mode register 2	TUM2		○	○	–	
FF73H	Timer unit mode register 3	TUM3		○	○	–	
FF74H	Timer control register 0	TMC0		○	○	–	
FF75H	Timer control register 1	TMC1		○	○	–	
FF76H	Timer control register 2	TMC2		○	○	–	04H
FF77H	Up/down counter control register	UDCC		○	○	–	00H
FF78H	Timer output control register 0	TOC0		○	○	–	
FF79H	Timer output control register 1	TOC1		○	○	–	
FF7AH	Timer output control register 2	TOC2		○	○	–	
FF7BH	Timer overflow status register	TOVS	Note 1 R/W	○	○	–	
FF7CH	Noise protection control register	NPC	R/W	○	○	–	
FF80H	Clock synchronous serial interface mode register 0	CSIM0		○	○	–	
FF82H	Serial bus interface control register	SBIC	Note 2 R/W	○	○	–	

Address	Special function register (SFR) name	Symbol	R/W	Access Unit (Bit)			State after RESET
				1-bit	8-bit	16-bit	
FF86H	Serial I/O shift register 0	SIO0	R/W	○	○	–	Undefined
FF88H	Asynchronous serial interface mode register	ASIM		○	○	–	80H
FF8AH	Asynchronous serial interface mode register	ASIS	R	○	○	–	00H
FF8CH	Serial reception buffer : UART	RXB		–	○	–	Undefined
FF8EH	Serial transmission shift register : UART	TXS	W	–	○	–	
FF90H	Clock synchronous serial interface mode register 1	CSIM1	R/W	○	○	–	00H
FF96H	Serial I/O shift register 1	SIO1		○	○	–	Undefined
FFA0H	PWM control register	PWMC		○	○	–	00H
FFA2H	PWM register 0L	PWM0L		○	○	–	Undefined
FFA2H	PWM register 0	PWM0		–	–	○	
FFA3H							
FFA4H	PWM register 1L	PWM1L		○	○	–	
FFA4H	PWM register 1	PWM1		–	–	○	
FFA5H							
FFA8H	In-service priority register	ISPR	R	○	○	–	00H
FFAAH	Interrupt mode control register	IMC	R/W	○	○	–	80H
FFACH	Interrupt mask register	MK0L		○	○	–	FFH
FFACH	Interrupt mask register	MK0		–	–	○	FFFFH
FFADH							
FFADH	Interrupt mask register	MK0H		○	○	–	FFH
FFAEH	Interrupt mask register	MK1L		○	○	–	
FFAEH	Interrupt mask register	MK1		–	–	○	00FFH
FFAFH							
FFB0H	A/D conversion result register 0	ADCR0	R	–	–	○	Undefined
FFB1H							
FFB1H	A/D conversion result register 0H	ADCR0H		–	○	–	
FFB2H	A/D conversion result register 1	ADCR1		–	–	○	
FFB3H							
FFB3H	A/D conversion result register 1H	ADCR1H		–	○	–	
FFB4H	A/D conversion result register 2	ADCR2		–	–	○	
FFB5H							
FFB5H	A/D conversion result register 2H	ADCR2H		–	○	–	
FFB6H	A/D conversion result register 3	ADCR3		–	–	○	
FFB7H							
FFB7H	A/D conversion result register 3H	ADCR3H		–	○	–	

Notes 1. Bits 7 and 6 : Fixed to 0
Bits 5, 4, 2, 1 : Read/write
Bits 3 and 0 : Read-only

2. Bits 7 and 5 : Read/write
Bits 6, 3, 2 : Read-only
Bits 4, 1, 0 : Write-only

Phase-out/Discontinued

SPECIAL-FUNCTION REGISTER (SFR) LIST

Address	Special function register (SFR) name	Symbol	R/W	Access Unit (Bit)			State after RESET
				1-bit	8-bit	16-bit	
FFB8H	A/D conversion result register 4	ADCR4	R	–	–	○	Undefined
FFB9H							
FFB9H	A/D conversion result register 4H	ADCR4H		–	○	–	
FFBAH	A/D conversion result register 5	ADCR5		–	–	○	
FFBBH							
FFBBH	A/D conversion result register 5H	ADCR5H		–	○	–	
FFBCH	A/D conversion result register 6	ADCR6		–	–	○	
FFBDH							
FFBDH	A/D conversion result register 6H	ADCR6H		–	○	–	
FFBEH	A/D conversion result register 7	ADCR7		–	–	○	
FFBFH							
FFBFH	A/D conversion result register 7H	ADCR7H		–	○	–	
FFC0H	Standby control register	Note 1 STBC	R/W	–	○	–	0000 X000B
FFC1H	CPU control word	CCW		○	○	–	00H
FFC2H	Watchdog timer mode register	Note 1 WDM		–	○	–	
FFC4H	Memory expansion mode register	MM		○	○	–	
FFC6H	Programmable wait control register	PWC		–	–	○	Note 2 C0AAH
FFC7H							
FFD0H – FFDFH	External SFR area	–		○	○	–	Undefined
FFE0H	Interrupt control register (INTOV0)	OVIC0		○	○	–	43H
FFE1H	Interrupt control register (INTOV3)	OVIC3		○	○	–	
FFE2H	Interrupt control register (INTP0/CC00)	PIC0		○	○	–	
FFE3H	Interrupt control register (INTP1/CC01)	PIC1		○	○	–	
FFE4H	Interrupt control register (INTP2/CC02)	PIC2		○	○	–	

Address	Special function register (SFR) name	Symbol	R/W	Access Unit (Bit)			State after RESET
				1-bit	8-bit	16-bit	
FFE5H	Interrupt control register (INTP3/CC30)	PIC3	R/W	○	○	–	43H
FFE6H	Interrupt control register (INTP4/CC31)	PIC4		○	○	–	
FFE7H	Interrupt control register (INTCM00)	CMIC00		○	○	–	
FFE8H	Interrupt control register (INTCM01)	CMIC01		○	○	–	
FFE9H	Interrupt control register (INTCM02)	CMIC02		○	○	–	
FFEAH	Interrupt control register (INTCM03)	CMIC03		○	○	–	
FFEBH	Interrupt control register (INTCM10)	CMIC10		○	○	–	
FFECH	Interrupt control register (INTCM11)	CMIC11		○	○	–	
FFEDH	Interrupt control register (INTCM20)	CMIC20		○	○	–	
FFEEH	Interrupt control register (INTCM21)	CMIC21		○	○	–	
FFEFH	Interrupt control register (INTCM40)	CMIC40		○	○	–	
FFF0H	Interrupt control register (INTCMUD0)	CMICUD0		○	○	–	
FFF1H	Interrupt control register (INTCMUD1)	CMICUD1		○	○	–	
FFF2H	Interrupt control register (INTSER)	SERIC		○	○	–	
FFF3H	Interrupt control register (INTSR)	SRIC		○	○	–	
FFF4H	Interrupt control register (INTST)	STIC		○	○	–	
FFF5H	Interrupt control register (INTCSI0)	CSIIC0		○	○	–	
FFF6H	Interrupt control register (INTCSI1)	CSIIC1		○	○	–	
FFF7H	Interrupt control register (INTAD)	ADIC		○	○	–	

Notes 1. Write is enabled only by special instructions.

2. CFAAH when MODE0 and MODE1 = HH (external 16-bit bus, ROM-less mode) ★

1. Port

Port mode register

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
PM0	PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00	FF20H	FFH	R/W
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	1	FF22H	FFH	R/W
PM3	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	FF23H	FFH	R/W
PM5	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	FF25H	FFH	R/W
PM8	PM87	PM86	PM85	PM84	PM83	PM82	PM81	PM80	FF28H	FFH	R/W
PM9	0	0	0	0	PM93	PM92	PM91	PM90	FF29H	0FH	R/W
PM10	PM10 7	PM10 6	PM10 5	PM10 4	PM10 3	PM10 2	PM10 1	PM10 0	FF2AH	FFH	R/W

PMXn	Specifies I/O mode of pin PXn (X=0-3, 5, 8, 10; n=0-7) (X=9; n=0-3)
0	Output mode (output buffer ON)
1	Input mode (output buffer OFF)

Port 2 mode control register

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
PMC2	PMC2 7	PMC2 6	PMC2 5	PMC2 4	PMC2 3	PMC2 2	PMC2 1	1	FF42H	01H	R/W

PMC21	Specifies control mode of pin P21
0	I/O port mode
1	INTP0 input mode/TO04 output mode

PMC22	Specifies control mode of pin P22
0	I/O port mode
1	INTP1 input mode/TO05 output mode

PMC23	Specifies control mode of pin P23
0	I/O port mode
1	INTP2 input mode

PMC24	Specifies control mode of pin P24
0	I/O port mode
1	INTP3 input mode

PMC25	Specifies control mode of pin P25
0	I/O port mode
1	INTP4 input mode

PMC26	Specifies control mode of pin P26
0	I/O port mode
1	TCLR2 input mode/TO21 output mode

PMC27	Specifies control mode of pin P27
0	I/O port mode
1	TO20 output mode

Port read control register

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
PRDC	0	0	0	0	0	0	0	PRDC 0	FF62H	00H	R/W

PRDC 0	Specifies operation mode
0	Normal mode
1	Pin access mode

Port 3 mode control register

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
PMC3	PMC3 7	PMC3 6	PMC3 5	PMC3 4	PMC3 3	PMC3 2	PMC3 1	PMC3 0	FF43H	00H	R/W

PMC30	Specifies control mode of pin P30
0	I/O port mode
1	TxD output mode

PMC31	Specifies control mode of pin P31
0	I/O port mode
1	RxD input mode

PMC32	Specifies control mode of pin P32
0	I/O port mode
1	SB0 I/O mode/SO00 output mode

PMC33	Specifies control mode of pin P33
0	I/O port mode
1	SB1 I/O mode/SI00 input mode

PMC34	Specifies control mode of pin P34
0	I/O port mode
1	$\overline{\text{SCK00}}$ I/O mode

PMC35	Specifies control mode of pin P35
0	I/O port mode
1	TCLR1 input mode

PMC36	Specifies control mode of pin P36
0	I/O port mode
1	TI1 input mode/TO11 output mode

PMC37	Specifies control mode of pin P37
0	I/O port mode
1	TO10 output mode

Port 0 mode control register

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
PMC0	PMC0 7	PMC0 6	PMC0 5	PMC0 4	PMC0 3	PMC0 2	PMC0 1	PMC0 0	FF40H	00H	R/W

PMC0n	Specifies control mode of pin P0n (n=0-3)
0	I/O port mode
1	Real-time output port mode/ ADTRG input mode

PMC0n	Specifies control mode of pin P0n (n=4-7)
0	I/O port mode
1	Real-time output port mode

Phase-out/Discontinued

Port 8 mode control register

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
PMC8	PMC87	PMC86	PMC85	PMC84	PMC83	PMC82	PMC81	PMC80	FF48H	00H	R/W

PMC80	Specifies control mode of pin P80
0	I/O port mode
1	TCLR0 input mode

PMC81	Specifies control mode of pin P81
0	I/O port mode
1	TI0 input mode/TO03 output mode

PMC82	Specifies control mode of pin P82
0	I/O port mode
1	TO00 output mode

PMC83	Specifies control mode of pin P83
0	I/O port mode
1	TO01 output mode

PMC84	Specifies control mode of pin P84
0	I/O port mode
1	TO02 output mode

PMC85	Specifies control mode of pin P85
0	I/O port mode
1	TCLRUD input mode

PMC86	Specifies control mode of pin P86
0	I/O port mode
1	PWM0 output mode

PMC87	Specifies control mode of pin P87
0	I/O port mode
1	PWM1 output mode

Port 10 mode control register

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
PMC10	PMC107	PMC106	PMC105	PMC104	PMC103	PMC102	PMC101	PMC100	FF4AH	00H	R/W

PMC100	Specifies control mode of pin P100
0	I/O port mode
1	SO10 output mode

PMC101	Specifies control mode of pin P101
0	I/O port mode
1	SI10 input mode

PMC102	Specifies control mode of pin P102
0	I/O port mode
1	$\overline{SCK10}$ I/O mode

PMC103	Specifies control mode of pin P103
0	I/O port mode
1	SO11 output mode

PMC104	Specifies control mode of pin P104
0	I/O port mode
1	SI11 input mode

PMC105	Specifies control mode of pin P105
0	I/O port mode
1	$\overline{SCK11}$ I/O mode

PMC106	Specifies control mode of pin P106
0	I/O port mode
1	TIUD input mode

PMC107	Specifies control mode of pin P107
0	I/O port mode
1	TCUD input mode

Pull-up resistor option register L

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
PUOL	0	0	PUO5	PUO4	PUO3	PUO2	PUO1	PUO0	FF44H	00H	R/W

PUOn	Pull-up resistor of port n (n=0-5)
0	Not provided
1	Provided

Pull-up resistor option register H

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
PUOH	0	0	0	0	0	PUO10	PUO9	PUO8	FF45H	00H	R/W

PUOn	Pull-up resistor of port n (n=8-10)
0	Not provided
1	Provided

2. A/D converter

A/D converter mode register 0

	⑦	6	5	4	3	2	1	0	Address	State after RESET	R/W
ADM0	CS	0	BS	MS	0	ANIS2	ANIS1	ANIS0	FF68H	00H	R/W

ANIS2	ANIS1	ANIS0	Select mode	Scan mode	
				A/D trigger mode	Timer/external trigger mode
0	0	0	ANI0	ANI0	1 time
0	0	1	ANI1	ANI0 - ANI1	2 times
0	1	0	ANI2	ANI0 - ANI2	3 times
0	1	1	ANI3	ANI0 - ANI3	4 times
1	0	0	ANI4	ANI0 - ANI4	ANI0 - ANI4
1	0	1	ANI5	ANI0 - ANI5	ANI0 - ANI5
1	1	0	ANI6	ANI0 - ANI6	ANI0 - ANI6
1	1	1	ANI7	ANI0 - ANI7	ANI0 - ANI7

MS	Specifies operation mode for A/D conversion
0	Scan mode
1	Select mode

BS	Specifies buffer mode in select mode
0	1-buffer mode
1	4-buffer mode

CS	Controls operation for A/D conversion
0	Stop
1	Start

★ A/D converter mode register 1

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
ADM1	EDG	TRG2	TRG1	TRG0	0	FR2	FR1	FR0	FF69H	07H	R/W

FR2	FR1	FR0	Number of conversion clock	Operation time for conversion (μs)		
				f_{CLK} = 16.0 MHz	f_{CLK} = 12.5 MHz	f_{CLK} = 8.0 MHz
0	0	0	8	Setting prohibited		
0	0	1	16	Setting prohibited		2.0
0	1	0	20			2.5
0	1	1	24			3.0
1	0	0	28	Setting prohibited	2.24	3.5
1	0	1	32	2.0	2.56	4.0
1	1	0	64	4.0	5.12	8.0
1	1	1	128	8.0	10.24	16.0

TRG2	TRG1	TRG0	Specifies trigger mode	
0	0	0	A/D trigger mode	
0	0	1		
0	1	0	Timer trigger mode	1-trigger mode
0	1	1		4-trigger mode
1	0	0	External trigger mode	1-trigger mode
1	0	1		4-trigger mode
Others			Setting prohibited	

EDG	Specifies active edge of external input signal in external trigger mode
0	Falling edge
1	Rising edge

Remark f_{CLK} : internal system clock

Timer unit mode register 2

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
TUM2	TES UD1	TES UD0	0	0	TES 11	TES 10	TES 01	TES 00	FF72H	00H	R/W

TESn1	TESn0	Specifies active edge of TIn (n=0, 1, UD)
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Rising and falling edges

Timer unit mode register 3

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
TUM3	CES UD1	CES UD0	CES 21	CES 20	CES 11	CES 10	CES 01	CES 00	FF73H	00H	R/W

CESn1	CESn0	Specifies active edge of TCLRn (n=0-2, UD)
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Rising and falling edges

3. Timer unit

Timer unit mode register 0

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
TUM0	TOM04	TOM02	TOM00	CMS 31	CMS 30	CMS 02	CMS 01	CMS 00	FF70H	00H	R/W

CMSmn	Specifies operation mode of capture/compare register (CCmn) (m=0, 3 n=0-2)
0	Capture mode
1	Compare mode

TOM0n	Specifies output mode of timer output pin (TO0n) (n=0, 2, 4)
0	Toggle output mode
1	Set/reset output mode

Timer unit mode register 1

	7	6	5	4	3	2	①	0	Address	State after RESET	R/W
TUM1	0	ECLR UD	0	ECLR 2	0	ECLR 1	OST	ECLR 0	FF71H	00H	R/W

ECLRn	Specifies clear mode of TCLRn (n=0-2, UD)
0	Disables clear by external input
1	Enables clear by external input

OST	Specifies operation in free running mode of TM0
0	Continues count up after timer overflow
1	Stops in clear state after timer overflow

Timer control register 0

	⑦	6	5	4	③	2	1	0	Address	State after RESET	R/W
TMC0	CE1	CLR1	PRM 11	PRM 10	CE0	CLR0	PRM 01	PRM 00	FF74H	00H	R/W

PRM01	PRM00	Specifies count clock to TM0 (Hz)
0	0	f_{CLK}/2
0	1	f_{CLK}/4
1	0	f_{CLK}/8
1	1	External clock (TI0 input)

CLR0	Specifies operation mode of TM0
0	Free running mode
1	Interval timer mode

CE0	Controls TM0 operation
0	TM0 is cleared and stopped
1	TM0 executes count operation

PRM11	PRM10	Specifies count clock to TM1 (Hz)
0	0	f_{CLK}/4
0	1	f_{CLK}/8
1	0	f_{CLK}/16
1	1	External clock (TI1 input)

CLR1	Specifies operation mode of TM1
0	Free running mode
1	Interval timer mode

CE1	Controls TM1 operation
0	TM1 is cleared and stopped
1	TM1 executes count operation

Remark f_{CLK} : internal system clock

Phase-out/Discontinued

Timer control register 1

	⑦	6	5	4	③	2	1	0	Address	State after RESET	R/W
TMC1	CE3	CLR3	PRM 31	PRM 30	CE2	CLR2	PRM 21	PRM 20	FF75H	00H	R/W

PRM21	PRM20	Specifies count clock to TM2 (Hz)
0	0	$f_{CLK}/4$
0	1	$f_{CLK}/8$
1	0	$f_{CLK}/16$
1	1	$f_{CLK}/32$

CLR2	Specifies operation mode of TM2
0	Free running mode
1	Interval timer mode

CE2	Controls TM2 operation
0	TM2 is cleared and stopped
1	TM2 executes count operation

PRM31	PRM30	Specifies count clock to TM3 (Hz)
0	0	$f_{CLK}/4$
0	1	$f_{CLK}/8$
1	0	$f_{CLK}/16$
1	1	$f_{CLK}/32$

CLR3	Specifies operation mode of TM3
0	Free running mode
1	Interval timer mode

CE3	Controls TM3 operation
0	TM3 is cleared and stopped
1	TM3 executes count operation

Remark f_{CLK} : internal system clock

Timer control register 2

	7	6	5	4	③	2	1	0	Address	State after RESET	R/W
TMC2	0	0	0	0	CE4	1	PRM 41	PRM 40	FF76H	04H	R/W

PRM41	PRM40	Specifies count clock (Hz) to TM4
0	0	f_{CLK}
0	1	$f_{CLK}/4$
1	0	$f_{CLK}/16$
1	1	$f_{CLK}/32$

CE4	Controls TM4 operation
0	TM4 is cleared and stopped
1	TM4 executes count operation

Remark f_{CLK} : internal system clock

Up/down counter control register

	⑦	6	5	4	3	2	1	0	Address	State after RESET	R/W
UDCC	CEUD	ENMD	PRM UD1	PRM UD0	$\overline{U}$/D	$\overline{I}$/E	0	0	FF77H	00H	R/W

$\overline{U}$/D	Specifies up/down count operation of UDC
0	Up count operation
1	Down count operation

PRM UD1	PRM UD0	$\overline{I}$/E	Count clock	Up/down count
0	0	0	$f_{CLK}/4$	Specified by $\overline{U}$/D bit
0	1	0	$f_{CLK}/8$	
1	0	0	$f_{CLK}/16$	
1	1	0	Setting prohibited	
0	0	1	TIUD (external clock)	Mode 1
0	1	1		Mode 2
1	0	1		Mode 3
1	1	1		Mode 4

ENMD	Specifies clear/preset operation of UDC by CMUD0
0	Disables clear/preset operation by CMUD0
1	Enables clear/preset operation by CMUD0

CEUD	Controls UDC operation
0	UDC is cleared and stopped
1	UDC executes count operation

Remark f_{CLK} : internal system clock

Timer output control register 0

	⑦	6	⑤	4	③	2	①	0	Address	State after RESET	R/W
TOC0	ENTO 03	ALV 03	ENTO 02	ALV 02	ENTO 01	ALV 01	ENTO 00	ALV 00	FF78H	00H	R/W

ALV00	Specifies active level of pin TO00
0	Low level
1	High level

ENTO 00	Specifies operation of pin TO00
0	Disables timer output (outputs ALV00)
1	Enables timer output

ALV01	Specifies active level of pin TO01
0	Low level
1	High level

ENTO 01	Specifies operation of pin TO01
0	Disables timer output (outputs ALV01)
1	Enables timer output

ALV02	Specifies active level of pin TO02
0	Low level
1	High level

ENTO 02	Specifies operation of pin TO02
0	Disables timer output (outputs ALV02)
1	Enables timer output

ALV03	Specifies active level of pin TO03
0	Low level
1	High level

ENTO 03	Specifies operation of pin TO03
0	TI0 input mode **Note**
1	Timer output mode

Note When bit PMC81 of PMC8 register is "1", if bit ENTO03 is reset (0), pin TO03 becomes high impedance.

Timer output control register 1

	⑦	6	⑤	4	③	2	①	0	Address	State after RESET	R/W
TOC1	ENTO 11	ALV 11	ENTO 10	ALV 10	ENTO 05	ALV 05	ENTO 04	ALV 04	FF79H	00H	R/W

ALV04	Specifies active level of pin TO04
0	Low level
1	High level

ENTO 04	Specifies operation of pin TO04
0	INTP0 input mode **Note 1**
1	Timer output mode

ALV05	Specifies active level of pin TO05
0	Low level
1	High level

ENTO 05	Specifies operation of pin TO05
0	INTP1 input mode **Note 2**
1	Timer output mode

ALV10	Specifies active level of pin TO10
0	Low level
1	High level

ENTO 10	Specifies operation of pin TO10
0	Disables timer output (outputs ALV10)
1	Enables timer output

ALV11	Specifies active level of pin TO11
0	Low level
1	High level

ENTO 11	Specifies operation of pin TO11
0	Disables timer output (outputs ALV11)
1	Enables timer output

Notes 1. When bit PMC21 of PMC2 register is "1", if bit ENTO04 is reset (0), pin TO04 becomes high impedance.

2. When bit PMC22 of PMC2 register is "1", if bit ENTO05 is reset (0), pin TO05 becomes high impedance.

Timer output control register 2

	7	6	5	4	③	2	①	0	Address	State after RESET	R/W
TOC2	TOM 20	TOM 10	0	0	ENTO 21	ALV 21	ENTO 20	ALV 20	FF7AH	00H	R/W

ALV20	Specifies active level of pin TO20
0	Low level
1	High level

ENTO 20	Specifies operation of pin TO20
0	Disables timer output (outputs ALV20)
1	Enables timer output

ALV21	Specifies active level of pin TO21
0	Low level
1	High level

ENTO 21	Specifies operation of pin TO21
0	TCLR2 input mode **Note**
1	Timer output mode

TOM10	Specifies output mode of pin TO10
0	Toggle output mode
1	Set/reset output mode

TOM20	Specifies output mode of pin TO20
0	Toggle output mode
1	Set/reset output mode

Note When bit PMC26 of PMC2 register is "1", if bit ENTO21 is reset (0), pin TO21 becomes high impedance.

Timer overflow status register

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
TOVS	0	0	UDF UD	OVF UD	OVF3	OVF2	OVF1	OVF0	FF7BH	00H	**Note**

R

OVF0	Overflow flag of TM0
0	Not overflowed
1	Overflowed

R/W

OVFn	Overflow flag of TMn (n=1, 2)
0	Not overflowed
1	Overflowed

R

OVF3	Overflow flag of TM3
0	Not overflowed
1	Overflowed

R/W

OVFUD	Overflow flag of UDC
0	Not overflowed
1	Overflowed

R/W

UDFUD	Underflow flag of UDC
0	Not underflowed
1	Underflowed

Note R/W differs by each bit.

Caution Bits OVF0 and OVF3 are cleared automatically by software write to bits OVIC0 and OVIC3 of interrupt control register or by hardware at starting interrupt processing.
Be sure to reset bits OVIF1, OVIF2, OVFUD, and UDFUD after resetting by software.

Noise protection control register

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
NPC	NRUD	NCUD	NIUD	NR2	NR1	NI1	NR0	NI0	FF7CH	00H	R/W

For TI0
For TCLR0
For TI1
For TCLR1
For TCLR2
For TIUD
For TCUD
For TCLRUD

Nxx	Specifies noise elimination time	★
0	4 clocks (250 ns : at f_{CLK}=16 MHz)	
1	16 clocks (1.0 μs : at f_{CLK}=16 MHz)	

Remark f_{CLK} : internal system clock

Real-time output port mode register

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
RTPM	TRH 1	TRH 0	TRL 1	TRL 0	0	RCM 2	RCM 1	RCM 0	FF63H	00H	R/W

RCM2	RCM1	RCM0	Specifies port 0 output bit of real-time output port register (RTPH, RTPL)	
			RTPH	RTPL
0	0	0	P07 - P00	\
0	0	1	P07 - P01	P00
0	1	0	P07 - P02	P01, P00
0	1	1	P07 - P03	P02 - P00
1	0	0	P07 - P04	P03 - P00
1	0	1	Setting prohibited	
1	1	0		
1	1	1		

TRL1	TRL0	Specifies trigger signal of real-time output port register (RTPL)
0	0	INTCM10
0	1	INTCM11
1	0	INTCM20
1	1	Software trigger

TRH1	TRH0	Specifies trigger signal of real-time output port register (RTPH)
0	0	INTCM10
0	1	INTCM11
1	0	INTCM20
1	1	Software trigger

5. Serial interface

Asynchronous serial interface mode register

	7	⑥	5	4	3	2	1	0	Address	State after RESET	R/W
ASIM	1	RXE	PS1	PS0	CL	SL	0	SCK	FF88H	80H	R/W

SCK	Specifies serial clock
0	Outputs internal baud rate generator
1	Internal clock f_{CLK}

SL	Specifies stop bit of transmission/reception data
0	1 bit
1	2 bits

CL	Character length of transmission/reception data
0	7 bits
1	8 bits

PS1	PS0	Specifies parity bit of transmission data
0	0	No parity
0	1	Transmission = add parity 0 Reception = no parity error
1	0	Parity of odd number
1	1	Parity of even number

RXE	Controls reception
0	Disables reception
1	Enables reception

Remark f_{CLK} : internal system clock

4. PWM unit

PWM control register

	⑦	6	5	4	③	2	1	0	Address	State after RESET	R/W
PWMC	PWME 1	ALV 1	PRM 11	PRM 10	PWME 0	ALV 0	PRM 01	PRM 00	FFA0H	00H	R/W

PRMn1	PRMn0	Bit length of counter and CMP register n (n=0, 1)
0	0	8 bits
0	1	10 bits
1	0	12 bits
1	1	Setting prohibited

ALVn	Specifies active level of PWMn signal output (n=0, 1)
0	Low level
1	High level

PWMEn	Controls operation of PWMn signal output (n=0, 1)
0	Operation stops
1	Enables operation

Asynchronous serial interface status register

	7	6	5	4	3	②	①	⓪	Address	State after RESET	R/W
ASIS	0	0	0	0	0	PE	FE	OVE	FF8AH	00H	R

OVE	Overrun error flag
1	The next reception is completed before reading data from reception buffer

FE	Framing error flag
1	Stop bit is not detected

PE	Parity error flag
1	Parity specification of transmission data and parity of reception data do not coincide

Clock synchronous serial interface mode register 0

	⑦	⑥	⑤	④	3	2	1	0	Address	State after RESET	R/W
CSIM0	CTXE 0	CRXE 0	WUP 0	MOD 02	MOD 01	MOD 00	CLS 01	CLS 00	FF80H	00H	R/W

CLS01	CLS00	Specifies serial clock		Pin $\overline{SCK}$
0	0	External clock		Input
0	1	Internal clock	Baud rate generator/2	Output
1	0		f_{CLK}/32	
1	1		f_{CLK}/8	

MOD 01	MOD 00	Operation mode	First bit	Number of used pin	Used pin
0	0	3-wire serial I/O mode	MSB	3	SO00/SB0, SI00/SB1, $\overline{SCK00}$
0	1		LSB		
1	0	SBI mode	MSB	2	SO00/SB0 (or SI00/SB1), $\overline{SCK00}$
1	1	Setting prohibited			

MOD 02	Specifies transmission/reception pin
0	Transmission/reception operation at pin SO00/SB0 (pin SI00/SB1 is high impedance)
1	Transmission/reception operation at pin SI00/SB1 (pin SO00/SB0 is high impedance)

WUP0	Control wake-up function
0	Generates interrupt request signal by serial transfer in every mode
1	Generates interrupt request signal only when address is received in SBI mode Serial output pin is high impedance

CRXE0	Reception operation
0	Disables ("0" is input to shift register if serial clock is input)
1	Enables

CTXE0	Transmission operation
0	Disables (output buffer of SO00/SB0, SI00/SB1 is high impedance)
1	Enables

Remark f_{CLK} : internal system clock

Serial bus interface control register

	⑦	⑥	⑤	④	③	②	①	⓪	Address	State after RESET	R/W
SBIC	BSYE	ACKD	ACKE	ACKT	CMDD	RELD	CMDT	RELT	FF82H	00H	**Note**

W	RELT	Controls trigger output of bus release signal (REL)
	0	Not output
	1	Output

W	CMDT	Controls trigger output of command signal (CMD)
	0	Not output
	1	Output

R	RELD	Detects bus release signal (REL)
	0	Not detected
	1	Detected

R	CMDD	Detects command signal (CMD)
	0	Not detected
	1	Detected

W	ACKT	Controls trigger output of acknowledge signal ($\overline{ACK}$)
	0	Not output
	1	Output

R/W	ACKE	Controls automatic output of acknowledge signal ($\overline{ACK}$)
	0	Disables
	1	Enables

R	ACKD	Detects acknowledge signal ($\overline{ACK}$)
	0	Not detected
	1	Detected

R/W	BSYE	Controls automatic output of synchronous busy signal ($\overline{BUSY}$)
	0	Disables
	1	Enables

Note R/W differs by each bit.

Clock synchronous serial interface mode register 1

	⑦	⑥	5	④	3	2	1	0	Address	State after RESET	R/W
CSIM1	CTXE 1	CRXE 1	0	MOD 12	0	MOD 10	CLS 11	CLS 10	FF90H	00H	R/W

CLS11	CLS10	Specifies serial clock		Pin $\overline{SCK}$
0	0	External clock		Input
0	1	Internal clock	Baud rate generator/2	Output
1	0		f_{CLK}/32	
1	1		f_{CLK}/8	

MOD 10	Operation mode	First bit	Number of used pin	Used pin
0	3-wire serial I/O mode	MSB	3	SO10/SI10, $\overline{SCK10}$ (or SO11, SI11, $\overline{SCK11}$)
1		LSB		

MOD 12	Specifies transmission/reception pin
0	Transmission/reception operation at pin SO10, SI10, $\overline{SCK10}$ (pin SO11, SI11, $\overline{SCK11}$ are high impedance)
1	Transmission/reception operation at pin SO11, SI11, $\overline{SCK11}$ (pin SO10, SI10, $\overline{SCK10}$ are high impedance)

CRXE1	Reception operation
0	Disables ("0" is input to shift register if serial clock is input)
1	Enables

CTXE1	Transmission operation
0	Disables (output buffer of SO10, SI10 (or SO11, SI11) are high impedance)
1	Enables

Remark f_{CLK} : internal system clock

6. Interrupt control

Interrupt control register

	⑦	⑥	⑤	④	3	2	①	⓪	Address	State after RESET	R/W
OVIC0	OVIF0	OV MK0	OV ISM0	OV CSE0	0	0	OV PR01	OV PR00	FFE0H	43H	R/W
OVIC3	OVIF3	OV MK3	OV ISM3	OV CSE3	0	0	OV PR31	OV PR30	FFE1H	43H	R/W
PIC0	PIF0	PMK0	PISM0	PCSE0	0	0	PPR01	PPR00	FFE2H	43H	R/W
PIC1	PIF1	PMK1	PISM1	PCSE1	0	0	PPR11	PPR10	FFE3H	43H	R/W
PIC2	PIF2	PMK2	PISM2	PCSE2	0	0	PPR21	PPR20	FFE4H	43H	R/W
PIC3	PIF3	PMK3	PISM3	PCSE3	0	0	PPR31	PPR30	FFE5H	43H	R/W
PIC4	PIF4	PMK4	PISM4	PCSE4	0	0	PPR41	PPR40	FFE6H	43H	R/W
CMIC00	CMIF 00	CMMK 00	CMISM 00	CMCSE 00	0	0	CMPR 001	CMPR 000	FFE7H	43H	R/W
CMIC01	CMIF 01	CMMK 01	CMISM 01	CMCSE 01	0	0	CMPR 011	CMPR 010	FFE8H	43H	R/W
CMIC02	CMIF 02	CMMK 02	CMISM 02	CMCSE 02	0	0	CMPR 021	CMPR 020	FFE9H	43H	R/W
CMIC03	CMIF 03	CMMK 03	CMISM 03	CMCSE 03	0	0	CMPR 031	CMPR 030	FFEAH	43H	R/W
CMIC10	CMIF 10	CMMK 10	CMISM 10	CMCSE 10	0	0	CMPR 101	CMPR 100	FFEBH	43H	R/W

Interrupt control register

	⑦	⑥	⑤	④	3	2	①	⓪	Address	State after RESET	R/W
CMIC11	CMIF 11	CMMK 11	CMISM 11	CMCSE 11	0	0	CMPR 111	CMPR 110	FFECH	43H	R/W
CMIC20	CMIF 20	CMMK 20	CMISM 20	CMCSE 20	0	0	CMPR 201	CMPR 200	FFEDH	43H	R/W
CMIC21	CMIF 21	CMMK 21	CMISM 21	CMCSE 21	0	0	CMPR 211	CMPR 210	FFEEH	43H	R/W
CMIC40	CMIF 40	CMMK 40	CMISM 40	CMCSE 40	0	0	CMPR 401	CMPR 400	FFEFH	43H	R/W
CMICUD0	CMIF UD0	CMMK UD0	CMISM UD0	CMCSE UD0	0	0	CMPR UD01	CMPR UD00	FFF0H	43H	R/W
CMICUD1	CMIF UD1	CMMK UD1	CMISM UD1	CMCSE UD1	0	0	CMPR UD11	CMPR UD10	FFF1H	43H	R/W
SERIC	SERIF	SERMK	SER ISM	SER CSE	0	0	SER PR1	SER PR0	FFF2H	43H	R/W
SRIC	SRIF	SRMK	SR ISM	SR CSE	0	0	SR PR1	SR PR0	FFF3H	43H	R/W
STIC	STIF	STMK	ST ISM	ST CSE	0	0	ST PR1	ST PR0	FFF4H	43H	R/W
CSIIC0	CSI IF0	CSI MK0	CSI ISM0	CSI CSE0	0	0	CSI PR01	CSI PR00	FFF5H	43H	R/W
CSIIC1	CSI IF1	CSI MK1	CSI ISM1	CSI CSE1	0	0	CSI PR11	CSI PR10	FFF6H	43H	R/W
ADIC	ADIF	ADMK	AD ISM	AD CSE	0	0	AD PR1	AD PR0	FFF7H	43H	R/W

××PR1	××PR0	Specifies priority
0	0	Priority 0 (highest)
0	1	Priority 1
1	0	Priority 2
1	1	Priority 3

××CSE	Context switching enable flag
0	Processed by vectored interrupt
1	Processed by context switching

××ISM	Macro service enable flag
0	Processed by vectored interrupt
1	Processed by macro service

××MK	Specifies enable/disable of interrupt request
0	Enables
1	Disables

××IF	Interrupt request flag
0	No interrupt request. No interrupt request signal occurred.
1	Interrupt request signal occurred and is requesting interrupt.

××PR1	××PR0	Specifies priority
0	0	Priority 0 (highest)
0	1	Priority 1
1	0	Priority 2
1	1	Priority 3

××CSE	Context switching enable flag
0	Processed by vectored interrupt
1	Processed by context switching

××ISM	Macro service enable flag
0	Processed by vectored interrupt
1	Processed by macro service

××MK	Specifies enable/disable of interrupt request
0	Enables
1	Disables

××IF	Interrupt request flag
0	No interrupt request. No interrupt request signal occurred.
1	Interrupt request signal occurred and is requesting interrupt.

Interrupt mask register
(at byte accessing)

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
MK0L	CMMK 00	PMK4	PMK3	PMK2	PMK1	PMK0	OVMK 3	OVMK 0	FFACH	FFH	R/W
MK0H	CMMK 40	CMMK 21	CMMK 20	CMMK 11	CMMK 10	CMMK 03	CMMK 02	CMMK 01	FFADH	FFH	R/W
MK1L	ADMK	CSI MK1	CSI MK0	STMK	SRMK	SERMK	CMMK UD1	CMMK UD0	FFAEH	FFH	R/W

××MK	Specifies enable/disable of interrupt request
0	Enables
1	Disables

(at word accessing)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
MK0	CMMK 40	CMMK 21	CMMK 20	CMMK 11	CMMK 10	CMMK 03	CMMK 02	CMMK 01	CMMK 00	PMK4	PMK3	PMK2	PMK1	PMK0	OVMK 3	OVMK 0	FFACH	FFFFH	R/W
MK1	0	0	0	0	0	0	0	0	ADMK	CSI MK1	CSI MK0	STMK	SRMK	SERMK	CMMK UD1	CMMK UD0	FFAEH	00FFH	R/W

··MK	Specifies enable/disable of interrupt request
0	Enables
1	Disables

Relation between each bit and interrupt request source

Register	Bit position	Bit name	Interrupt request source
MK0	Bit 0	OVMK0	Overflow of timer 0 (INTOV0)
	Bit 1	OVMK3	Overflow of timer 3 (INTOV3)
	Bit 2	PMK0	Coincidence of INTP0 pin input and CC00 (INTP0/INTCC00)
	Bit 3	PMK1	Coincidence of INTP1 pin input and CC01 (INTP1/INTCC01)
	Bit 4	PMK2	Coincidence of INTP2 pin input and CC02 (INTP2/INTCC02)
	Bit 5	PMK3	Coincidence of INTP3 pin input and CC30 (INTP3/INTCC30)
	Bit 6	PMK4	Coincidence of INTP4 pin input and CC31 (INTP4/INTCC31)
	Bit 7	CMMK00	Coincidence of CM00 (INTCM00)
	Bit 8	CMMK01	Coincidence of CM01 (INTCM01)
	Bit 9	CMMK02	Coincidence of CM02 (INTCM02)
	Bit 10	CMMK03	Coincidence of CM03 (INTCM03)
	Bit 11	CMMK10	Coincidence of CM10 (INTCM10)
	Bit 12	CMMK11	Coincidence of CM11 (INTCM11)
	Bit 13	CMMK20	Coincidence of CM20 (INTCM20)
	Bit 14	CMMK21	Coincidence of CM21 (INTCM21)
	Bit 15	CMMK40	Coincidence of CM40 (INTCM40)

Relation between each bit and interrupt request source

Register	Bit position	Bit name	Interrupt request source
MK1	Bit 0	CMMKUD0	Coincidence of CMUD0 (INTCMUD0)
	Bit 1	CMMKUD1	Coincidence of CMUD1 (INTCMUD1)
	Bit 2	SERMK	Serial error interrupt (INTSER)
	Bit 3	SRMK	Serial reception finish interrupt (INTSR)
	Bit 4	STMK	Serial transmission finish interrupt (INTST)
	Bit 5	CSIMK0	Serial transmission/reception finish interrupt (INTCSI0)
	Bit 6	CSIMK1	Serial transmission/reception finish interrupt (INTCSI1)
	Bit 7	ADMK	A/D conversion finish interrupt (INTAD)

Phase-out/Discontinued

Interrupt mode control register

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
IMC	PRSL	0	0	0	0	0	0	0	FFAAH	80H	R/W

PRSL	Controls nesting operation
0	Enables nesting between interrupts set to level 3 (lowest level)
1	Disables nesting between interrupts set to level 3 (lowest level)

In-service priority register

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
ISPR	0	0	0	0	ISPR3	ISPR2	ISPR1	ISPR0	FFA8H	00H	R

ISPRn	Priority level (n=0-3: priority)
0	Interrupt of priority n is not accepted
1	Interrupt of priority n is being accepted

External interrupt mode register 0

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
INTM0	ES21	ES20	ES11	ES10	ES01	ES00	0	ESN0	FF3CH	00H	R/W

ESN0	Specifies active edge of NMI
0	Falling edge
1	Rising edge

ESn1	ESn0	Specifies active edge of INTPn (n=0-2)
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Rising and falling edges

External interrupt mode register 1

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
INTM1	0	0	0	0	ES41	ES40	ES31	ES30	FF3DH	00H	R/W

ES31	ES30	Specifies active edge of INTP3
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Rising and falling edges

ES41	ES40	Specifies active edge of INTP4 pin input
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Rising and falling edges

7. Watchdog timer

Watchdog timer mode register

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
WDM	RUN	0	0	PRC	0	WDI2	WDI1	0	FFC2H	00H	R/W

WDI2	WDI1	Count clock	Overflow time (ms)	
			f_{CLK}= 12.5 MHz	f_{CLK}= 16.0 MHz
0	0	$f_{CLK}/2^9$	10.5	8.2
0	1	$f_{CLK}/2^{11}$	41.9	32.8
1	0	$f_{CLK}/2^{13}$	167.8	131.1
1	1	Setting prohibited		

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PRC	Priority if watchdog timer interrupt request
0	Interrupt request of NMI pin input > interrupt request of watchdog timer
1	Interrupt request of NMI pin input < interrupt request of watchdog timer

RUN	Specifies operation of watchdog timer
0	Stops watchdog timer
1	Watchdog timer is cleared and starts counting

Caution Only dedicated instructions (MOV WDM and #byte) can write to WDM.

Remark f_{CLK} : internal system clock

8. CPU control

Standby control register

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
STBC	0	0	0	0	SBF	0	STP	HLT	FFC0H	0000 X000B	R/W

Specification bit of HALT mode
When "1" is written, it becomes HALT mode. When HALT mode is released, it is reset to 0.

Specification bit of STOP mode
When "1" is written, it becomes STOP mode. When STOP mode is released, it is reset to 0.

Judging bit of cold start/hot start
It is reset only at the rise of power supply voltage. Cannot be reset to 0 by software.

Caution Only dedicated instructions (MOV STBC and #byte) can write to STBC.

CPU control word

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
CCW	0	0	0	0	0	0	TPF	0	FFC1H	00H	R/W

TPF	Specifies vector table field
0	0000H-007FH are used as vector table field
1	8000H-807FH are used as vector table field

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9. External bus interface control

Memory expansion mode register

	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
MM	0	MM6	MM5	0	MM3	MM2	MM1	MM0	FFC4H	00H	R/W

MM2	MM1	MM0	Specifies operation mode of pins P40 - P47, P50 - P57		
0	0	0	Port mode	Single-chip mode	P40 - P47 : input port P50 - P57 : port mode
0	0	1			P40 - P47 : output port P50 - P57 : port mode
0	1	0	Setting prohibited		
0	1	1	Expansion mode	256 bytes	P40 - P47 : expansion mode P50 - P57 : port mode
1	0	0		4 K bytes	P40 - 47, P50 - P53 : expansion mode P54 - P57 : port mode
1	0	1		16 K bytes	P40 - 47, P50 - P55 : expansion mode P56, P57 : port mode
1	1	0	Setting prohibited		
1	1	1	Expansion mode	Full-expansion mode	P40 - P47, P50 - P57 : expansion mode

MM3	Internal RAM size
0	2 K bytes
1	1 K bytes

MM6	MM5	Internal ROM size
0	0	48 K bytes
0	1	32 K bytes
1	0	24 K bytes
1	1	16 K bytes

Cautions 1. Be sure to input "0" to bits 4 and 7. If "1" is set, it does not operate normally.

2. Be sure not to write any of the code combinations which are described as "Setting prohibited" in above table.

Phase-out/Discontinued

Programmable wait control register

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	State after RESET	R/W
PWC	AW1	AW0	0	0	BW3	BW2	BW1	BW0	PWC7	PWC6	PWC5	PWC4	PWC3	PWC2	PWC1	PWC0	FFC6H	**Note**	R/W

PWC1	PWC0	Specifies number of clocks in memory (0000H - 3FFFH)			
		Wait cycle	Data access cycle	Fetch cycle mode	Fetch cycle
0	0	0	3	Normal fetch	3
0	1	1	4		4
1	0	2	5		5
1	1	0	3	High-speed fetch	2

PWC3	PWC2	Specifies number of clocks in memory (4000H - 7FFFH)			
		Wait cycle	Data access cycle	Fetch cycle mode	Fetch cycle
0	0	0	3	Normal fetch	3
0	1	1	4		4
1	0	2	5		5
1	1	0	3	High-speed fetch	2

PWC5	PWC4	Specifies number of clocks in memory (8000H - BFFFH)			
		Wait cycle	Data access cycle	Fetch cycle mode	Fetch cycle
0	0	0	3	Normal fetch	3
0	1	1	4		4
1	0	2	5		5
1	1	0	3	High-speed fetch	2

PWC7	PWC6	Specifies number of clocks in memory (C000H - F6FFH, FFD0H - FFDFH)			
		Wait cycle	Data access cycle	Fetch cycle mode	Fetch cycle
0	0	0	3	Normal fetch	3
0	1	1	4		4
1	0	2	5		5
1	1	0	3	High-speed fetch	2

BW0	Specifies external data bus width (valid address : 0000H - 3FFFH)
0	8- bit bus
1	16-bit bus

BW1	Specifies external data bus width (valid address : 4000H - 7FFFH)
0	8- bit bus
1	16-bit bus

BW2	Specifies external data bus width (valid address : 8000H - BFFFH)
0	8- bit bus
1	16-bit bus

BW3	Specifies external data bus width (valid address : C000H - F6FFH, FFD0H - FFDFH)
0	8- bit bus
1	16-bit bus

AW0	Controls address wait (valid address : 0000H - 7FFFH)
0	Address wait is not added
1	Address wait is added

AW1	Controls address wait (valid address : 8000H - F6FFH, FFD0H - FFDFH)
0	Address wait is not added
1	Address wait is added

Note The value at reset depends on the operation mode specified with the MODE0 and MODE1 pins. ★

MODE0	MODE1	μPD78355	μPD78356	μPD78P356	State after RESET
L	L	Setting prohibited	Single-chip mode		C0AAH
L	H	Setting prohibited			—
H	L	ROM-less mode (external 8-bit bus)		PROM mode	C0AAH
H	H	ROM-less mode (external 16-bit bus)			CFAAH