To our customers,

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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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TTL

Common Matter

1. Absolute Maximum Ratings

1.1 Table of Absolute Maximum Ratings

Item	Symbol	Diode input	Emitter input	Unit
Supply voltage	V_{CC} Note1	7	7	V
Input voltage	V_{IN}	7	5.5	V
Interemitter voltage	V_{BI} Note2	—	5.5	V
Power dissipation	PT	400	400	mW
Storage temperature range	Tstg	–65 to +150	–65 to +150	°C

Notes: 1. Voltage value, unless otherwise noted, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies between inputs that go directly into the same AND or NAND gate in the functional block diagram.

1.2 Output Voltage of Open Collector Outputs

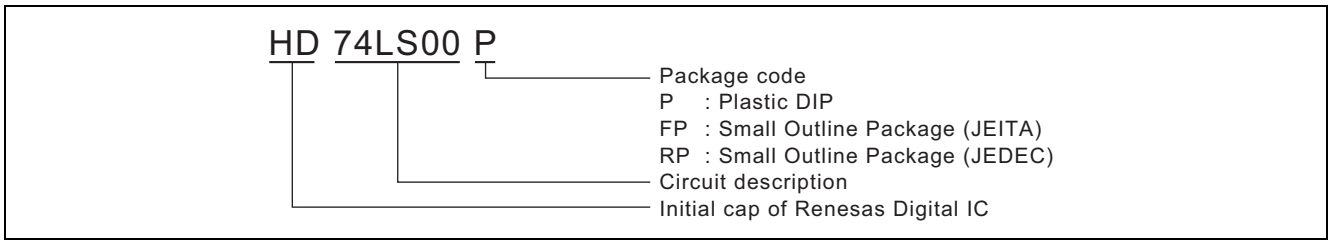
Item	Symbol	Rating	Unit	Applicable type No.
High level output voltage	$V_{O(OFF)}$	15	V	HD74LS26, HD74LS47, HD74LS145, HD74LS247
		30	V	HD74LS06. HD74LS07

1.3 Output Voltage of Three-state Outputs

Item	Symbol	Rating	Unit
High level output voltage	$V_{O(OFF)}$	5.5	V

2. Packaging Information

Factory orders for circuits described in this document should include a three-part type number as explained in the following example.



3. Recommended Operating Conditions

- Recommended Operating Conditions (1)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH} Note	—	—	–400	µA
	I_{OL}	—	—	8	mA
Operating temperature	Topr	–20	25	75	°C

Note: Totem-pole output only.

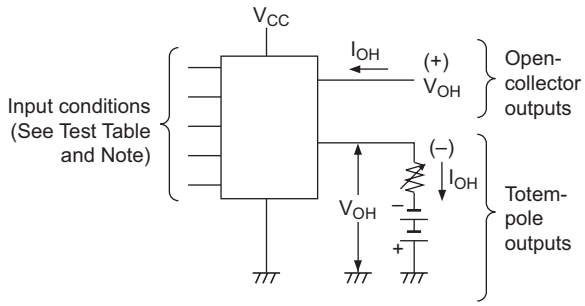
- Recommended Operating Conditions (2)

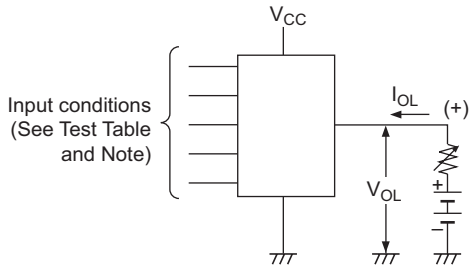
Item	Symbol	Applicable type	Value	Unit
High level output current	I_{OH} Note1	37, 40	–1.2	mA
		125A, 126A, 251, 253, 257, 258, 365A, 366A, 367A, 368A, 373, 374	–2.6	
		240, 241, 242, 243, 244, 245, 640, 641, 642, 645	–15	
Low level output current	I_{OL}	37, 38, 40, 47, 145, 125A, 126A, 240, 241, 242, 243, 244, 245, 247, 299, 365A, 366A, 367A, 368A, 373, 374, 640, 641, 642, 645	24	mA
Output voltage	$V_{O(off)}$ Note2	26, 47, 145, 247	15	V
		06, 07	30	V

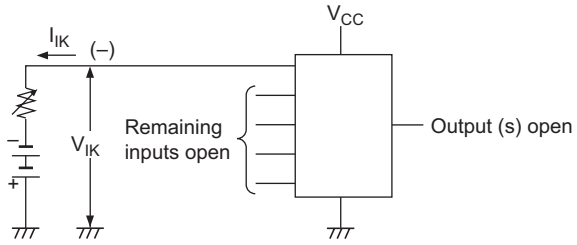
Notes: 1. Applied to totem-pole output.
2. Applied to open collector outputs at off-state.

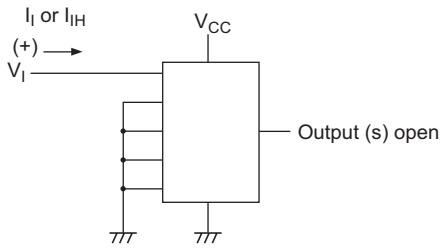
4. Testing Method of Electrical Characteristics

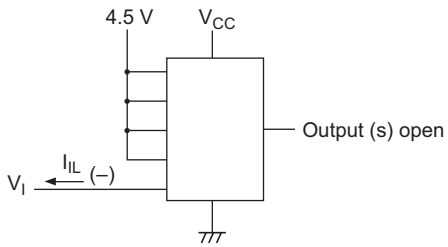
4.1 DC Characteristics

<table>
<tr><th>Item</th><th>Testing Method</th></tr>
<tr><td>V_{IH}
V_{IL}
V_{OH}
V_{OL}</td><td>


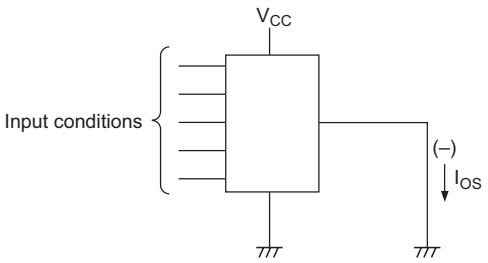
Test Table
<table>
<tr><th>Function</th><th>Input conditions</th></tr>
<tr><td>NAND</td><td>Input under test at $V_{IL\ max}$, all others at 4.5 V</td></tr>
<tr><td>AND</td><td>All inputs at $V_{IH\ min}$</td></tr>
<tr><td>NOR</td><td>All inputs at $V_{IL\ max}$</td></tr>
<tr><td>OR</td><td>Input under test at $V_{IH\ min}$, all others at GND</td></tr>
<tr><td>AND-OR-INVERT</td><td>Input under test (a set including one input of each AND gate) at $V_{IL\ max}$, all others at 4.5 V</td></tr>
<tr><td>AND-OR</td><td>All input of AND gate under test at $V_{IH\ min}$, all others at GND</td></tr>
</table>
Note: For functions having three-state outputs, input conditions should be preset to cause the outputs to be enabled (low-impedance).
</td></tr>
<tr><td>V_{IH}
V_{IL}
V_{OL}</td><td>


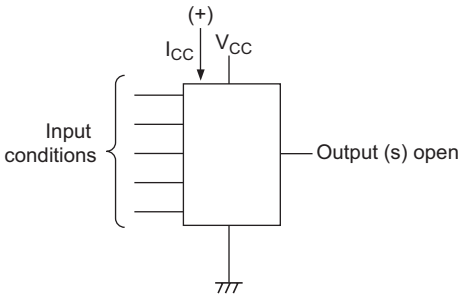
Test Table
<table>
<tr><th>Function</th><th>Input conditions</th></tr>
<tr><td>NAND</td><td>All inputs at $V_{IH\ min}$</td></tr>
<tr><td>AND</td><td>Input under test at $V_{IL\ max}$, all others at 4.5 V</td></tr>
<tr><td>NOR</td><td>Input under test at $V_{IH\ min}$, all others at GND</td></tr>
<tr><td>OR</td><td>All inputs $V_{IL\ max}$</td></tr>
<tr><td>AND-OR-INVERT</td><td>All input of AND gate under test at $V_{IH\ min}$, all others at GND</td></tr>
<tr><td>AND-OR</td><td>Input under test (a set including one input of each AND gate) at $V_{IL\ max}$, all others at 4.5 V</td></tr>
</table>
</td></tr>
<tr><td>V_{IK}</td><td>


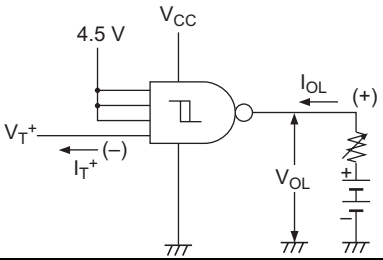
Note: Each input should be tested separately.
</td></tr>
<tr><td>I_I
I_{IH}</td><td>


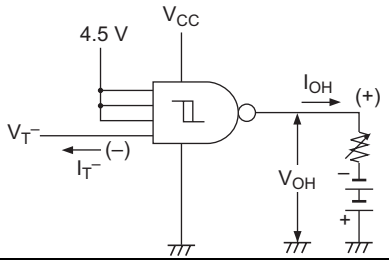
Notes: 1. Each input should be tested separately.
2. When testing AND-OR INVERT or AND-OR gates, the inputs of AND gates not under test should be open for I_I testing and be grounded for I_{IH} testing.
</td></tr>
<tr><td>I_{IL}</td><td>


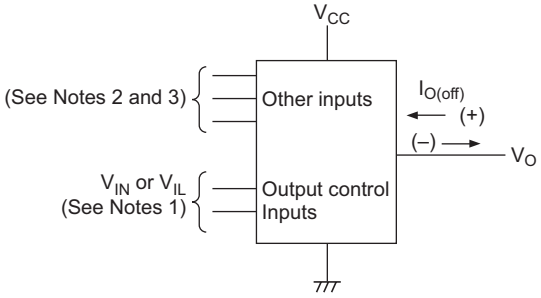
Notes: 1. Each input should be tested separately.
2. When testing AND-OR INVERT or AND-OR gates, the inputs of AND gates not under test should be open.
</td></tr>
</table>

<table>
<tr><th>Item</th><th>Testing Method</th></tr>
<tr><td>I_{OS}</td><td>


Test Table
<table>
<tr><th>Function</th><th>Input conditions</th></tr>
<tr><td>NAND</td><td>All inputs at GND</td></tr>
<tr><td>AND</td><td>All inputs at 4.5 V</td></tr>
<tr><td>NOR</td><td>All inputs at GND</td></tr>
<tr><td>OR</td><td>All inputs at 4.5 V</td></tr>
<tr><td>AND-OR-INVERT</td><td>All inputs at GND</td></tr>
<tr><td>AND-OR</td><td>All inputs at 4.5 V</td></tr>
</table>
Notes: 1. For functions having three-state outputs, input conditions should be preset to cause the outputs to be enabled (low-impedance).
2. Not more than one output should be shorted at a time.
</td></tr>
<tr><td>I_{CC}</td><td>


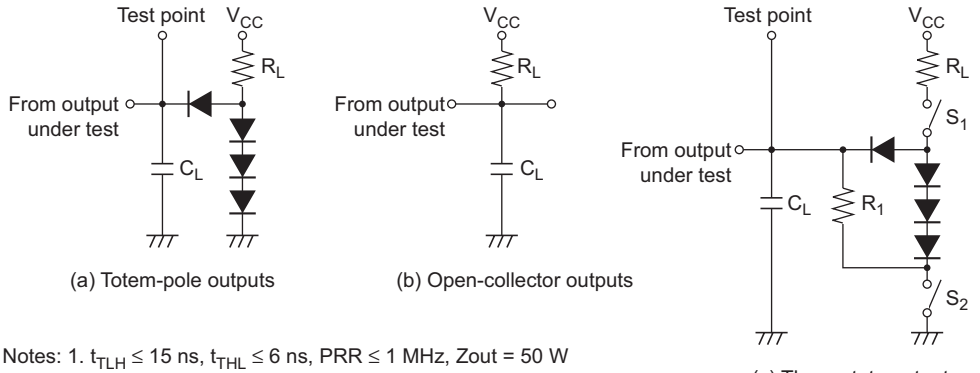
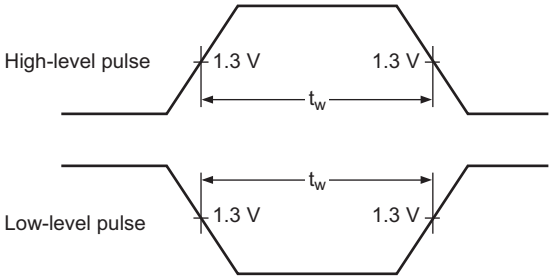
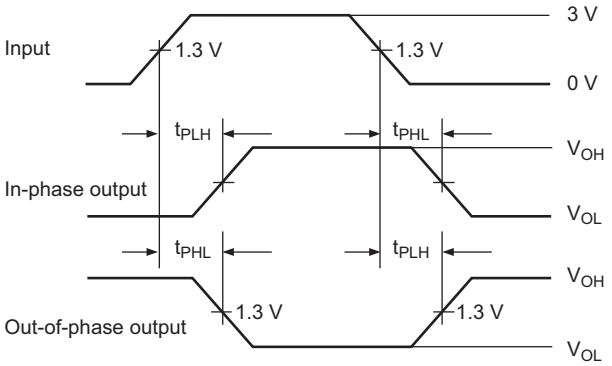
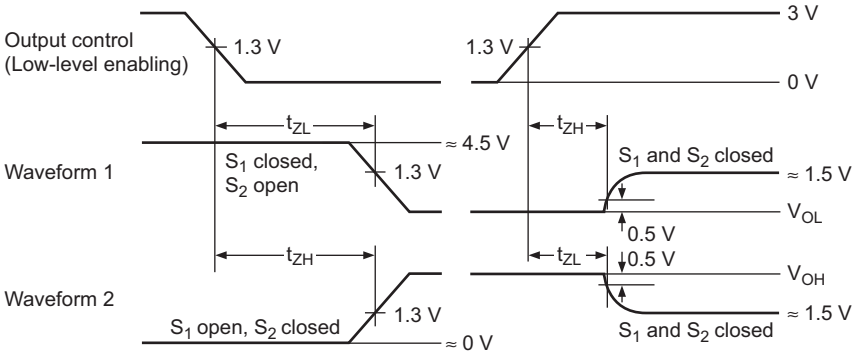
Test Table
<table>
<tr><th>Function</th><th colspan="2">Input conditions</th></tr>
<tr><td>NAND</td><td>All inputs at GND</td><td>All inputs at 4.5 V</td></tr>
<tr><td>AND</td><td>All inputs at 4.5 V</td><td>All inputs at GND</td></tr>
<tr><td>NOR</td><td>All inputs at GND</td><td>One input at 4.5 V
All others at GND</td></tr>
<tr><td>OR</td><td>One input at 4.5 V
All others at GND</td><td>All inputs at GND</td></tr>
<tr><td>AND-OR-INVERT</td><td>All inputs at GND</td><td>All inputs of one AND gate at 4.5 V
All others at GND</td></tr>
<tr><td>AND-OR</td><td>All inputs of one AND gate at 4.5 V
All others at GND</td><td>All inputs at GND</td></tr>
</table>
</td></tr>
<tr><td>V_T^+, I_T^+, V_{OL}</td><td>


</td></tr>
<tr><td>V_T^-, I_T^-, V_{OH}</td><td>


</td></tr>
<tr><td>I_{OZ} (Three-state output)</td><td>


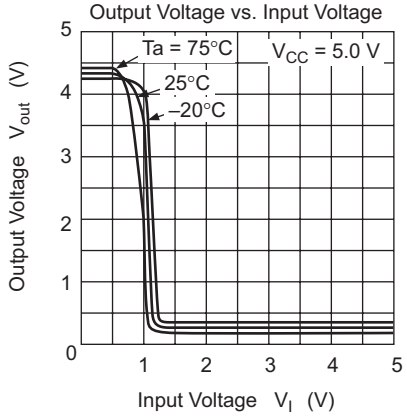
Notes: 1. Input conditions should be preset to ensure that the three-state output(s) is(are) disabled to cause the high-impedance state. See function table or logic for the particular device.
2. When testing with a H-level voltage applied to the output, input conditions should be preset to ensure that the output goes to L-level when enabled.
3. When testing with a L-level voltage applied to the output, input conditions should be preset to ensure that the output goes to H-level when enabled.
</td></tr>
</table>

4.2 DC Characteristics

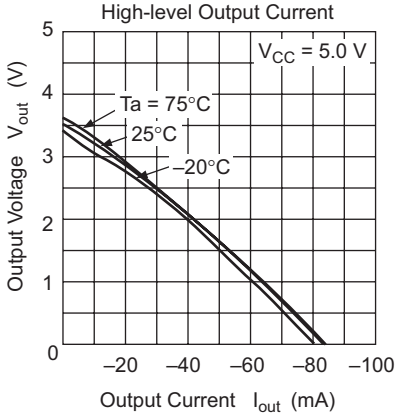
Item	Testing Method
Load circuits	 (a) Totem-pole outputs (b) Open-collector outputs (c) Three-state outputs Notes: 1. $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR ≤ 1 MHz, Zout = 50 W 2. CL includes probe and jig capacitance. 3. ALL diodes are 1S2074(H)
Voltage Waveforms	
Pulse width (t_w)	
Propa-gation delay times	 Note: When measuring propagation delay times of three-state outputs, switches S1 and S2 should be closed
Enable and disable times, three-state outputs	 Note: Waveform 1 shows an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 shows an output with internal conditions such that the output is high except when disabled by the output control.

5. Typical Characteristics

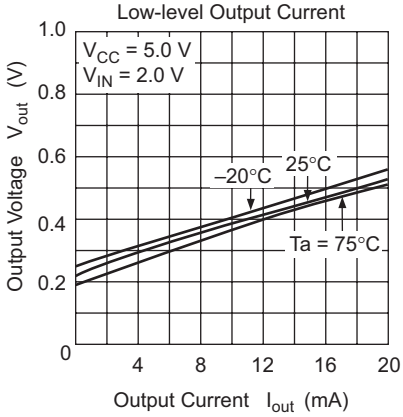
Output Voltage vs. Input Voltage



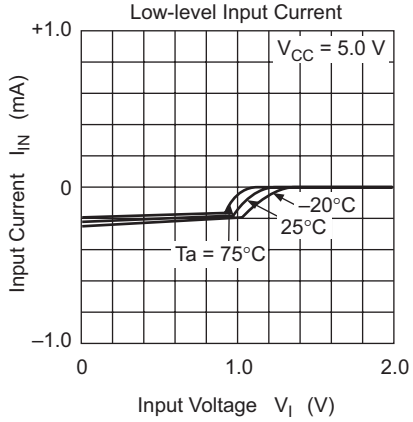
High-level Output Voltage vs. High-level Output Current



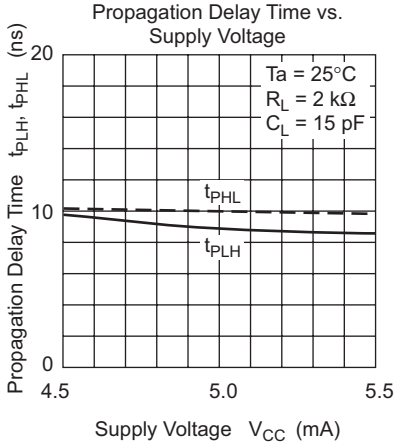
Low-level Output Voltage vs. Low-level Output Current



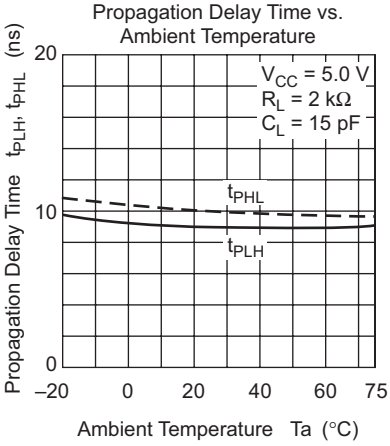
Low-level Input Voltage vs. Low-level Input Current



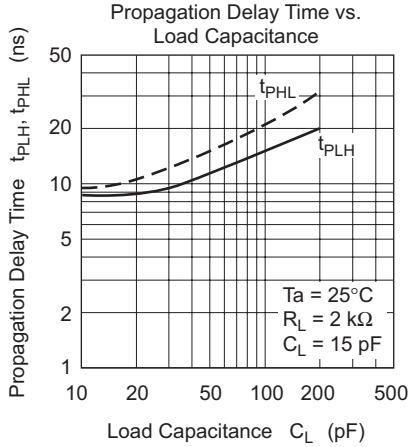
Propagation Delay Time vs. Supply Voltage



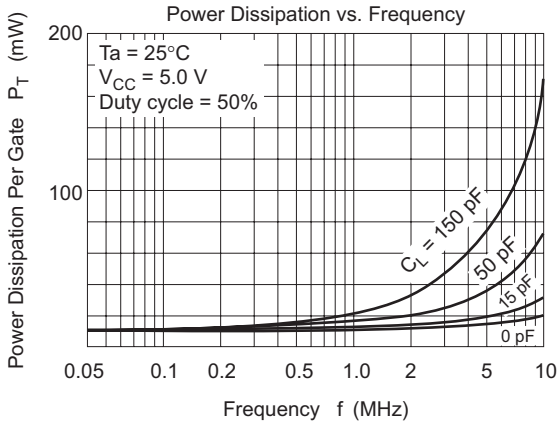
Propagation Delay Time vs. Ambient Temperature



Propagation Delay Time vs. Load Capacitance



Power Dissipation vs. Frequency



6. Precautions for Handling

6.1 Absolute Maximum Ratings

The Absolute maximum ratings of supply voltage (V_{CC}), input voltage (Vin), power dissipation (P_T), storage temperature (Tstg), etc. are defined. The limits should never be exceeded to avoid decrease of the operational margin, deterioration of characteristics, shorterning of life time and destruction of the devices.

6.2 Power Supply

6.2.1 Supply voltage

DC characteristics and functions are guaranteed for 5 V ±5% operation. This operating voltage range includes the ±5% supply tolerance. The DC fluctuation (fluctuation of primary power supply, load, temperature, etc.) and AC fluctuation (ripple, noise spike, etc.) which affect the supply voltage should be minimized and never exceed this tolerance limit.

6.2.2 Power Source Impedance

Lower power source impedance is recommended (for both AC and DC). The high power source impedance may generate a spike current or other noise problems. To avoid this, it is required to minimize the impedance by stabilizing the power supply and applying the low impedance V_{CC} and GND lines. It is also required to by-pass the spike current. Namely, on ever board, 0.01 to 0.1 µF decoupling capacitors with excellent high frequency characteristics should be used between V_{CC} and GND at least one of every 5 to 10 TTL devices.

6.3 Unused Input Pins

When making up a system with the TTL devices, unused input pins sometimes exist. These unused inputs should not be left floating because the input level at the open inputs is set just above the threshold level and it may be easily affected by noise. To obtain high performance and high reliability, the unused inputs of the AND or NAND gates should be connected to the point between V_{IHmin} and V_{INmax}. Several method of achieving this is shown below.

(a) Connect the unused inputs to V_{CC} through a resistor.
(b) Connect the unused inputs to the output of an unused NAND or invert gate whose input is grounded.
(c) Connect the unused inputs to the used terminal. In this case, there should be room in fan-out at logical “H” level.
(d) Connect the unused inputs to the power supply (V_{IHmin} to 5.5 V).

6.4 Input Logic Levels

To achieve high performance, the input logic levels should be established as designated. The required input levels of the TTL devices are V_{IH} = 2.0 V and V_{IL} = 0.8 V (specific values are shown in the data sheet of each device). These input logic levels should be maintained even in the worst conditions.

6.5 Input Waveform

On most of the TTL devices, oscillation is caused when the signal with the very slow rise or fall is supplied. The rise and fall times of TTL devices are recommended as;

Combinational Logic: less than 1 µs
Sequential Logic (Trigger gate): less than 150 ns
Others: less than 1 µs

When the input signal has very slowly rise or fall, re-shape its waveform by the schmitt circuit before supplying to a TTL device.

6.6 Output Short Circuit

The short circuit between the output terminals and the GND should be avoided because it may cause the heat-up or other unfavorable happening of the devices. However, if it is unavoidable, only one output short circuit period of HD74, HD74LS and HD74S is limited to 1 sec max.

6.7 Handling Precautions

(1) Thermal and humid stress should be minimized.
(2) The outer leads should not suffer from any mechanical stress such as cutting, forming, and stress force of the printed circuit board after mounting.
(3) To avoid the destruction of the devises by static electricity or surge voltages, humanbodies and tools should be grounded before coming in contact with the TTL devices. The destruction level against static electricity (the point of the accumulated defects becomes 50% of the total test samples under discharging from 200 pF capacitor) is:
Standard TTL devices: 400 V
Shottky TTL devices: 200 V
(4) When choosing the package types to be used (ceramic mold or plastic mold), please contact the engineer of our company.

7. Thermal Resistance of the Packages for TTL IC

The following table shows the thermal resistance of the packages for TTL IC's. It will contribute to the thermal design of the sets and the estimation of the fault rate of TTL devices.

7.1 Thermal Data of a Package

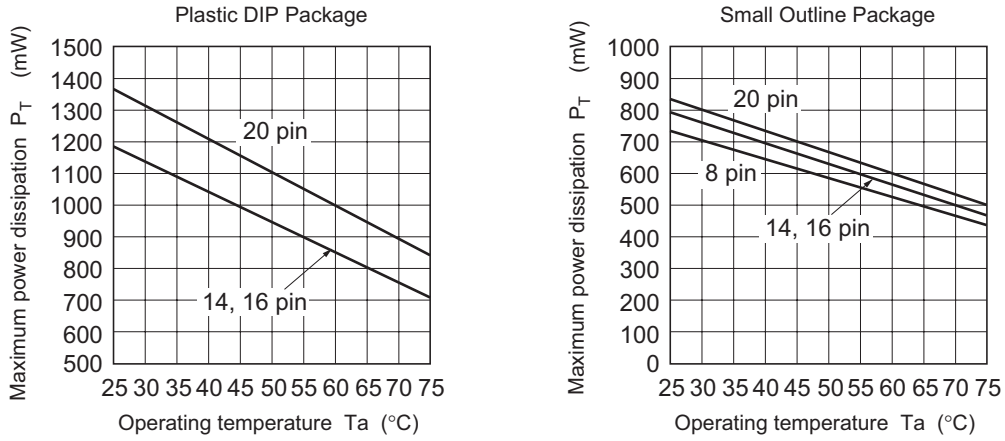
- Plastic DIP Package

Number of Pin	Thermal resistance θ_{j-a} (°C/W)	Derating factor (mW/°C)	Maximum power dissipation Ta = 25°C (mW)
14, 16	105	9.5	1185
20	90	11.0	1375

- Small Outline Package

Number of Pin	Thermal resistance θ_{j-a} (°C/W)	Derating factor (mW/°C)	Maximum power dissipation Ta = 25°C (mW)
8	170	5.9	735
14, 16	160	6.3	785
20	150	6.7	835

7.2 Derating Curve of TTL IC Package



Notes: 1. Testing method: V_{BE} method, airflow: 0 m/sec.
2. Mounting method: When a package is mounted on the glass epoxy board with wiring density of 10%.

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.09.04	—	First edition issued

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   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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