Tsi384™
Board Design Guidelines

80E1000_AN004_05

September 2009

Contents

About this Document

This section discusses the following topics:

Scope

The *Tsi384 Board Design Guidelines* provides hardware reference information for the Tsi384, such as layout guidelines and schematic review information. It is intended for hardware designers who are designing system interconnect applications with the Tsi384.

Document Conventions

This document uses the following conventions.

Non-differential Signal Notation

Non-differential signals are either active-low or active-high. An active-low signal has an active state of logic 0 (or the lower voltage level), and is denoted by a lowercase "n". An active-high signal has an active state of logic 1 (or the higher voltage level), and is not denoted by a special character. The following table illustrates the non-differential signal naming convention.

State	Single-line signal	Multi-line signal
Active low	NAMEn	NAMEn[3]
Active high	NAME	NAME[3]

Differential Signal Notation

Differential signals consist of pairs of complement positive and negative signals that are measured at the same time to determine a signal's active or inactive state (they are denoted by "_p" and "_n", respectively). The following table illustrates the differential signal naming convention.

State	Single-line signal	Multi-line signal
Inactive	NAME_p = 0 NAME_n = 1	NAME_p[3] = 0 NAME_n[3] =1
Active	NAME_p = 1 NAME_n = 0	NAME_p[3] is 1 NAME_n[3] is 0

Numeric Notation

- Hexadecimal numbers are denoted by the prefix *0x* (for example, 0x04).

- Binary numbers are denoted by the prefix *0b* (for example, 0b010).

- Registers that have multiple iterations are denoted by {x..y} in their names; where *x* is first register and address, and *y* is the last register and address. For example, REG{0..1} indicates there are two versions of the register at different addresses: REG0 and REG1.

Symbols

This symbol indicates a basic design concept or information considered helpful.

This symbol indicates important configuration information or suggestions.

This symbol indicates procedures or operating levels that may result in misuse or damage to the device.

Revision History

80E1000_AN004_05, Formal, September 2009

This document was rebranded as IDT. It does not include any technical changes.

80E1000_AN004_04, Formal, July 2008

- Changed a capacitor value for VDDA_PLL to 0.01uF from 0.1uF (see Figure 11)

- Added a new section that discusses "Lane and Polarity Reversal"

- Moved the schematic checklist content to the "Signal Descriptions" chapter of the *Tsi384 User Manual*

80E1000_AN004_03, Formal, December 2007

- Corrected the pull-up/pull-down description for the PWRUP_PLL_BYPASSn signal (see *Tsi384 User Manual*).

80E1000_AN004_02, Formal, September 2007

- Added filter circuit information for VDD_PCIE (see "VDD_PCIE")

- Simplified PCI bus routing guidelines (see "Bus Routing Rules")

80E1000_AN004_01, Formal, April 2007

This is the first version of the *Tsi384 Board Design Guidelines*.

1. Designing a Printed Circuit Board for PCIe Signals

Topics discussed include the following:

- "PCIe Signals"
- "Transmission Line Terms"
- "Trace Geometry"
- "Trace Length Matching"
- "Reference Planes"
- "Bends in PCIe Differential Pairs"
- "Device Breakout Area"
- "Vias in Differential Traces"
- "Routing Guidelines Summary"
- "PCIe Tx Capacitors"
- "PCIe_REFCLK"
- "Lane and Polarity Reversal"

> Dimensions in this chapter are given in British imperial units. Use this conversion ratio for Metric units:
>
> - 1 inch = 25.4 mm
> - 1 mil = 0.0254 mm

1.1 PCIe Signals

The following table lists the PCIe signals that are subject to the layout guidelines.

Table 1: Tsi384 PCIe Signals

Signal Name	Pin Number
PCIE_TXD_p0	R5
PCIE_TXD_n0	T5
PCIE_TXD_p1	R7
PCIE_TXD_n1	T7
PCIE_TXD_p2	R9

Table 1: Tsi384 PCIe Signals *(Continued)*

Signal Name	Pin Number
PCIE_TXD_n2	T9
PCIE_TXD_p3	R11
PCIE_TXD_n3	T11
PCIE_RXD_p0	N5
PCIE_RXD_n0	M5
PCIE_RXD_p1	N7
PCIE_RXD_n1	M7
PCIE_RXD_p2	N9
PCIE_RXD_n2	M9
PCIE_RXD_p3	N11
PCIE_RXD_n3	M11
PCIE_REFCLK_P	T3
PCIE_REFCLK_n	R3

1.2   Transmission Line Terms

- Microstrips – Traces that are adjacent to a continuous reference plane. In a PCB stackup, the microstrips are on the primary and secondary layers.

- Striplines – Traces routed in inner layers and have two reference planes. In a PCB stack-up, striplines are on internal layers.

1.3   Trace Geometry

The PCIe protocol uses differential pair routing, which requires greater care to meet the impedance targets on these signals versus other single-ended interfaces. Variations in the impedance of these signals will impact the overall jitter and loss within the system. The main areas of concern for board trace routing of PCIe data and clock signals include: spacing within the differential pair, coupling to an adjacent reference plane, and the thickness of the traces within the pair. Close coupling or relatively close physical spacing within the differential pairs, along with increased spacing to unrelated differential pairs and other signals, helps to minimize crosstalk and EMI effects.

The width and spacing guidelines of the PCIe differential signals determines the impedance of the traces and helps to insure that interconnect loss and jitter budgets are met. Signal integrity within the system is also impacted by whether or not appropriate spacing exists between differential pairs and adjacent traces.

Edge-coupled microstrip traces of each differential pair within the PCIe Interface should use a width of 5 mil with a 7-mil space within the pair. This 5/7/5 routing method provides the best compromise between impedance targets, loss impacts, crosstalk immunity, and routing flexibility. This trace geometry, however, will typically produce impedance results slightly lower than the 100Ω target. If stripline traces are used, they should maintain a 5/5/5 routing geometry with 5-mil trace widths combined with a 5-mil spacing within the pair.

A 20-mil edge-to-edge spacing should be used between traces of adjacent differential pairs in order to minimize negative crosstalk effects. A 20-mil spacing should also be maintained between differential pairs and non-PCIe signals. If unrelated signals have significantly higher voltage levels or edge rates when compared to PCIe, then a minimum 30-mil spacing should be used to avoid coupling issues.

Figure 1 provides a graphical representation of the width and spacing recommendations for PCIe differential pairs. It is recommended that the differential pairs be routed in a non-interleaved fashion – as displayed in the figure – which is known to minimize the affect of near-end crosstalk.

Figure 1: PCIe Board Trace Width and Spacings Example

PCIe Interleaved Microstrip Board Traces

PCIe Non-Interleaved Microstrip Board Traces

PCIe Stripline Board Traces
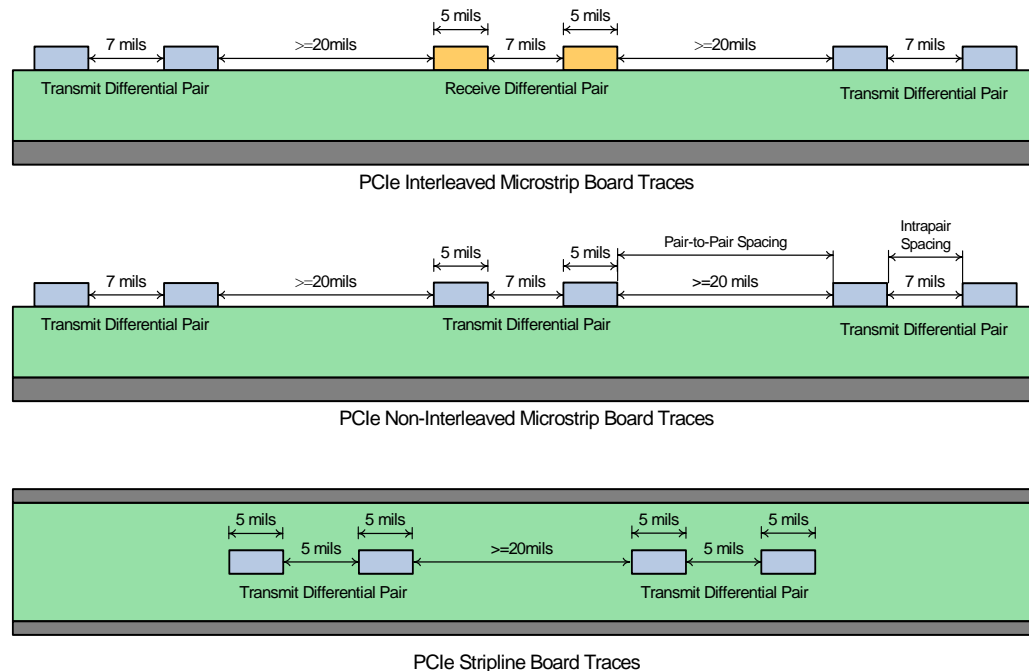
If board constraints require routing sections of a differential pair uncoupled where the intrapair spacing exceeds the 7-mil requirement, then the width of the uncoupled section of trace can be increased to 7 mil (see Figure 1). This applies to uncoupled sections that exceed 100 mil in distance. Using a 7-mil trace versus a 5-mil trace within the uncoupled sections helps to maintain the correct differential impedance across the uncoupled region.

1.4   Trace Length Matching

PCIe signals have constraints with respect to trace lengths and matching in order to meet jitter and loss budgets within a system. Each inch of board trace within a differential pair can add 1ps of jitter and up to 0.35dB of loss. Typically, the PCIe specification can be met with a chip-to-chip routing length up to 15 inches. When routing differential pairs connecting the finger connector pad to a Tsi384 pin on an add-in card, traces can be routed up to 3.5 inches.

Pair-to-pair length matching within the PCIe Interface is normally not required due to the large skew allowed at the receiver; however, it should be minimized in order to reduce the overall latency of the system. Intrapair skew is much more important and requires that the length of the traces within a differential pair be matched to within 5 mil of one another. Length matching within a differential pair should be performed on a segment-by-segment basis rather than only as an overall measurement.

## 1.5   Reference Planes

High quality reference planes within the PCIe Interface improve signal integrity, reduce EMI effects, and minimize AC common-mode noise within the differential pairs. It is recommended that the differential signal pairs reference the main ground plane within the PCB stackup, and reference only a single plane along the entire routing path. Differential traces should not be routed across or near any discontinuities in the reference plane. A 20-mil spacing should be maintained when routing near and parallel to the edge of a reference plane.

1.6   Bends in PCIe Differential Pairs

Bends or turns within the PCIe differential pairs should be kept to a minimum. The angles between traces should be greater than or equal to 135 degrees, and there should never be any 90 degree turns or bends along a trace. The inner spacing within a bend of a differential pair should equal or exceed the minimum pair-to-pair spacing of 20 mil in order to minimize the introduction of common-mode noise within the system (see Figure 1). Segments within a bend should have a length equal to or greater than 1.5x the width of the trace, and if possible the number of left- and right-hand bends should be matched as closely as possible to minimize length skew differences within a differential pair.

1.7   Device Breakout Area

Within the breakout areas of the Tsi384, the PCIe signal pairs should maximize the differential routing while minimizing any discontinuities or trace length skew. Length matching of the differential traces should occur as close as possible to the pad or pin while avoiding the addition of "tight" bends within the traces. The breakout areas should not exceed 250 mil in length for the PCIe Interface. Within the breakout areas, the trace routing guidelines of the differential pairs can be slightly relaxed (if absolutely necessary) to facilitate successful breakout of the signals. A width and spacing geometry of 5/5/5 can be used with a minimum spacing to other signals of 7 mil.

Figure 2: Tsi384 PCIe Differential Trace Breakout
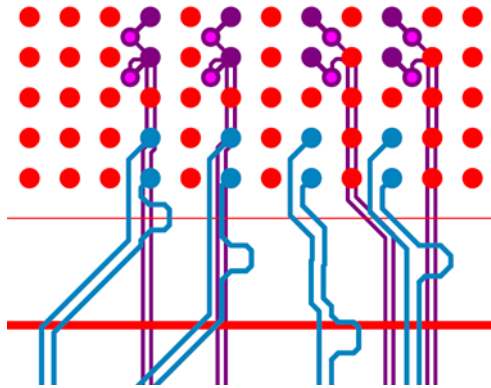
Blue traces are PCIe_TXD routed on the top layer.
Purple traces are PCIe_RXD routed on an inner layer.

1.8   Vias in Differential Traces

Use of vias within the differential traces of the PCIe signals can have an adverse effect on system performance. If vias must be used, they should have a pad size of less than 25 mil with a finished hole size of less than 14 mil. Vias should always be placed in pairs at the same relative location and should be symmetrical between the differential traces. A maximum of four via pairs can be used within each transmit differential pair of the PCIe link. Each receive differential pair can have a maximum of two vias along its path. A maximum of six via pairs are allowed along the entire PCIe interconnect path.

When traces change layers in a PCB, the reference plane for the differential traces also changes. It is recommended to introduce a stitching via close to the differential trace vias (see Figure 3). The stitching via connects all the ground planes together, and allows return current to flow easily from one ground plane to another.

Figure 3: Differential Pair Vias in PCIe Finger Connector

Stitching via
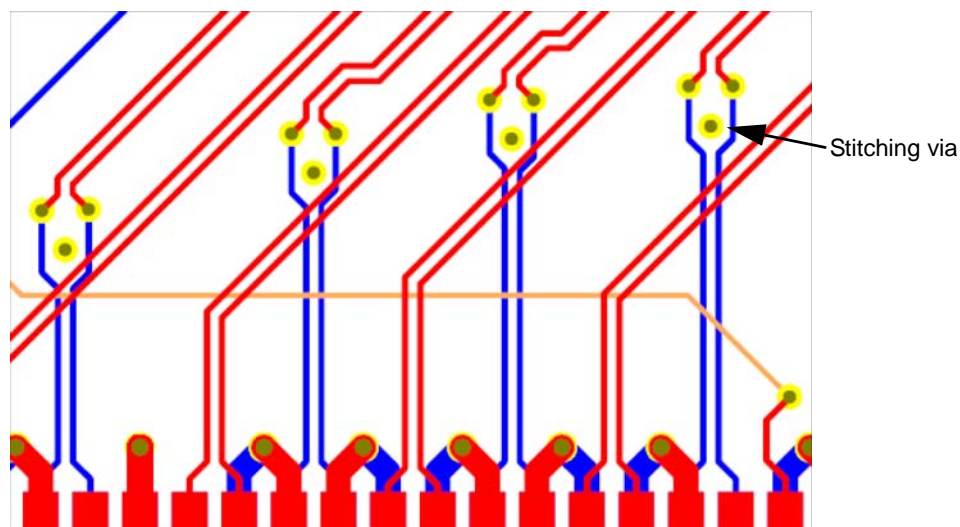
1.9   Routing Guidelines Summary

The routing guidelines should be used for board routing of the transmit and receive data. The guidelines are summarized in Table 2.

Table 2: PCIe Interface PCB Routing Guidelines

Parameter	Main Route System Board	Special Breakout Area
Differential Impedance Target	100 ohms $\pm$15 %	-
Single-ended Impedance Target	60 ohms $\pm$15 %	-
Trace Width	5 mil	7 mil if uncoupled length $\geq$ 100 mil
Differential Pair (within pair) Spacing	7 mil	5-mil spacing is acceptable
Pair-to-Pair Spacing	$\geq$ 20 mil	7-mil spacing is acceptable
Trace Length Restrictions	$\leq$ 15" chip-to-chip $\leq$ 3.5" chip-to-add-in card edge Connectors	Breakout is limited to $\leq$ 250 mil (included in overall trace length recommendations for main routes)
Length Matching within Pair	5 mil	-
Length Matching Pair-to-Pair	Keep moderate for latency. 1.25ns maximum lane-to-lane skew.	-
Reference Plane	GND plane recommended. Use stitching vias when changing layers. If a power plane is used as a reference plane, place decoupling capacitors close to the vias where the traces change layers.	GND islands on PWR layer are acceptable as long as the connection to the main ground planes is local.
Splits/Voids	No routing over splits or voids.	No more than half the trace width should be over via anti-pad.
Via Usage (maximum) (6 total, entire path)	Four vias per Tx trace. Two vias per Rx trace.	Acceptable to include one via in breakout area.
Bends	Match left and right turn bends where possible. No 90-degree or "tight" bends.	Avoid "tight" bends when routing in breakout area.

1.10   PCIe Tx Capacitors

The PCIe specification requires that each lane of the link is AC coupled between its corresponding transmitter and receiver. The AC coupling capacitors for the Tsi384 are discrete components located along each transmitter link on the PCB. These AC coupling capacitors allow the transmitter and receiver on a link to be biased at separate voltages. Table 3 summarizes the guidelines for implementing the PCIe AC coupling capacitors on a system board. Recommended capacitor layout and placement are provided in Figures 4 and 5.

Table 3: PCIe Interface AC Coupling Capacitor Guidelines

Parameter	Implementation Guideline
AC Coupling	AC coupling capacitors are required on the Tx pairs originating from the Tsi384.
Capacitor Value	$75nF \leq C_{AC\text{-}COUPLING} \leq 200nF$
Capacitor Tolerance	Specified minimum/maximum range must be met when capacitor tolerance is considered along with effects due to temperature and voltage.
Capacitor Type	Size 603 ceramic capacitors are acceptable, however, size 402 capacitors are strongly encouraged. The smaller the package size, the less ESL is introduced into the topology. The same package and capacitor size should be used for each signal in a differential pair. Do not use capacitor packs for PCIe AC coupling.
Capacitor Pad Size	To minimize parasitic impacts, pad sizes for each capacitor should be the minimum allowed per PCB manufacturer.
Capacitor Placement	AC coupling capacitors should be located at the same place within the differential pair. They should not be staggered in distance from one trace of the differential pair to the other. Capacitors should be placed as close to each other as possible to avoid creating large uncoupled sections within the differential pair traces. Relative location from one differential pair to another is not important.
Capacitor Location – Chip-to-Connector Routing	Capacitors should be placed such that they are not located in the center point of a trace route (for example, capacitors should be placed next to the connector or 1/3 the distance between the connector and the Tsi384).
Capacitor Location – Chip-to-Chip Routing	Capacitors should be located off-center within the interconnect (for example, placing the capacitors next to the Rx pins of one device is generally better than locating the capacitors in the midpoint of the interconnect).

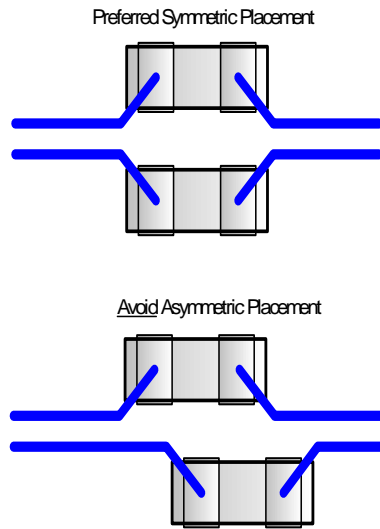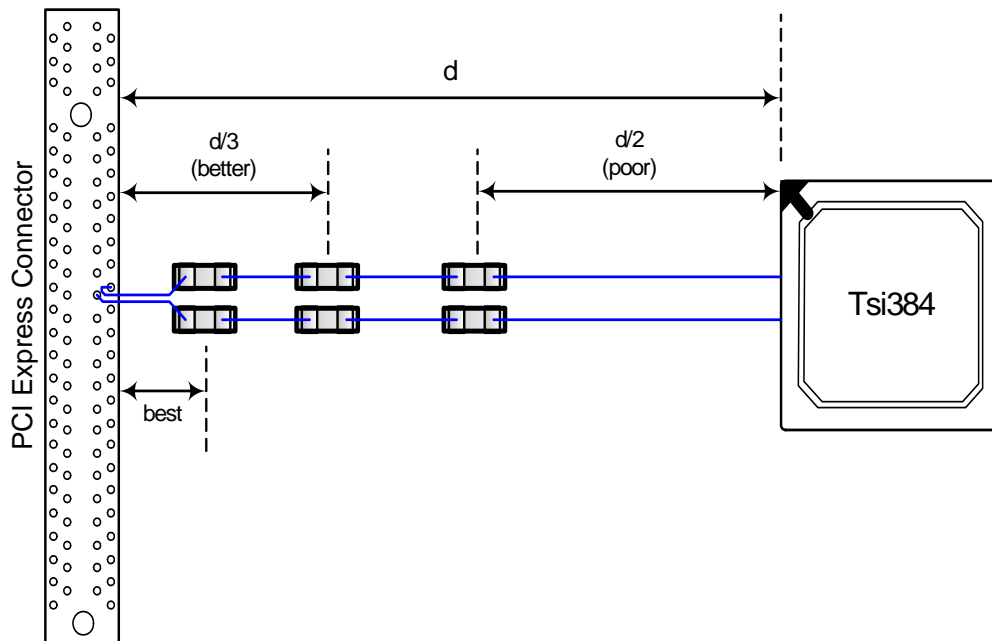**Figure 4: PCIe AC Coupling Capacitor Symmetric Layout**

Preferred Symmetric Placement

Avoid Asymmetric Placement

Figure 5: PCIe AC Coupling Capacitor Recommended Board Placement

PCI Express Connector

d

d/3
(better)

d/2
(poor)

best

Tsi384

1.11   PCIe_REFCLK

The Tsi384 must receive a 100-MHz differential reference clock on its PCIE_REFCLK_p/n input pins. This clock can be generated from an on-board oscillator if a PCIe system clock is not available. PCIE_REFCLK must be AC coupled with 0.1uF ceramic capacitors. The clock generator should provide an HCSL output-level clock that meets the PCIE_REFCLK duty cycle and jitter requirement, as specified in the *Tsi384 User Manual*. Figure 6 represents a simplified schematic of an HCSL PCIE_REFCLK circuit. The HCSL source termination is specified by the HCSL clock device vendor.
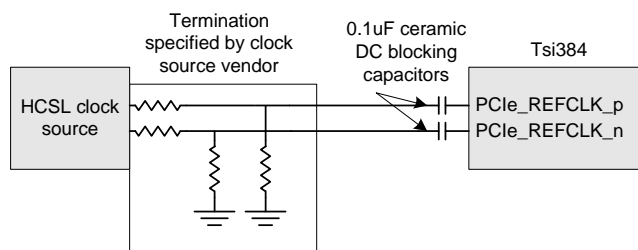
Figure 6: Simplified PCIE_REFCLK Circuit

Table 4: PCIE_REFCLK Layout Guidelines

Parameter	Implementation Guidelines
AC Coupling for System Board Reference Clock	AC coupling capacitors are required on the REFCLK differential pairs originating from the system board.
AC Coupling for On-board Clock Generator	The PCIE_REFCLK signal must have AC coupling capacitors between the clock source and the PCIE_REFCLK input pins.
Capacitor Value	0.1uF ceramic capacitors
Capacitor Placement	Both AC coupling capacitors should be located at the same place within the differential pair. They should not be staggered in distance from one trace of the differential pair to the other. Capacitors should be placed as close to each other as possible to avoid creating large uncoupled sections within the differential pair traces. The capacitor pair can be placed anywhere in the clock path.
PCIE_REFCLK Differential Trace Impedance	100 Ohms
PCIE_REFCLK Length Restriction for Add-in Card	From finger connector to Tsi384 (or any other device): 4 inches
Length Matching within Pair	≤ 10 mil

1.12　Lane and Polarity Reversal

If you are using lane reversal with the Tsi384 and lane degradation occurs, the device may end up in an unsupported or invalid lane configuration. When designing with lane reversal, you may want to consider the situation where lane degradation occurs, and whether or not your design will still function correctly based on the information in Table 5.

Table 5: Lane and Polarity Reversal

Configuration	Physical Lanes				Logical Lane Numbers			
	Lane 3	Lane 2	Lane 1	Lane 0	Lane 3	Lane 2	Lane 1	Lane 0
x4 Mode								
Normal	On	On	On	On	3	2	1	0
Lane Reversal	On	On	On	On	0	1	2	3
x2 Mode								
Normal	Off	Off	On	On	-	-	1	0
Lane Reversal	Off	Off	On	On	-	-	0	1
Normal	On	On	Off	Off	1	0	-	-
Lane Reversal	On	On	Off	Off	0	1	-	-
x1 Mode								
Normal	Off	Off	Off	On	-	-	-	0
Normal	Off	Off	On	Off	-	-	0	-
Normal	Off	On	Off	Off	-	0	-	-
Normal	On	Off	Off	Off	0	-	-	-

Polarity reversal is the process of inverting the polarity of the transmitter or receiver differential signals. For the Tsi384, polarity reversal is supported on a lane by lane basis, or by the transmitter or receiver alone.

2. Power Supply Filtering and Decoupling

Topics discussed include the following:

- "Analog Power Supply Filtering"
- "Decoupling Capacitors"

2.1 Analog Power Supply Filtering

2.1.1 VDDA_PCIE

The two VDDA_PCIE power pins are noise sensitive. Noise on these pins may translate into unwanted jitter on the serial bit streams. The VDDA_PCIE pin should be connected to a filtered 3.3V supply (for an example filter circuit, see Figure 7).

Based on the circuit in Figure 7, the VDDA_PCIE net can be implemented as a local plane located under the BGA. Ideally, the 0.1uF capacitors should be located under the BGA within the breakout vias. If this is not possible, the capacitors should be very close to the edge of the package. The net from the ferrite bead to the VDDA_PCIE pins can also be implemented as a trace from the ferrite bead to the VDDA_PCIE pin breakout via, as long as the decoupling capacitors are located under the BGA and connected to the breakout via with short traces (see Figure 8).
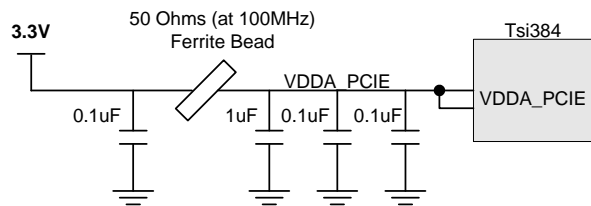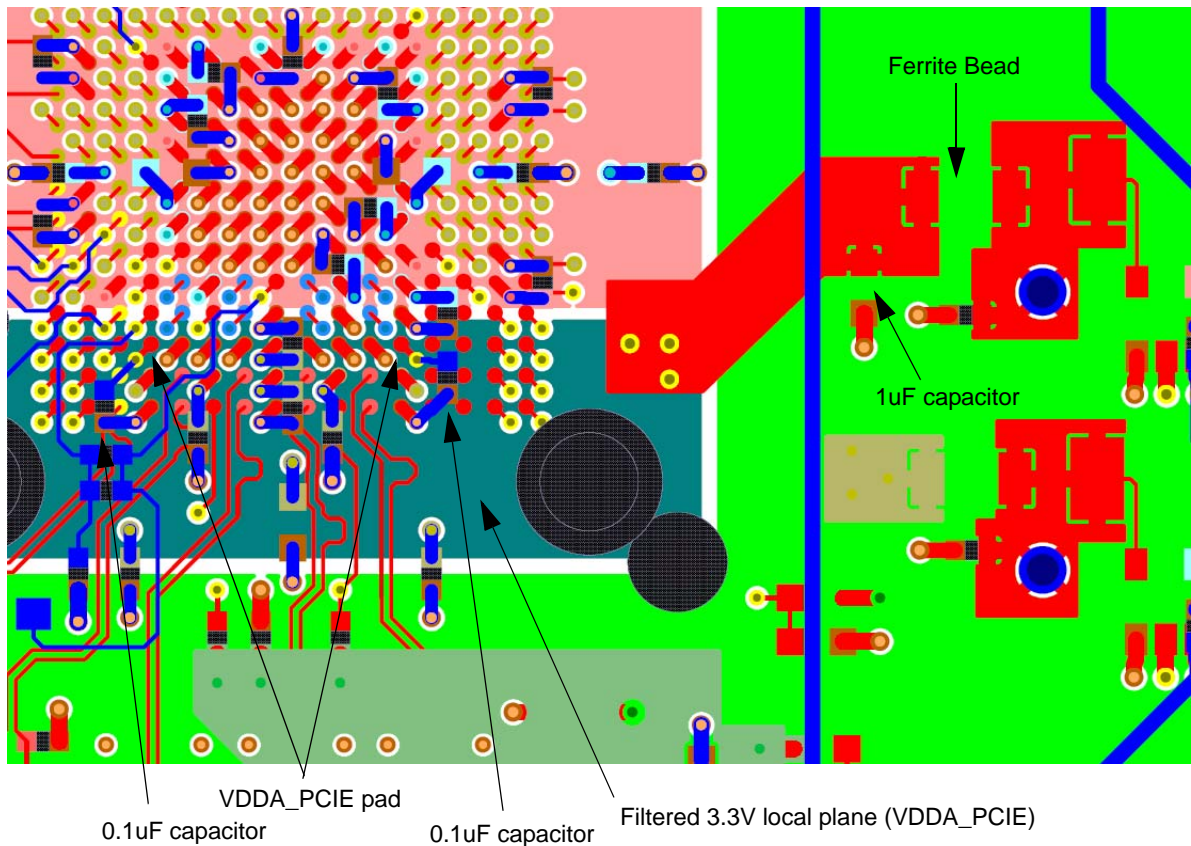
Figure 7: Supply Filter Circuit for VDDA_PCIE

Figure 8: VDDA_PCIE Filtered Plane Layout Example

Red: Top layer
Blue: Bottom layer
Turquoise: Filtered 3.3V plane on a power layer

2.1.2   VDD_PCIE

The VDD_PCIE power pins provide 1.2V to the Tsi384 SerDes circuit. The noise restriction on the VDD_PCIE pins is 50mV peak-to-peak. As displayed in Figure 9, a filter circuit can be used to reduce the noise from the main 1.2V supply. Ideally, the 0.1uF capacitors should be located under the BGA within the breakout vias. If this is not possible, the capacitors should be very close to the edge of the package. Preferably, the VDD_PCIE net is implemented as a local power plane under the BGA. Figure 10 shows VDD_PCIE decoupling capacitor placement (yellow pads) under the BGA.
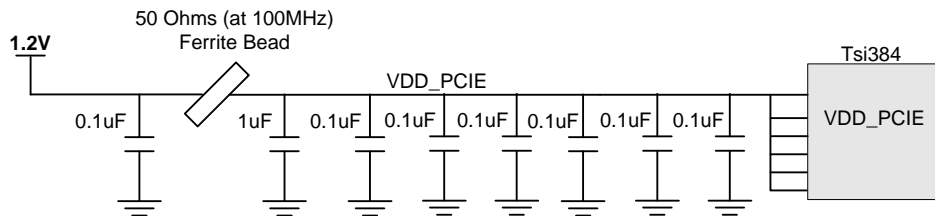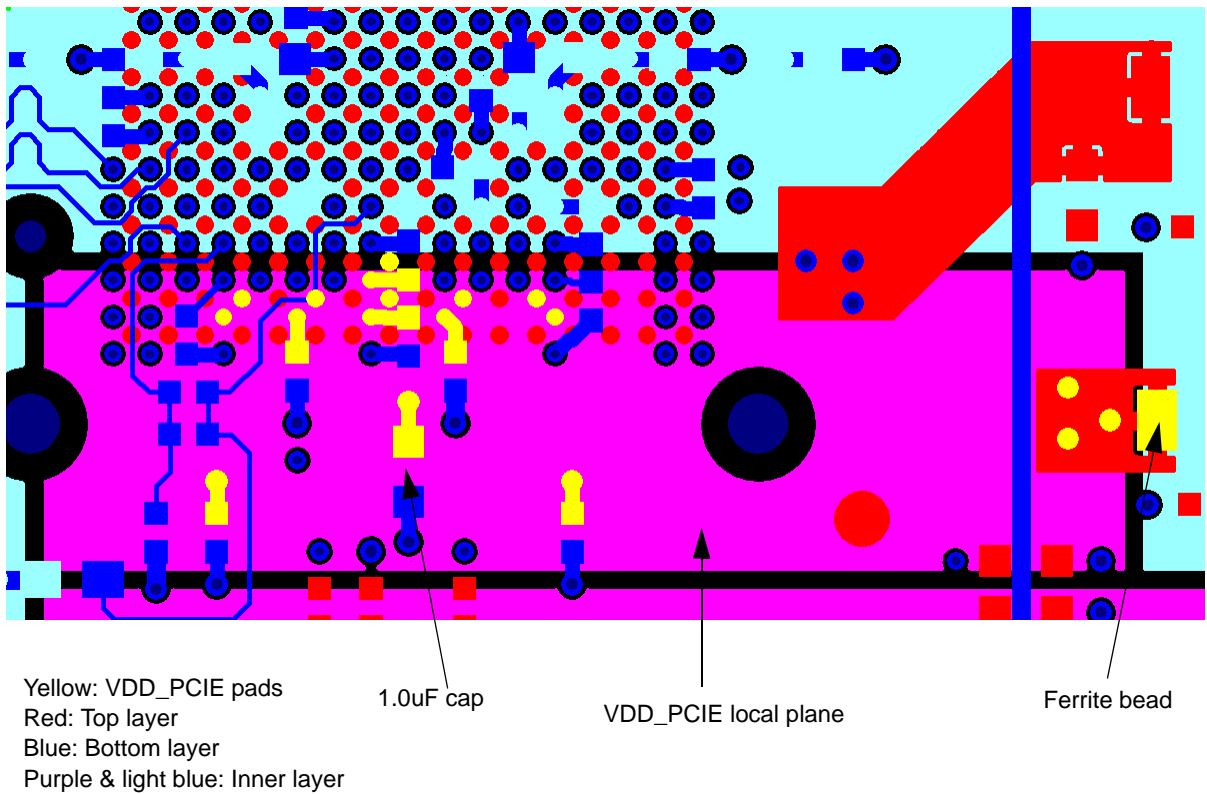
Figure 9: Supply Filter Circuit for VDD_PCIE

Figure 10: VDD_PCIE Filtered Plane Layout Example

Yellow: VDD_PCIE pads
Red: Top layer
Blue: Bottom layer
Purple & light blue: Inner layer

1.0uF cap

VDD_PCIE local plane

Ferrite bead

2.1.3   VDDA_PLL

The VDDA_PLL supply pin provides power to the internal clock PLL circuit inside the Tsi384. Use a filter circuit similar to the one in Figure 11. Place the 0.1uF and 0.01uF capacitors in the via breakout under the BGA.

**Figure 11: Supply Filter Circuit for VDDA_PLL**
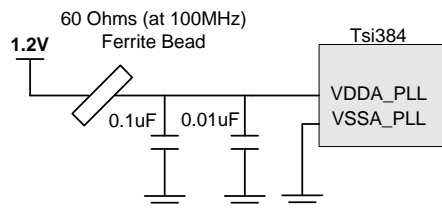
2.2   Decoupling Capacitors

The Tsi384 decoupling recommendation is provided in Table 6. Other components, including PCI connectors must also be adequately decoupled.

Table 6: Decoupling Capacitor Recommendations

Rail	Capacitor value	Quantity	Placement	Description
VDD	0.1uF	10	Ideally several are placed within the BGA breakout. Others are placed close to the BGA.	Ceramic (X5R or X7R) Surface mount Case size 0402 or 0603
VDD	1uF	2	Close to Tsi384	
VDD_PCI	0.1uF	7	Close to Tsi384	
VDD_PCI	1uF	1	Close to Tsi384	
VDD_PCIE	0.1uF	6	Ideally several are placed within the BGA breakout. Others are placed close to the BGA.	
VDD_PCIE	1uF	1	Close to Tsi384	

The layout example in Figure 12 shows one method for inserting decoupling capacitors within the BGA breakout. Not all decoupling capacitor from Table 6 are placed in the breakout. The remaining capacitors are located near the chip.

Figure 12: Top View of Bottom Layer, Decoupling Capacitors in Via Field
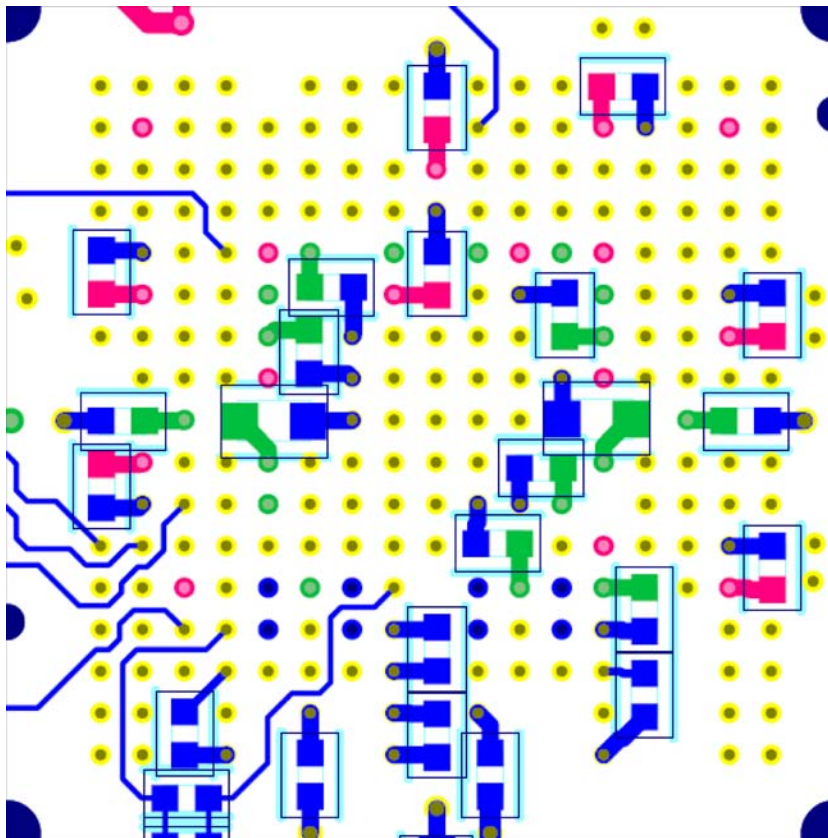
Red: VDD_PCI rail
Green: VDD rail
 Blue: Ground and other

3. PCI/X Bus Design Notes

Topics discussed include the following:

- "PCI-X Bus Loading"
- "PCI/X Clocking Modes"
- "Bus Routing Rules"

3.1 PCI-X Bus Loading

PCI-X's high switching frequency and tight setup and hold specification requirements impose restrictions on PCI-X bus design. At 133 MHz, the PCI-X timing specification cannot be met when the load on the bus signals is too high. Loading depends on the number of components attached to the PCI-X bus as well as the bus topology connecting to the devices. The loading information in Table 7 is based on general recommendations rather than detailed analysis. When exceeding the recommended load, a detailed timing analysis is recommended.

Table 7: PCI-X Bus Loading

PCI-X Clock Frequency	Number of Loads[a]
PCI-X 133 MHz	Two discrete devices or one connector (with a plug-in card)
PCI-X 66 MHz	Four discrete devices or two connectors (with plug-in cards)

a. A load corresponds to one PCI-X device or one connector.

3.1.1 IDSEL Resistor

Use a 2K-Ohm resistor between the PCI_AD line and the IDSEL pins of other PCI-X devices (ICs or connectors) when the bus is used in PCI-X mode only. Use a 1K-Ohm resistor when connecting to PCI devices (ICs or connectors) when the bus is used in both PCI and PCI-X modes. The Tsi384 will pre-drive the address lines to account for the longer setup time on the IDSEL input. Note that a lower resistor value is acceptable, but the load on the address lines connected to IDSEL inputs will be higher.

3.1.2 PCI_AD[32:63] Pull ups

As per the PCI specification, pull-up resistors are required on the PCI_AD[32:63] signals and the PCI_CBE[4:7] signals. A resistor value of 8.2K is recommended.

3.2 PCI/X Clocking Modes

The Tsi384 supports two clocking modes: Master and Slave. These clocking modes are discussed in the following sections.

3.2.1 PCI/X Slave Mode Clocking

Slave mode clocking requires an external PCI clock source (see Figure 13). The clock source must connect to the Tsi384 PCI_CLK, as well as to all other PCI devices on the same bus. Clock signal trace lengths should all be matched. The Tsi384 uses PCI_M66EN, PCI_PCIXCAP, and PCI_SEL100 to enable or disable internal clock compensation. It is important that these three signals reflect the proper clock rate. If they are used to define the external clock oscillator frequency, they should also be connected to the Tsi384. If the external clock frequency is set using other methods, PCI_M66EN should be set to 0 if the bus frequency is 33 MHz or less, and set to 1 if the bus frequency is above 33 MHz.

Table 8: Slave Mode Setup

Signal	Setting
PWRUP_CLK_MST	0
PWRUP_EXT_CLK_SEL	X
PCI_M66EN	0 = 33 MHz or less 1 = Above 33 MHz

Figure 13: Slave Mode Clocking
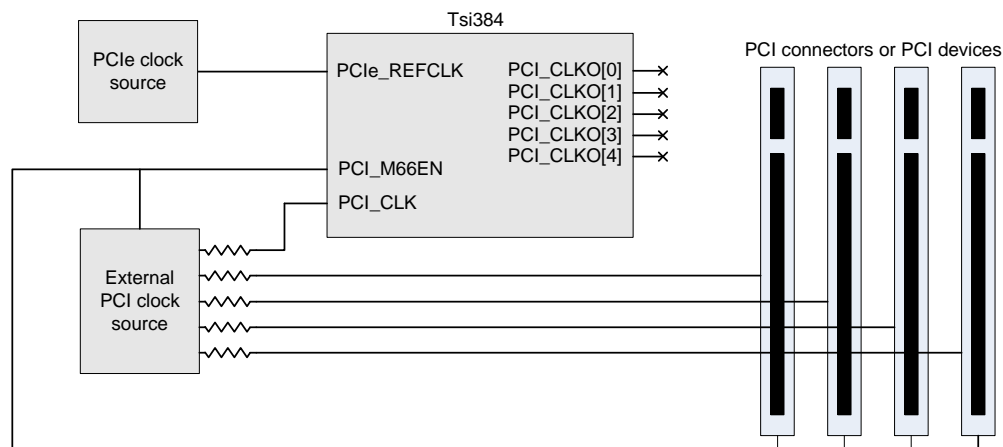
3.2.2 PCI/X Master Mode Clocking

Master mode clocking uses the PCIe input clock to generate the PCI clock outputs (see Figure 14). PCI_CLKO[4] should be connected to PCI_CLK for PCB trace and internal delay compensation. When the bus frequency is defined for 33-MHz operation, it is acceptable to ground PCI_IN and use PCI_CLKO[4] as a regular output. Clock compensation is not required at 33 MHz. In Master mode, it is important to set PCI_PCIXCAP, PCI_SEL100, and PCI_M66EN at the appropriate level because these signals are used to set the output clock frequency.

Table 9: Master Mode Setup

Signal	Setting
PWRUP_CLK_MST	1
PWRUP_EXT_CLK_SEL	1

Figure 14: Master Mode Clocking – PCI Clock for All Frequencies
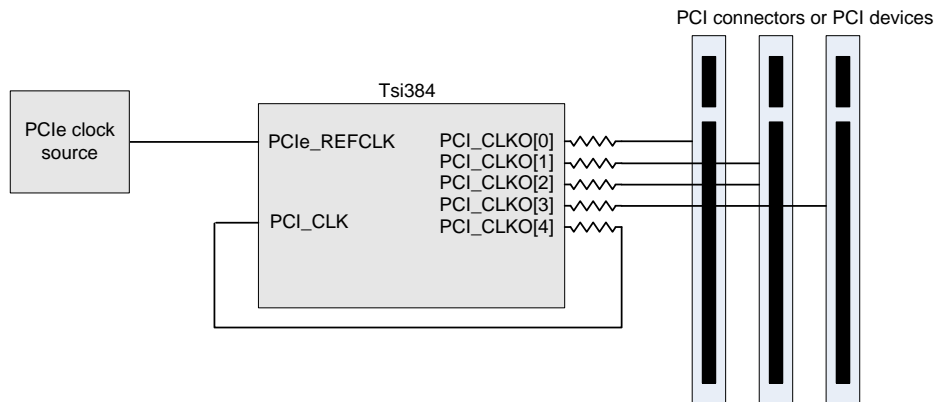
Table 10: Master Mode Setup when PCI Clock Frequency Never Exceeds 33 MHz

Signal	Setting
PWRUP_CLK_MST	1
PWRUP_EXT_CLK_SEL	0

Figure 15: Master Mode Clocking: PCI Clock Frequency Never Exceeds 33 MHz
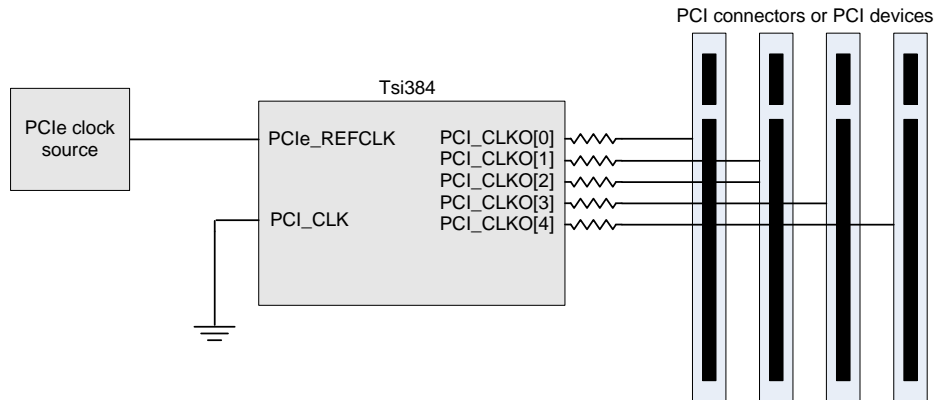
3.3   Bus Routing Rules

The PCB trace parameters outlined in Tables 11 and 12 are derived from the *PCI-X Specification's* System Timing Budget and the Tsi384's setup and hold timing parameters.

The clock traces should be matched in length. When all PCI devices see the clock rising edges at the same time, the PCI/X bus timing budget specifies the maximum propagation delay, T_{PROP}, for the PCI/X bus signals between all the devices. The propagation delay, however, must also include delays due to slow edge rates and other waveform distortions such as overshoots and undershoots. This propagation delay varies significantly depending on the bus topology, signaling level, and bus loading. The maximum skew recommendation provided in Table 11 is derived from about 50% of the maximum propagation time. This margin takes the other T_{PROP} factors into account. An accurate bus timing analysis requires board level bus topology simulation.
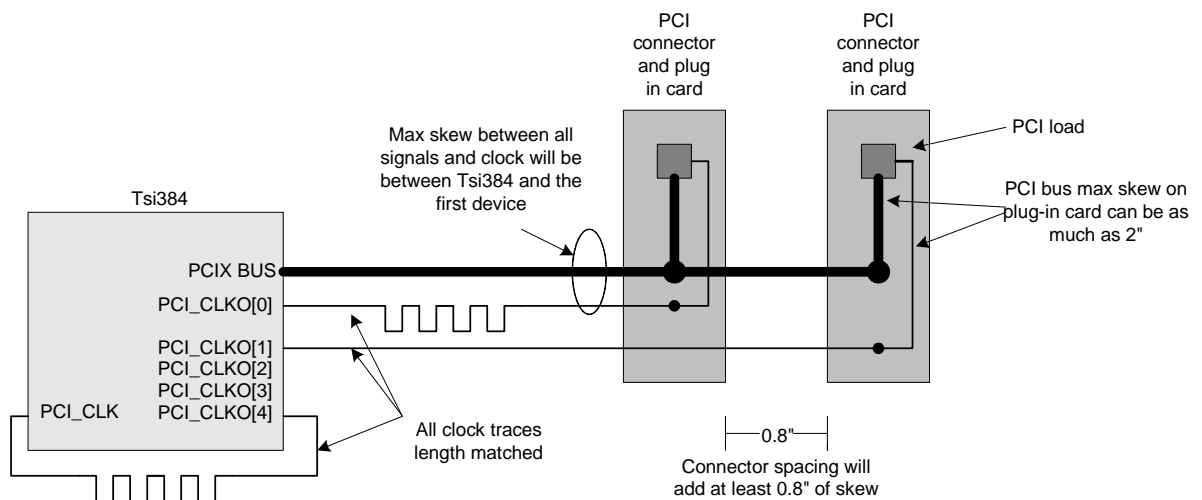
Table 11: PCI/X Propagation Delays

Bus Mode	Frequency	T_{PROP}	Propagation Length (190ps/inch)	Recommended Maximum Skew
PCI-X	133 MHz	2.0 ns	10.5"	3"
	66 MHz	9.0 ns	47.3"	20"
PCI	66 MHz	5 ns	26.3"	15"
	33 MHz	10 ns	57.9"	30"

Table 12: PCI/X Bus Routing Parameters

Parameter	Implementation Guideline
Maximum bus length	For 133-MHz operation: 11 inches from the Tsi384 to the last load on the bus, including connectors and plug-in card trace lengths.
Minimum bus length	For 133-MHz operation: 1.7 inch from the Tsi384 to the first load on the bus, including connectors and plug-in card trace lengths.
Trace impedance	60 Ohms +/- 15%
Skew within a PCI-X bus	Clocks and PCI_AD trace lengths should not be skewed by more than 3" for 133-MHz and 20" for 66-MHz PCI-X operation. When using connectors, the skew between connectors and the skew on plug-in cards, must be considered. On a plug-in card, the clock to PCI_AD skew can be as much as 2". This leaves a maximum of 1" skew from the Tsi384 to the connector. When two connectors are used, the space between the connectors reduces the maximum skew allowed. Skew for discrete devices: 3" Skew when using one connector: 1" Skew when using two connectors 0.8" apart: 200mils
Skew within a PCI bus	Clocks and PCI_AD trace lengths should not be skewed by more than 15" for 66-MHz PCI operation and 30" for 33MHz operation. When using connectors, the skew between connectors and the skew on plug-in cards, must be considered. On a plug in card, the clock to PCI_AD skew can be as much as 2".

Figure 16 summarizes the bus routing restrictions for a 66-MHz PCI-X bus with two plug-in connectors.

Figure 16: PCI/X Bus Topology With Two Connectors

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