Computing Power Reference Design Adaptation Guide

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Abstract

The goal of this design guide is to aid in rapidly prototyping a new design on an Intersil evaluation board using an existing reference design provided from an application engineer as a starting point. This procedure will give a solid first pass of a new design with additional fine tuning and output filter modification required once the end application board is laid out and tested. Use this guide for quickly checking the feasibility and performance of key parts (e.g., inductors, FETs, bulk caps, etc.) that may differ from those called out in reference designs against both Intel and Intersil specifications. This is by no means an exhaustive reference to designing with Intersil regulators; it is a stepping stone to getting a new design up and running before additional, more thorough, testing can be done.

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Assumptions

This guide assumes the following:

- An Intersil evaluation board is being used for testing
- The desired inductor, FETs and/or output capacitors have been chosen
- A reference design provided by Applications is being used as a starting point
- DCR sensing

Required Equipment

- Oscilloscope
- Digital multimeter
- Intel Gen 4 VRTT with appropriate interposer
- R-C substitution box
- V_{IN} and +5V power supplies
- Evaluation board documentation
- Part datasheet

Optional Equipment

- Differential oscilloscope probe for V_{OUT}
- Electronic load - more accurate for DC loads than VRTT
- Additional R-C substitution boxes - speed up the process by changing multiple components at once
- List of standard 1% resistor values

Design Procedure

1. Modify the evaluation board to configure it with the desired inductor(s), FETs and number of output bulk and ceramic capacitors.
   - Not all ceramic caps are created equal and capacitors from different vendors do not give the same performance. For quick design checks, leave the MLCCs used by Intersil on the board. For more thorough testing, populate the exact ones to be used in the end application.
2. Leave the compensation components used by the reference design in place. They should provide a good starting point for a reasonable range of output filters.
3. Calculate R_i using the formula below and solder connections from the R-C box to the appropriate resistor on the evaluation board. Dial the box to the 1% resistor value closest to the calculated result.

$$R_i = \frac{R_{ntcnet} \bullet DCR \bullet I_{CCmax}}{N \cdot \left(R_{ntcnet} + \frac{R_{sum}}{N}\right) \bullet I_{droopmax}} \quad \text{(EQ. 1)}$$

   - For single phase designs, set N = 1
   - If using the Intersil default design parameters:
     - R_{sum} = 3.65kΩ
     - R_{ntcnet} = 5.875kΩ (see datasheet for formulas if changing NTC network)
     - $I_{droopmax}$ = 48µA (This sets the OCP point 25% higher than I_{CCmax} as OCP trips when I_{droop} = 60µA.)
       - For low I_{CCmax} applications $I_{droopmax}$ might need to be decreased to allow for additional current when slewing V_{OUT}.
4. Using the VRTT, or electronic load, apply an appropriate DC load to the part that will not damage any components such as the FETs. Adjust R_i in 1% resistor value increments while monitoring the voltage at the IMON pin until it is as close as possible to the correct value. Use the formula below to find the IMON voltage for a given load current.
   - Typically R_{IMON} = 100kΩ and any further adjustments to this value can be made after the rest of the design is completed.

$$V_{IMON} = 1.2V\left(\frac{I_{LOAD}}{I_{CCmax}}\right) \quad \text{(EQ. 2)}$$

   Solder the final resistor value in place for R_i and move the R-C box to the R_{droop} resistor on the feedback resistor to dial in the DC load line.
5. Calculate R_{droop} using the following formula and dial the R-C box to the closest 1% value.

$$R_{droop} = \frac{I_{CCmax}}{I_{droopmax}} \bullet DC\_LL \quad \text{(EQ. 3)}$$

   - If using the Intersil default design parameters:
     - $I_{droopmax}$ = 48µA
6. Using a VRTT, load the part with a transient from 1A to I_{CCmax}, at a 300Hz rep rate, and monitor V_{OUT} on the scope. Set the time base on the scope so that one full cycle is visible. Position the cursors on the scope as shown in Figure 1 on page 3 and adjust R_{droop} in 1% increments until V_{droop} is dialed into spec.
   - A duty cycle of 50% or lower is recommended for the load transient.

$$V_{droop} = DC\_LL \bullet (I_{CCmax} - 1) \quad \text{(EQ. 4)}$$

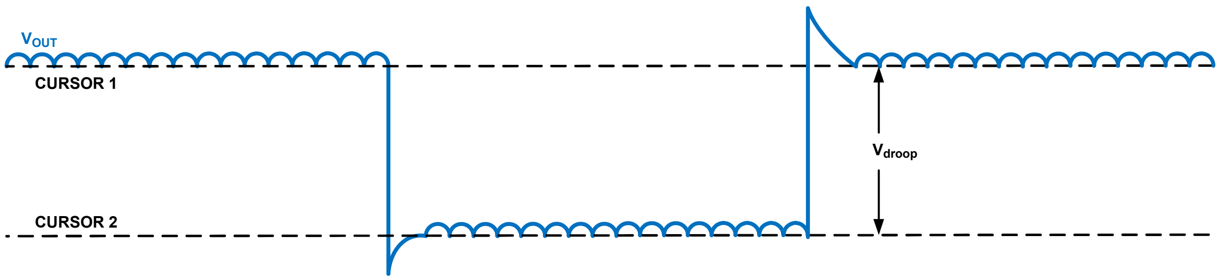

FIGURE 1. V_{DROOP} ADJUSTMENT

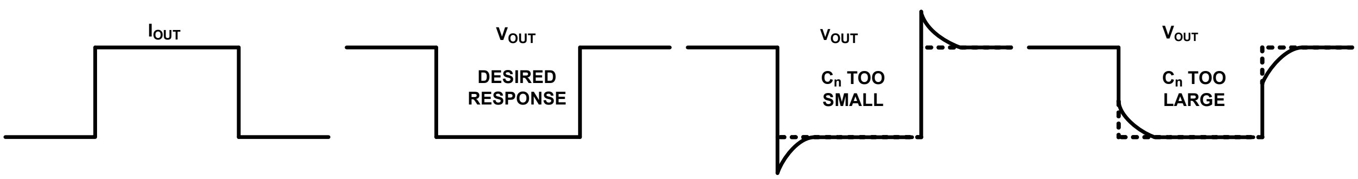

FIGURE 2. LOAD RESPONSE ADJUSTMENT

7. Solder the final resistor value in place for R_{droop} and move the R-C box to the C_n capacitor in the DCR network.
8. Calculate C_n and dial the R-C box to the closest standard capacitor value possible. If necessary, assume two capacitors in parallel when setting the substitution box.

$$C_n = \frac{L}{\left(\frac{R_{ntcnet} \bullet \frac{R_{sum}}{N}}{R_{netcnet} + \frac{R_{sum}}{N}}\right) \bullet DCR} \quad \text{(EQ. 5)}$$

- For single phase designs, set N = 1
- If using the Intersil default design parameters:
  - R_{sum} = 3.65kΩ
  - R_{ntcnet} = 5.875kΩ (see datasheet for formulas if changing NTC network)

9. Using a VRTT, load the part with a transient from 1A to I_{CCmax}, at a 300Hz rep rate, and monitor V_{OUT} on the scope. Set the time base on the scope so that one full cycle is visible. Adjust C_n in standard capacitor increments until V_{OUT} matches the desired response.
   - A duty cycle of 50% or lower is recommended for the load transient. (See Figure 2)
10. Solder down the final C_n capacitor value(s) and move the R-C box to the compensation components.
11. Using a VRTT, load the part with a transient from 1A to I_{CCmax}, at a 300Hz rep rate, and monitor V_{OUT} on the scope. Trigger on the falling edge of V_{OUT} and adjust the compensation components as needed to fine tune the transient response. (See Figure 3)
    - A duty cycle of 50% or lower is recommended for the load transient.

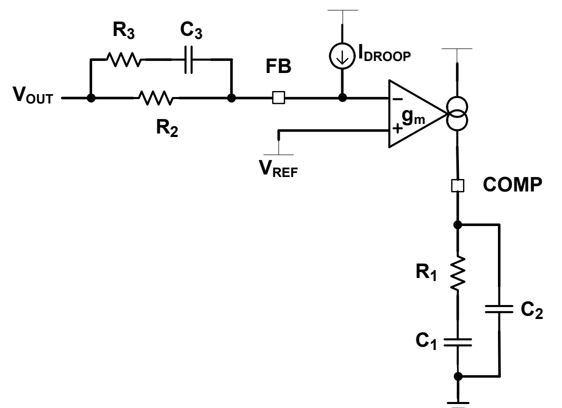

FIGURE 3. COMPENSATION ADJUSTMENT

- Compensation scheme assumes C_1 >> C_2 and R_2 >> R_3
- Make sure overall response is square through C_n adjustment in Step 9.
- R_3 and C_2 can be used to adjust the initial response to a load step (~2µs after insertion)
- C_3 can be used to adjust the response approximately 5 to 10µs after load step
- R_1 and C_1 can adjust the transient response >10µs after load step.

12. Sweep the load transient repetition rate up to 1MHz with the persistence feature of the scope turned on while checking if over and undershoot on V_{OUT} meet the required Intel specs. Adjust compensation and C_{OUT} as needed to pass.

13. Check the following parameters to ensure they are within spec and iterate through the design process as needed until all requirements are met.
    - CCM ripple at no load and full load
    - DCM ripple at 0A and light loads
    - DC load line
    - Transient response

The completed design can then be used as a starting point on the end application board and further modified as more thorough testing is completed. If assistance is required during the design process, contact an Intersil FAE or Applications Engineer.

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

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Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

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