

Packaging Information

Surface Mount Assembly Guidelines for Optical Co-Package Sensor and LED

TB489

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Introduction

Optical co-packages are developed for light sensor and proximity applications; they have an LED as well as a silicon chip in each device. The co-package mechanical structure is significantly different from a conventional DFN, with a hightemperature thermoplastic housing and light barrier, and an epoxy light-directing baffle. The cast molding compound is a transparent material rather than conventional black compound. Transparent molding compound allows transmission of ambient light and near-IR through the molding compound, to reach the proximity sensing target and return to the die sensor area. It also allows normal optical sensing for the Ambient Light Sensing feature. The package is lead-free, with a pre-plated Nickel-Palladium-Gold (NiPdAu) finish on the terminals (Figure 1). As Figure 1 shows, the package finish is transparent to allow light transmission, while at the same time protecting the device from the environment.

The package follows conventional DFN/QFN guidelines for PCB land pattern design and surface mount processing. Some additional recommendations are made to accommodate the special construction, which includes clear epoxy that has a lower glass transition temperature (Tg) and a higher coefficient of thermal expansion (CTE) compared to conventional molding compounds. This technical brief provides guidelines for assembly and handling during board mount process.

Board Mounting Guidelines

The package board mounting process is similar to that of conventional DFN/QFN packages; however, there are some key differences in the materials used. It is therefore recommended that users account for these differences in their application method. Specific guidelines in this technical brief are meant to accommodate for the differences in the materials. Only vacuum unit pickup with a soft rubber tip or a large flat area is recommended. Mechanical component grabbers (including manual tweezer handling) are not recommended.

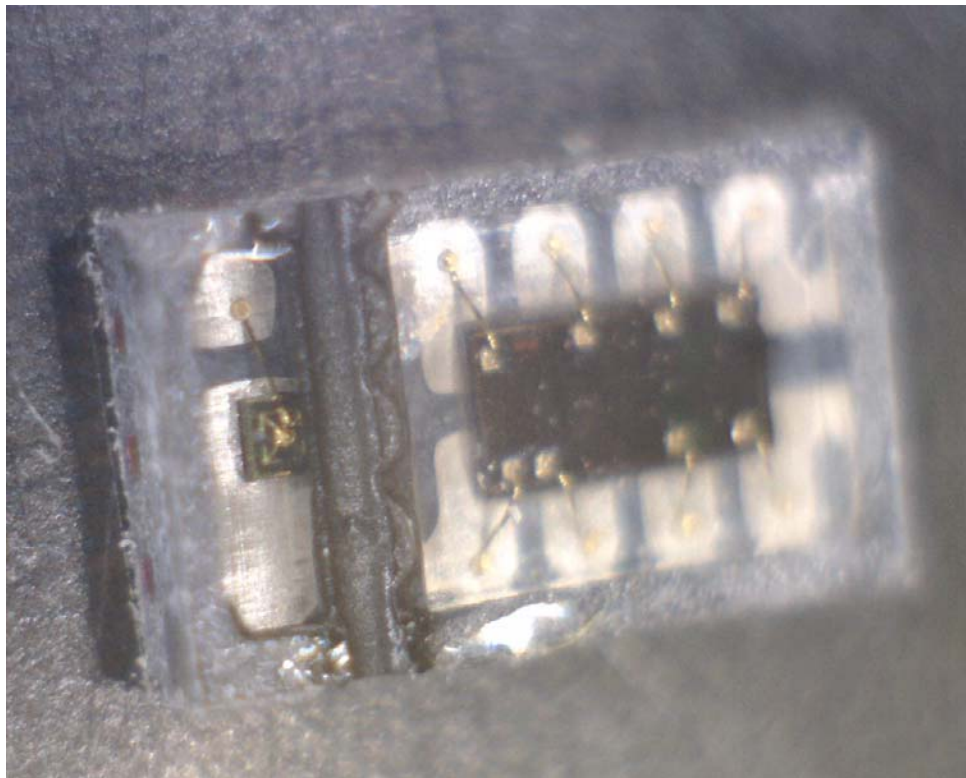


FIGURE 1.

Product Packing

Optical co-package products have been qualified under JEDEC J-STD-033B.1 MSL-3 test criteria and are generally shipped in tape and reel format. The packing quantity varies depending on the application and purchasing options. The moisture protection seal should not be broken until the board mounting process is ready. If the seal is broken, follow standard instructions for baking per JEDEC standard methods, but using the lower temperatures described in Moisture Sensitivity and Bake Conditions.

Package Construction

Optical co-packages have a nominal package thickness of 0.65mm. Figure 2 on page 2 shows a package outline drawing for the optical co-package with dimensions and tolerances. Because dimensions can change slightly with manufacturing process improvements, for board design, obtain the current package outline from the product data sheet. Although it is important to design PCB land patterns that correspond to the lead dimension (see PCB Land Pattern Design and product

outline drawing on data sheet), experimentation has shown that a PCB land that is up to 50% wider than the lead also gives successful soldering.

The co-package has an exposed paddle underneath the LED only as part of the package construction. As shown in Figure 2, the asymmetry of the exposed pad and leads indicates the Pin 1 location for the product. The exposed pad is part of the device circuitry and may be connected to the same potential as Pin 1. These are also connected internally to the device, so the solder pad on the circuit board does not have to be connected for electrical contact.

Optical co-packages are assembled on pre-plated copper leadframes, and individual units are singulated by a sawing process. The occasional presence of a slight oxide layer at the sawn surface (tip end) of the copper leads (on the side of the package) is not a concern for solder joint quality. Poor wetting to this exposed side edge does not affect solder joint quality or reliability, because the true solder joint is on the bottom of the package.

Package Outline Drawing

L10.2.1X3.5E

10 LEAD OPTICAL CO-PACKAGE

Rev 2, 1/12

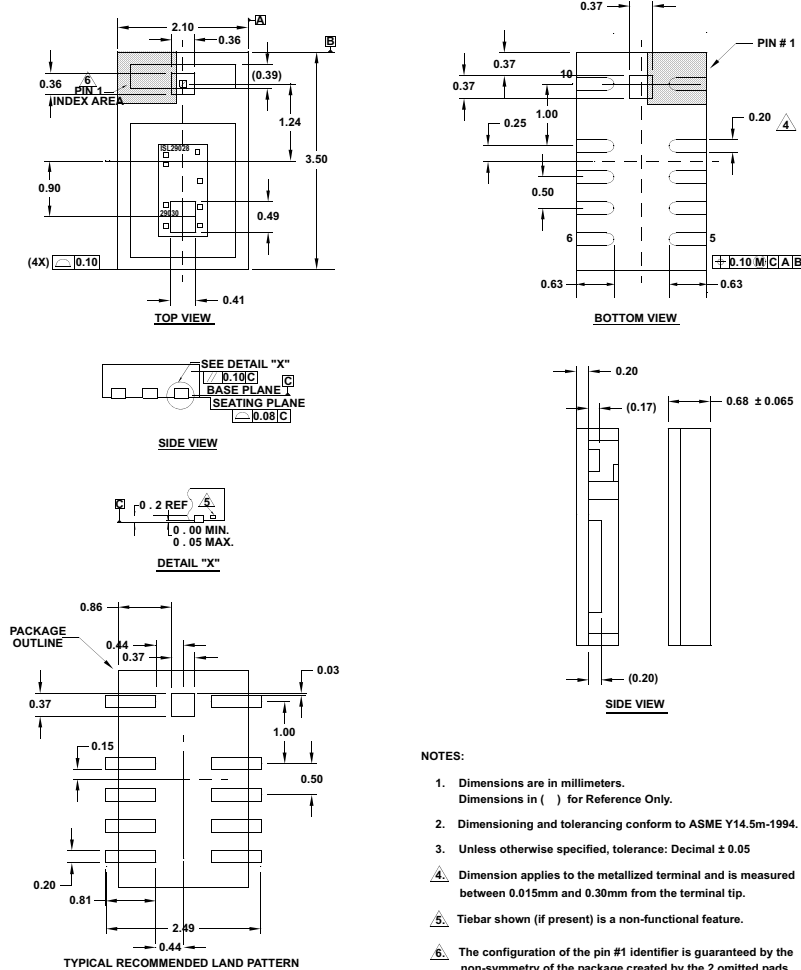


FIGURE 2.

PCB Land Pattern Design

Intersil Technical Brief 389

(<http://www.intersil.com/design/packages/#TechBriefs>) provides detailed information for PCB design and DFN and QFN packages, and is generally applicable to optical co-packages, with the exceptions listed in this technical brief. Additionally, package-specific land pattern information is available on package outline drawings, which are located at <http://www.intersil.com/design/packages/>. The package outline drawings are also included in product data sheets. An example of a land pattern recommendation is shown in Figure 2, below the package top view. The main features can be summarized as follows:

- 1:1 match with exposed pad area preferred. Larger solder pads on the circuit board can lead to bridging.
- 1:1 match with pin width (in this case, 0.2mm, but can be up to 50% wider)
- Land length for pin = pin length + 0.26mm (extending out from the package edge) allows some solder heat transfer, and test access to the device

Figure 3 shows a reference solder joint shape after package mounting on PCB. The solder joint under the exposed pad is intended to provide the package stand-off height and more robust assembly, but is not necessary.

The pad definition on the board is recommended to be nonsolder-mask-defined (NSMD), although solder-mask-defined (SMD) pads of the same effective wettable dimension are acceptable as well. A Nickel/Gold surface finish with 0.2µm maximum gold thicknesses on the circuit board is recommended for good solder wettability and shelf-life for the SMT process. OSP surface finish is also acceptable but requires appropriate controls on shelf life and exposure of the PCB to the environment. HASL or solder-plated finishes (pre-plated solder) should not be used for these products.

Solder Stencil

- A 0.100mm or 0.125mm thick stainless steel stencil is recommended.
- The stencil should be laser-cut followed by electropolish (chemical finishing not recommended). Alternatively, an additive build-up stencil may be used.
- Solder paste volume is a key contributor to solder joint reliability (higher solder volume leads to greater reliability). Solder volume must be controlled, however, because solder bridging may occur when solder paste is excessive.
- It is recommended that the exposed package pad be soldered to the corresponding landing pad on the PCB. Care should be taken to ensure there is no excessive solder under the exposed area. Excessive solder can cause open solder joints due to the excess stand-off it creates. The optimal value for solder paste in the center pad is 70% to 80% solder paste coverage on the exposed pad area.

Solder Paste

The package itself is lead-free and is compatible with both eutectic Tin/Lead or lead-free Tin/Silver/Copper solders. These packages have been qualified at a +260 °C maximum temperature reflow profile (3 cycles) for lead-free solder. Solder paste with “no-clean” flux and “Type 3” or “Type 4” solder particle size distribution is recommended.

Reflow Profile

Direct infrared (IR) heating of these packages must not be done as it can damage the part. Pure convection reflow of these parts is recommended. Typical reflow profiles per JEDEC J-STD-020 methods are recommended for the eutectic Sn/Pb and the leadfree Sn/Ag/Cu solders. Peak temperature for the Sn/Pb and Sn/Ag/Cu profile is *not to exceed* +260 °C. A recommended profile is described in Table 1. Due to the package construction, rework cannot be done without damaging the component. If rework is needed, replace the device with a fresh unit.

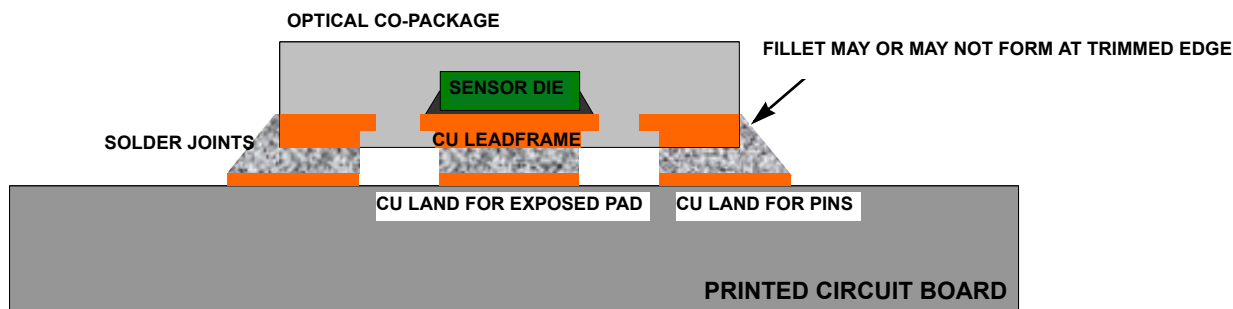


FIGURE 3.

Visual Inspection

Visual inspection of solder joints should be done to verify that there is no solder bridging between pads, and that the solder joint is “bright and shiny” (lead-free solder appears “dull” compared to Sn/Pb). The package should not be tilted or offcenter with respect to the PCB land pattern. A solder fillet at the edge of the package leads is not a requirement, and in fact, it may not form at all. Hand-solder touch-up is not recommended, as excess heat from the air nozzle or soldering iron can damage the component.

TABLE 1. SOLDER REFLOW PROFILE LIMITS

PARAMETER	LIMITS
Ramp +25 °C to +130 °C	+0.67 °C/s max
Ramp +130 °C to +170 °C	+0.44 °C/s min, 0.66 °C/s max
Dwell above +217 °C (tL)	40s min, 60s max
Peak temp	+260 °C max
Cooling ramp +217 °C to +150 °C	-4 °C max, -1 °C min

Optical Co-Package Specific Application Guidelines

The transparency requirement of Co-packaged products does not allow conventional filler loading as a means for controlling mechanical properties of the mold compound [such as coefficient of thermal expansion (CTE), modulus, or glass transition temperature (Tg)]. As such, the CTE of a clear epoxy is higher than that of a conventional black epoxy with fillers, and it has a lower modulus and a lower Tg. The Intersil device also has a second thermoplastic (LCP) black polymer, which forms a major portion of the housing and forms optical barriers around the emitter and detector structures. This material has glass-fiber reinforcement, but not a high modulus, and can be damaged with hard tools, such as tweezer tips or knife blades.

The following sections outline features of the optical co-package for proper application of the product.

Sensor Location and Optics Design

In general, the package body center does not always coincide with the center of the light sensor. The sensor location (a green and black checkerboard area on top part of IC) is also offset from the geometric center of the IC. The location of the sensor itself is specific to the product design in question, and therefore should be obtained from the product data sheet. Figure 2 shows an example of the sensor location description relative to the package body. In this example, the sensor area is 0.41mmx0.49mm and is offset from the center of the IC as well as the package. The application set-up should be designed to lead the light to the center of the sensor area and not to the center of the package. On the other hand, the sensor surface height is always located at 0.27 ±0.10mm below the top surface of the package. Solder joint and package height (0.65mm nom) should also be considered in calculating the sensor surface height from the PCB top surface.

Moisture Sensitivity and Bake Conditions

Optical co-packages have been qualified at JEDEC moisture sensitivity levels of MSL3 for +260 °C solder reflow profiles. The properties of clear mold compound are such that moisture saturation occurs rapidly. Therefore, it is

important to control the exposure time once the moisture protection seal is broken. It is recommended that these components be baked according to the moisture sensitivity level labeling on the reel if the exposure time exceeds the recommended level on the label prior to board mounting.

The recommended baking condition is +100 °C for 24 hours for loose parts. A bake temperature higher than +105 °C can result in discoloration of the clear molding compound. Baking in tape is not recommended, because the tape and cover tape cannot handle temperatures over +40 °C for extended times.

Pick-and-Place with Clear Packages

These optical packages are fully compatible with visionbased placement machines. These packages are not recommended to be placed with mechanical centering placement machines or chip-shooters. Placement with tweezers is also not recommended.

Rework and Associated Risks

Optical co-package products can be reworked using a reflow profile that closely matches the production reflow profile described previously. The packages should not be exposed to >260 °C during rework operation. Do not reuse the same product upon removal from the PCB. Fresh replacement units should be used. Excessive heating of clear mold compound can result in change in color of the mold compound (yellowing) and can also compromise wire bond integrity due to the high coefficient of thermal expansion of the mold compound material.

Marking, Visual Criteria, and Traceability

Optical products cannot be marked on the top side of the package because of the need for unobstructed transparency. On the bottom of the package, there is a 4-letter-code laser marking that can be used to trace the lot and part details. In addition, when viewing from the top and bottom, the package is decidedly not symmetrical, so pin 1 location is obvious. Visual discoloration of the clear epoxy in the LED die cavity is not unusual, and it does not affect the IR emission. Care must be exercised to prevent scratching or damage above the detector region of the IC, which can alter optical measurement performance.

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