Using the ISL6269 and ISL6269A for 5V VOUT Applications

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Description

This document specifies the requirements for the extended output voltage regulation range of the ISL6269 and ISL6269A Single-Phase Synchronous-Buck PWM controllers. The application space specified within the ISL6269 and ISL6269A datasheets is +7.0V to +25.0V input voltage and +0.6V to +3.3V output voltage. The application space may be amended to accommodate an output voltage of 5V when the requirements of this document are followed.

Requirements

- The input voltage of the converter must be between +12.0V to +25.0V.
- The FCCM pin must be connected to the VCC pin, forcing the converter into continuous conduction mode. If allowed into discontinuous conduction mode at low load, the bootstrap capacitor voltage could discharge to 0V during the time interval between PWM pulses.
- A 499Ω resistor R_{MS} is placed in series with the VO pin to protect the internal ESD diode that is connected to V_{CC}. The ESD diode will conduct current into the V_{CC} node in the unlikely event where the tolerance stack up of V_{CC}, V_{FB}, I_{FB}, V_{OVR}, R_{TOP}, and R_{BOTTOM} results in a voltage sufficient to forward bias the device. Refer to Figure 5.

V_{COMP} and Duty Cycle

A window voltage V_W is referenced with respect to the error amplifier output voltage V_{COMP}, creating an envelope into which the ripple voltage V_R across ripple capacitor C_R is compared. Figure 1 shows PWM pulses being generated as V_R traverses the V_W and V_{COMP} thresholds.

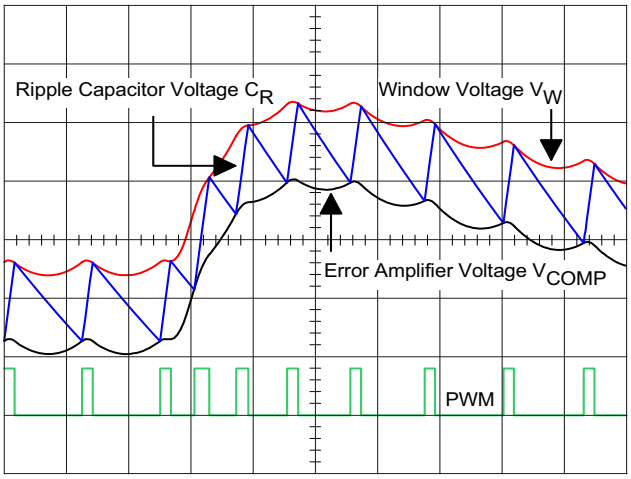

FIGURE 1. MODULATOR LOAD TRANSIENT WAVEFORMS

The static V_{COMP} voltage increases as V_{OUT}, I_{LOAD}, and duty cycle increases. The duty cycle increases as V_{IN} decreases or in response to a load transient. As the slew rate of the transient becomes faster, the ΔV_{COMP} becomes larger. A minimum V_{IN} of 12V has been established so that V_{COMP} does not hit an internal 3.20V clamp in applications where V_{OUT} is programmed to 5V. The voltage clamp ensures that there will be sufficient head room above V_{COMP} so that the window voltage V_W, which can be as large as 900mV, does not saturate at the minimum specified V_{CC} input bias voltage of 4.75V. A graphical representation of the V_{COMP} range is found in Figure 4. The waveforms in Figure 2 show the transient response of the 5V converter at 7V V_{IN} and a transient load of 1Ω. Notice that the duty cycle goes to 100%, V_{OUT} starts falling, and V_{COMP} hits the 3.20V clamp.

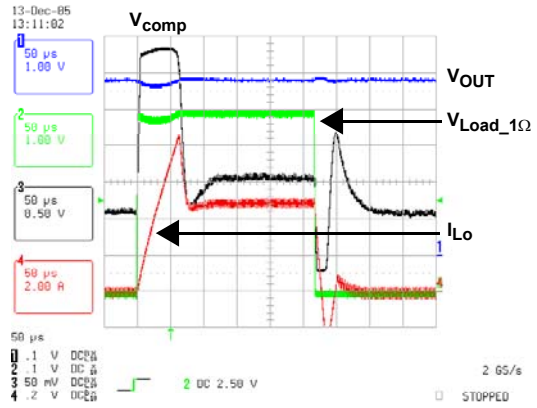

FIGURE 2. TRANSIENT RESPONSE AT 7V V_{IN}

The waveforms in Figure 3 show the transient response of the 5V converter at 15V V_{IN} and a transient load of 1Ω. Notice that V_{OUT} stays well regulated and V_{COMP} avoids the 3.20V clamp.

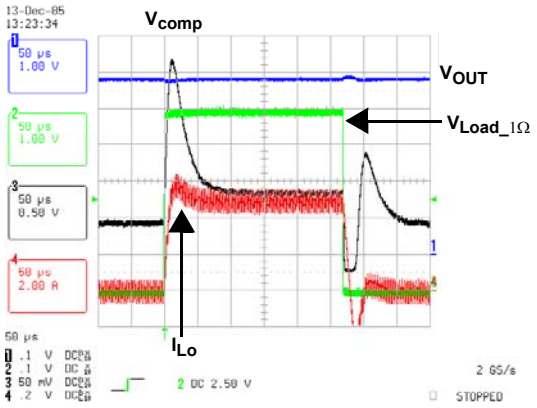

FIGURE 3. TRANSIENT RESPONSE AT 15V V_{IN}

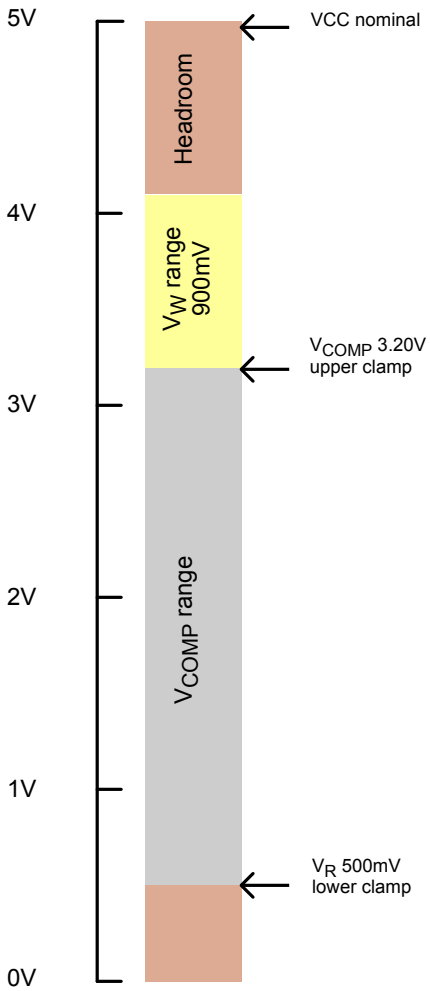

FIGURE 4. V_{COMP} RANGE

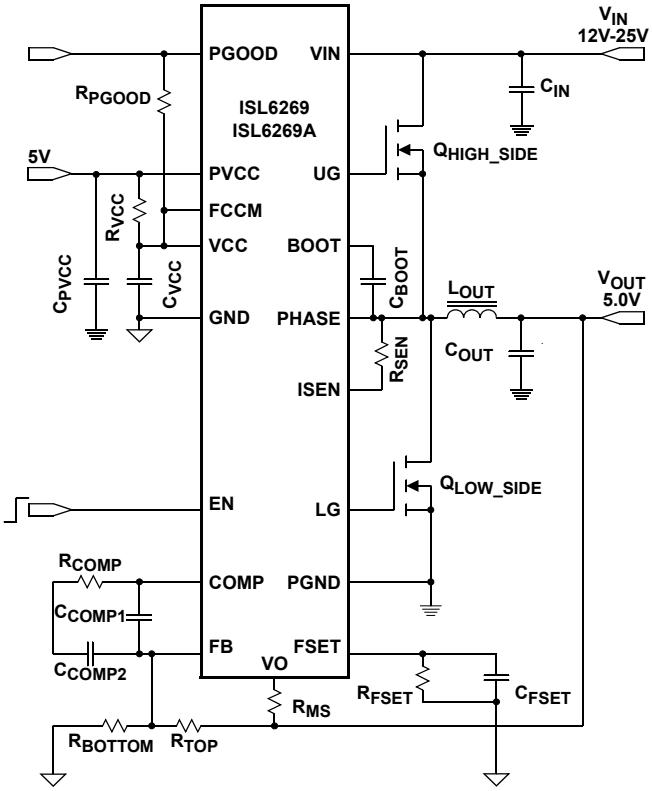

FIGURE 5. SCHEMATIC OF 5V V_{OUT} APPLICATION

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