

PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages

Renesas' Quad Flat No Lead (QFN) package family offering is a relatively new packaging concept that is currently experiencing rapid growth. This package family includes the general version, QFN, as well as thinner versions such as TQFN, UTQFN, and XQFN. The family encompasses lead pitches of 0.4mm and above. A sub-set of the Quad Flat No Lead is the Dual sided type (leads on only 2 of the 4 sides) which includes versions such as the DFN, TDFN, UTDFN, and XDFFN. Within this document, the term QFN represents all family options. This family offers a variety of benefits including reduced lead inductance, a small sized near chip scale footprint, thin profile and low weight. It also uses perimeter I/O pads to ease PCB trace routing, and the exposed copper die-pad technology offers good thermal and electrical performance. These features make the QFN an ideal choice for many new applications where size, weight, and thermal and electrical performance are important.

There are general industry references, such as IPC-SM-782, for printed circuit board (PCB) land pattern design. But because the QFN package style is relatively new, such industry guidelines for it are still in development. This Tech Brief helps by providing general guidelines for use in developing land pattern layouts and solder mounting processes.

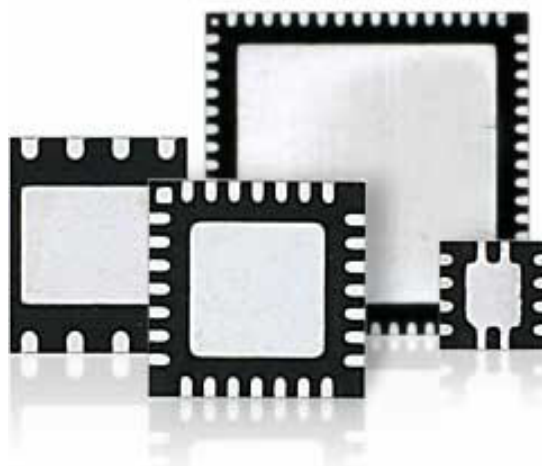


Figure 1. QFN PACKAGES

It should be emphasized that these guidelines are general in nature and should only be considered a starting point in this effort. The user must apply their actual experiences and development efforts to optimize designs and processes for their manufacturing practices and the needs of varying end-use applications.

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1. QFN Package Outline Drawings

Renesas' individual product datasheets reference to the appropriate Renesas package outline drawings. These in turn reference compliance to any applicable industry standard outlines. For QFNs, the JEDEC MO-220 outline series generally applies. The QFN dimensions used in the land pattern design can be taken from these drawings.

2. General Design Guidelines

The die pad and perimeter I/O pads of the QFN are fabricated from a planar copper lead-frame substrate. This is encapsulated in plastic with the bottom of the die pad and I/O pads exposed to create a very small footprint exposed-pad package. Both the I/O pads and die pad should be soldered to the PCB.

The corresponding PCB lands need to be designed to fit well within the PCB assembly process capabilities, as well as promote good long term solder joint reliability. Note that soldering the exposed die pad anchors the package and provides important thermo-mechanical temp cycling stress benefits that improve the reliability of the I/O pad solder joints.

The PCB thermal land design for the exposed die pad should include thermal vias that drop down and connect to buried metal plane(s). This combination of vias for vertical heat escape and buried planes for heat spreading allows the QFN to achieve its full thermal potential.

3. Land Pattern Guidelines

3.1 Peripheral I/O Lands

The I/O lands should be 0.15mm longer than the package I/O pads. Inward corners may be rounded to match the I/O pad shape. The I/O land width should match the package I/O pads width (1:1) see [Figure 2](#). Design dimension guidelines are shown in the individual package outline drawing.

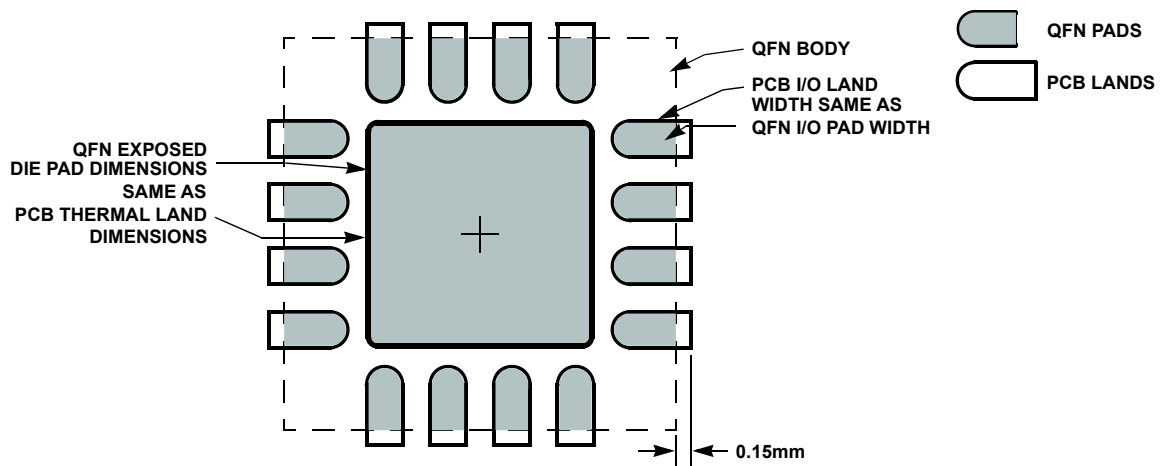


Figure 2. Typical QFN Land Pattern Layout with Package Overlay

3.2 PCB Thermal Land

The thermal land should match 1:1 with the package exposed die pad. See [Figure 2](#).

3.3 Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drop down and connect to buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter, with the barrel plated to about 1.0 ounce copper.

Although adding more vias (such as by decreasing via pitch) will improve thermal performance, diminishing returns will be seen as more and more vias are added. Therefore, simply use as many vias as practical for the thermal land size and your board design ground rules.

4. Solder Mask Design

Two types of land patterns are used for surface mount packages:

- Solder Mask Defined (SMD) – Solder mask openings smaller than metal pads.
- Non-Solder Mask Defined (NSMD) – Solder mask openings larger than metal pads.

Better control of the copper etching process as compared to the solder masking process makes NSMD preferable. Also, the SMD pad definition can introduce stress concentrations near the solder mask overlap region that can result in solder joints cracking under extreme fatigue conditions. Using NSMD instead improves the reliability of solder joints as solder is allowed to wrap around the sides of the metal pads on the board.

For these reasons, NSMD is recommended for the perimeter I/O lands and generally for the thermal land; however SMD should be used on the thermal land when it is relatively large as discussed below.

For NSMD pads, the solder mask opening should be about 120µm to 150µm larger than the pad size, providing a 60µm to 75µm design clearance between the copper pad and solder mask. Rounded portions of package pads should have a matching rounded solder mask-opening shape, especially at corner leads to allow for enough solder mask web to prevent solder bridging.

Typically each pad on the PCB should have its own solder mask opening with a web of solder mask between adjacent pads. However for 0.4mm pitch parts with an I/O land width of about 0.25mm, space may not be available for solder mask web in between the pads. In that case, use one big opening designed around a whole strip of pads (for instance all the pads on one side of a package) with no solder mask in between the pads.

For package designs with exposed die pad sizes near the maximum available for that package, the gap between the thermal land and I/O pads may be small. In this case there may be more potential for solder bridging, so the thermal land should be solder mask defined (SMD). The mask opening should be approximately 100µm smaller than the thermal land on all four sides, which increases the solder mask web between the thermal and I/O lands.

Solder masking is also required for thermal vias to prevent solder wicking inside the vias, drawing solder away from the thermal land-to-die pad interface. The solder mask diameter should be about 100µm larger than the via diameter. The vias can be plugged or tented with solder mask, either from the bottom or top surface of the PCB. Tenting from the top is considered a better option as it results in smaller voids under the die pad. Solder masking of vias from the bottom side can result in increased outgassing during reflow, creating bigger voids around vias. But note that small voids in this area are not unusual and will have little effect on thermal or electrical performance or on the reliability of the perimeter I/O pad solder joints.

5. Stencil Guidelines

5.1 Stencil Design for I/O Lands

Re-flowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2 mil to 3 mil) standoff height. The solder paste stencil design is the first step in developing such optimized, reliable joints.

Stencil aperture size-to-land size should typically be a 1:1 ratio. For finer pitch parts, especially as tight as 0.4mm, the aperture width may need to be reduced slightly to help prevent solder bridging between adjacent I/O lands.

5.2 Stencil Design for Thermal Land

To reduce solder paste volume on the thermal land, it is recommended that an array of smaller apertures be used instead of one large aperture. The smaller apertures can be circular or square and of various dimensions and array sizes; but the main goal should be a dimensional combination that results in 50 to 80% solder paste coverage. This reduced coverage on the thermal land is important in achieving good solder joints and good temperature cycling related reliability at the perimeter I/O lands. Other reasons that the thermal land's solder paste coverage should not be reduced too low are that this could potentially affect the self alignment feature of the package during SMT reflow, and could contribute to increased solder voiding which could affect thermal performance.

5.3 Stencil Type and Thickness

A laser-cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing smooths aperture walls, resulting in reduced surface friction, good paste release and void reduction. Using a trapezoidal section aperture (TSA) promotes paste release and also forms “brick-like” paste deposits that assist in firm component placement.

A 0.125mm stencil thickness is recommended for finer pitch packages (0.5mm and smaller), and this may be increased to 0.15mm to 0.2mm thickness for greater than 0.5mm pitch packages.

6. Solder Paste and Reflow Profile

Due to the low mounted height of the QFN, No Clean Type 3 paste per ANSI/J-STD-005 is recommended. Nitrogen purge is also recommended during reflow.

A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the QFN. The profiles given in [Figure 3](#) and [Table 1](#), [Table 2](#), and [Table 3](#) are provided as guidelines, to be customized for varying manufacturing practices and applications.

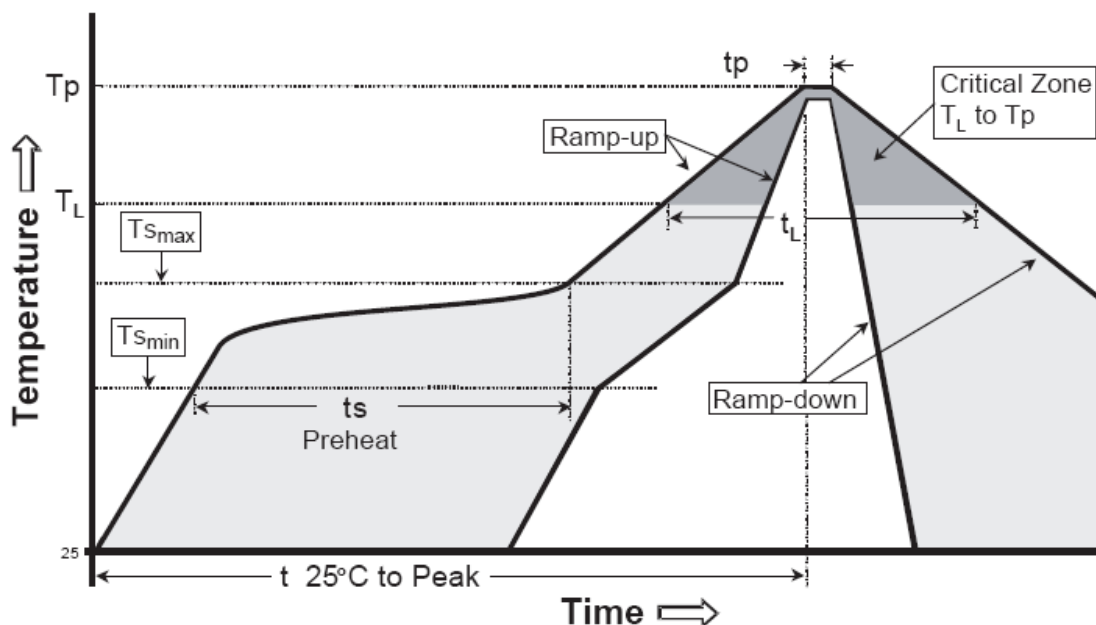


Figure 3. Typical Reflow Profile

Table 1. Package Peak Reflow Temperatures - Sn/Pb

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5mm	240 +0°C/-5°C	225 +0°C/-5°C
≥2.5mm	225 +0°C/-5°C	225 +0°C/-5°C

Table 2. Package Peak Reflow Temperatures - Pb-Free

Package Thickness	Volume mm ³ <350 ^[1]	Volume mm ³ 350 -2000 ^[1]	Volume mm ³ >2000 ^[1]
<1.6mm	260 +0°C	260 +0°C	260 +0°C
1.6mm to 2.5mm	260 +0°C	250 +0°C	245 +0°C
≥2.5mm	250 +0°C	245 +0°C	245 +0°C

1. Tolerance: The device manufacturer/supplier assures process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example, 260°C+0°C at the rated MSL level.

Table 3. Reflow Profile Parameters

Profile Parameter	Sn/Pb	Pb-Free
Average Ramp-Up Rate (Ts _{MAX} to Tp)	3°C/second maximum	3°C/second maximum
Preheat Temperature Min (Ts _{MIN})	+100°C	+150°C
Temperature Max (Ts _{MAX})	+150°C	+200°C
Time (ts _{MIN} to ts _{MAX})	60 to 120 seconds	60 to 180 seconds
Time maintained above: ▪ Temperature (T _L) ▪ Time (t _L)	+183°C 60 to 150 seconds	+217°C 60 to 150 seconds
Peak/Classification Temperature (Tp)	See Table 1	See Table 2
Time within +5°C of Actual Peak Temperature (tp)	10 to 30 seconds	20 to 40 seconds
Ramp-Down Rate	+6°C/second maximum	+6°C/second maximum
Time +25°C to Peak Temperature	6 minutes maximum	8 minutes maximum

7. Solder Joint Criteria

QFN packages feature Bottom Only type terminations as described in Section 7.5.15 of the Joint Industry Standard *IPC/EIA J-Std-001E: Requirements for Soldered Electrical and Electronic Assemblies*. The solder joint requirements for QFN packages are given in Table 4 and Figure 4.

IMPORTANT: The bottom only QFN termination does NOT have ANY requirement for solder joint fillet heights of any kind. Only solder joint length, width and solder joint thickness are specified. As a result, QFN components do not exhibit any toe fillets and are not as easily inspected with a microscope. X-ray inspection, similar to what is done on BGA assemblies, is the preferred inspection technique.

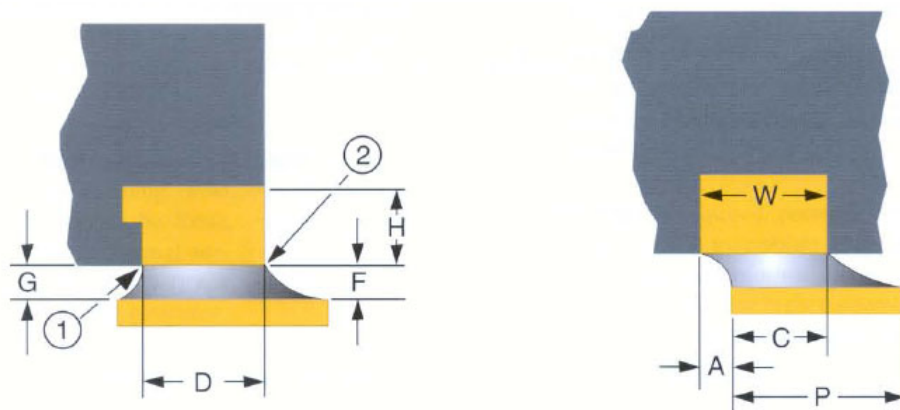


Figure 4. QFN Terminations

Table 4. Dimensional Criteria - QFN

Feature	DIM.	Class 1	Class 2	Class 3
Maximum Side Overhang	A	50% (W)[1]		25% (W)[1]
Toe Overhang (outside edge of component termination)	B	Not Permitted		
Minimum End Joint Width	C	50% (W)	75% (W)	
Minimum Side Joint Length	D	[2]		
Solder Fillet Thickness	G	[3]		
Minimum Toe (End) Fillet Height	F	[4][5]		G + H[4][5]
Termination Height	H	[5]		
Solder Coverage of Thermal Pad		[2]		
Land Width	P	[4]		
Termination Width	W	[4]		

1. Does not violate minimum electrical clearance.
2. Not a visually inspectable attribute.
3. Wetting is evident.
4. Unspecified parameter or variable in size as determined by design.
5. H = height of solderable surface of lead, if present. Some package configurations do not have a continuous solderable surface on the sides and do not require a toe (end) fillet.

8. Maximum Downward Force

The maximum downward force (or continuous force) that is allowed on QFN packages is shown in [Table 5](#).

Table 5. QFN Maximum Downward Force

Package Configuration	Maximum Force (N)
Standard QFN, Multi-chip module QFN and Power QFN.	500
Exposed Si die or exposed heat slug QFN, Multi-chip module QFN and Power QFN.	100

9. Rework Guidelines

After PCB assembly, the package should be inspected in transmission x-ray for the presence of voids, solder balling, or other defects underneath the package. Cross sectioning may also be required to determine the fillet shape and size, and the joint standoff height. In a QFN, only the external side-fillet solder joint is exposed and any retouch is limited to this area. For rework of defects underneath the package, the whole package needs to be removed.

Although the QFNs are small, the removal and rework can be done manually. Removal and rework of QFNs can be a challenge due to their small size and since they are commonly mounted on smaller, thinner, and denser PCBs. The following steps are provided as a guideline – a starting point in developing a successful rework process.

9.1 Bake

Before rework, bake the PCB assembly at +125°C for at least 24 hours to remove any residual moisture.

9.2 Component Removal

Ideally, the reflow profile for part removal should be similar to that of the component attachment. However, the time above liquidus can be reduced as long as the reflow is complete.

It is recommended that the board be heated from the bottom side using convective heaters and from the top side with hot gas nozzle directing heat at the component to be removed. A hot plate set at +235°C to +325°C with the circuit board held in place at approximately 25mm above the hot plate can be used (see [Figure 5](#) and [Figure 6](#)).

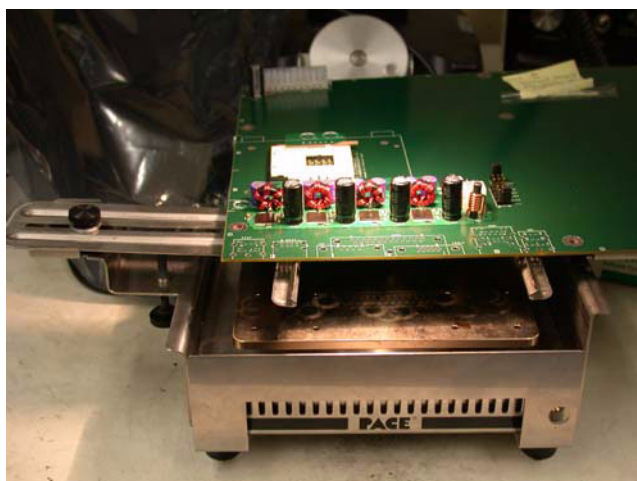


Figure 5. Hot Plate Rework Station

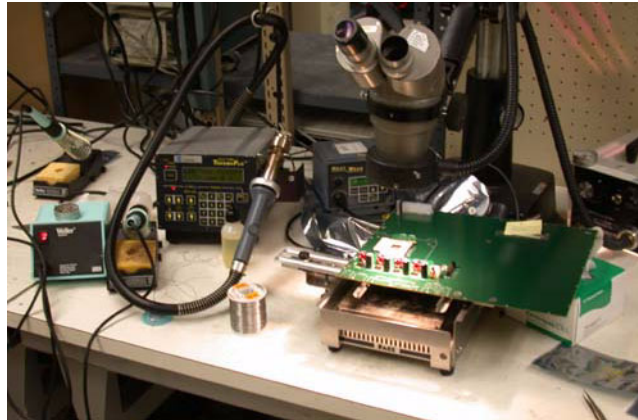


Figure 6. Hot Plate Rework Station Overview

The circuit board/component being removed should reach at least $55^{\circ}\text{C} \pm 5^{\circ}\text{C}$ using a temperature ramp of 1°C to $3^{\circ}\text{C}/\text{min}$ before applying the hot gas. The hot gas temperature can be approximately 425°C . At the discretion of the operator, the visible peripheral solder joints may or may not be wicked off using a solder braid. The hot gas can be applied with the nozzle tip approximately 15mm to 25mm away (see [Figure 7](#)) from the component in a circular motion to bring the component and underlying solder to reflow temperature.

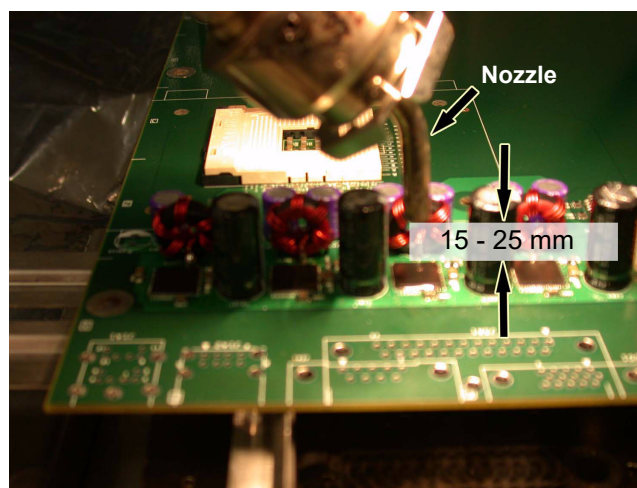


Figure 7. Hot Gas Nozzle Proximity

As reflow temp is approached it is sometimes useful to apply the heat edge on to the component to try and get the heat to go under the package to reflow the large thermal land. It is also helpful to wedge a tweezer tip under a corner of the QFN and supply a slight upward prying force (see [Figure 8](#)) so when the thermal land begins to flow the component lifts up.

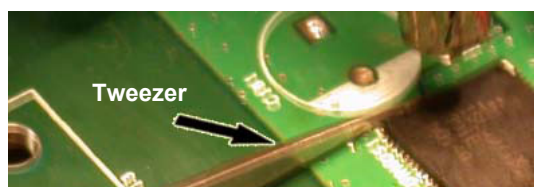


Figure 8. Tweezer Tip Upward Force

Heating of adjacent components should be minimized. QFNs are small and light so avoid excessive flow.

When the joints have reflowed, remove the QFN with a vacuum pick up or tweezer. Because of the small package size, vacuum pressure should be kept below 15" of Hg to prevent premature board/land lift (see [Figure 9](#)) before all joints have fully reflowed.

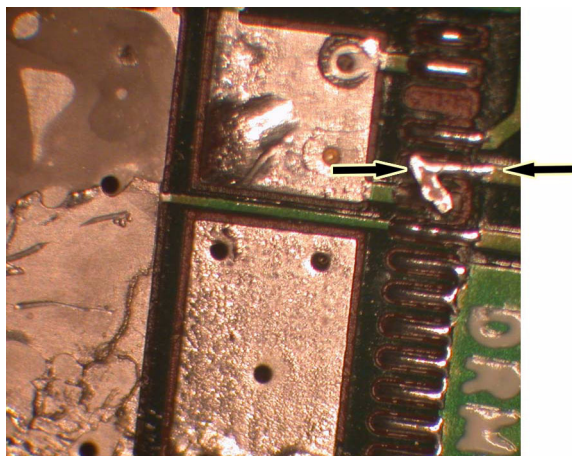


Figure 9. Example of Board Land Lift

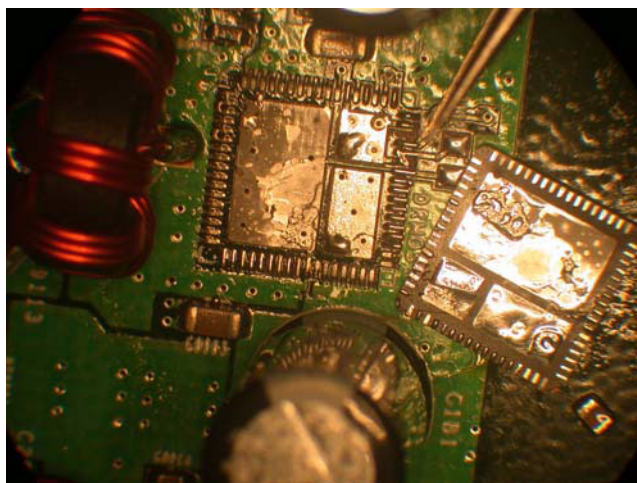


Figure 10. Component Lifted Off/Removed

9.3 Site Redress

Clean the site properly, removing residual solder with a combination of a blade-style conductive tool and/or desoldering braid (see Figure Figure 11). After residual solder removal clean the lands with a solvent specific to the type of paste used in the original assembly (see Figure 12).

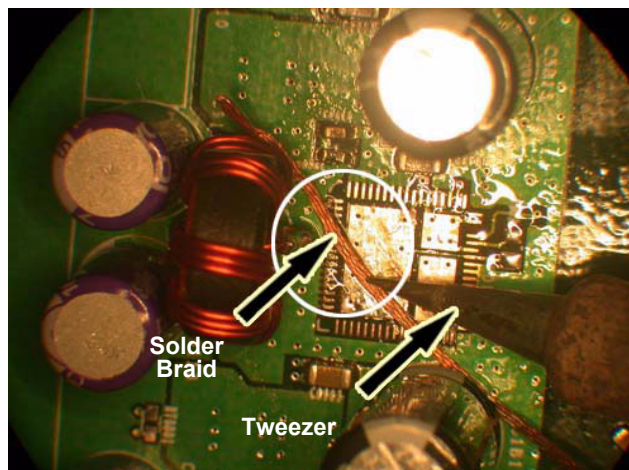


Figure 11. Site Redress Using Solder Braid

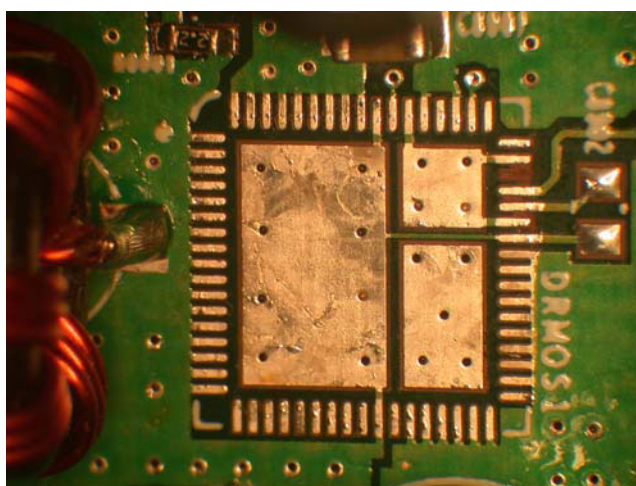


Figure 12. Finished Site Redress

9.4 Solder Paste Printing

Use a miniature stencil specific to the component and align the stencil aperture under appropriate magnification (~50 to 100X). Lower the stencil onto the PCB and deposit the paste with a small squeegee blade. The blade width should be the same as the package width to ensure single pass paste deposition, avoiding any overprinting.

9.5 Component Placement and Reflow

Due to its small mass, the QFN has good self-centering abilities during solder reflow, so the placement of this package should be similar to that of BGAs. The placement machine should have fine adjustment capability in the x, y, and rotational axes. Because the pads are on the underside of the package, use an optical system that can overlay an image of the solder paste pattern to aid in component alignment, which should be done at 50 to 100X magnification. Reflow the PCB using the same profile as that developed for the initial attachment.

9.6 Manual Alternative to Solder Paste Printing/Component Placement and Reflow

In cases where no mini stencil exists or where the PCB density is too great to allow paste stencil, the following manual technique can be employed.

First measure and record the thickness of the replacement QFN using a caliper. Be sure to measure the thickness from the top plane of the package to the bottom plane of the package that contains the large center thermal land (see [Figure 13](#)). This measurement is used later in this procedure.

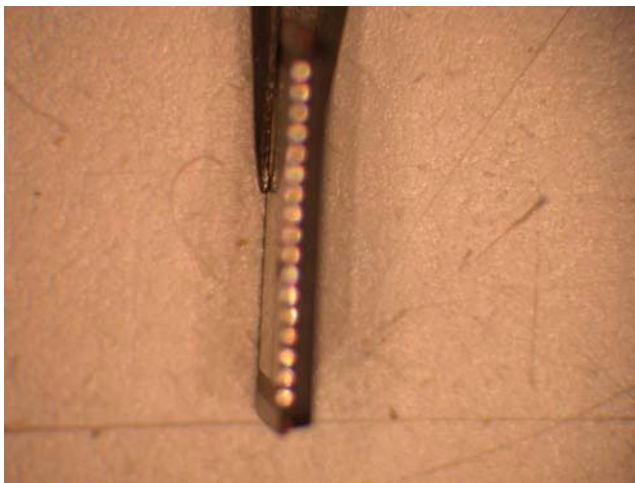


Figure 13. Caliper Thickness Measurement of Replacement QFN

Second, tin the large center thermal land on the bottom of the replacement component using a hot iron with a tip temp of approximately 370°C. This is done by first tinning the iron tip with solder. Then liberally apply liquid flux to the component center thermal land and “dab” the tinned iron tip onto the large thermal land of the component in a tapping type motion (see [Figure 14](#) and [Figure 15](#)).

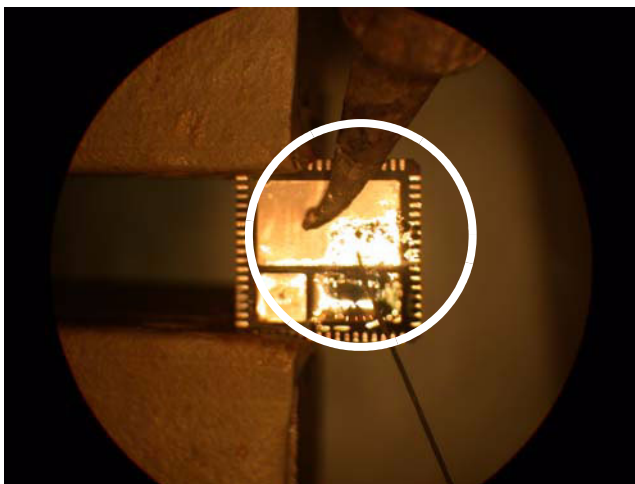


Figure 14. Tinning of Thermal Land on QFN (25% Complete)

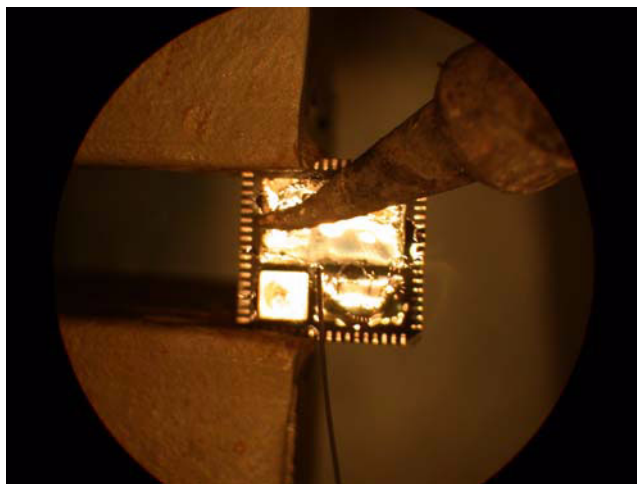


Figure 15. Tinning of Thermal Land on QFN (90% Complete)

Do not apply and hold the iron tip to the thermal land. As this tapping motion continues, observe the flux begin to boil and watch for the solder to wick out and wet onto the large center thermal land of the component.

The wetted thermal land resembles a pillow with the solder mounded up in the center of the land and wetting out to the edges of the land (see [Figure 16](#) and [Figure 17](#)).

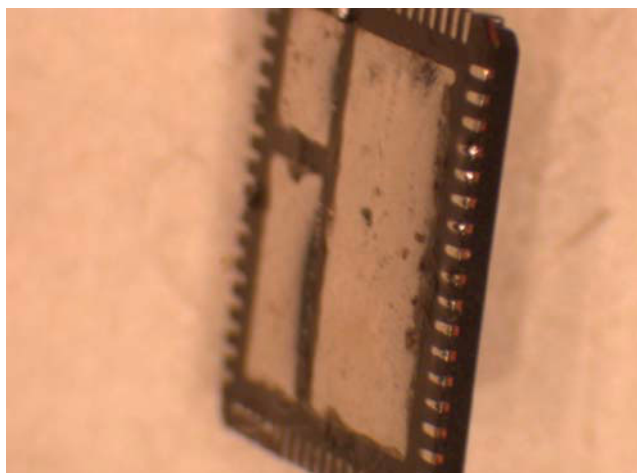


Figure 16. Finished Tinned Thermal Land on QFN



Figure 17. Finished Tinned Thermal Land on QFN

Clean off the flux residue from the component. Check the thickness of the now tinned package from the top of the package to the top of the solder pillow (thickest point) on the tinned bottom center thermal pad and compare it to measurement that was taken before the replacement component was tinned. The target is to apply 0.1mm to 0.35mm of solder to the center thermal land as measured at the thickest point.

If required, re-apply some fresh liquid flux and wick off some of the wetted solder on the large thermal land using a solder braid and then reflow the remaining solder on the land using the tapping motion mentioned above to create a slightly thinner pillow.

Repeat tinning and braiding as required to ensure proper thickness. It is important not to have too much solder on the center thermal land of the component in order to avoid bridging during component replacement on the board. It is better to have less than more. When the appropriate solder thickness has been acquired on the large center land on the bottom of the QFN, wick off any excess solder/bridging that may have occurred on any of the peripheral lead terminations on the QFN.

Third, apply some flux onto the large redressed board land that will accept the newly tinned large center thermal land on the component. Be sure to properly orient the component on the board and identify the pin 1 location. Under a microscope at magnification sufficient to see the entire component, place the newly tinned replacement component onto the board and align/center the component as best you can. You will feel the component rock or teeter totter due to the tinned center land on the bottom of the component. This is normal. Holding the component in place with tweezers and light downward pressure, apply heat from the hot gas nozzle as described previously until the solder on the large thermal pad under the component reflows (see [Figure 18](#)).

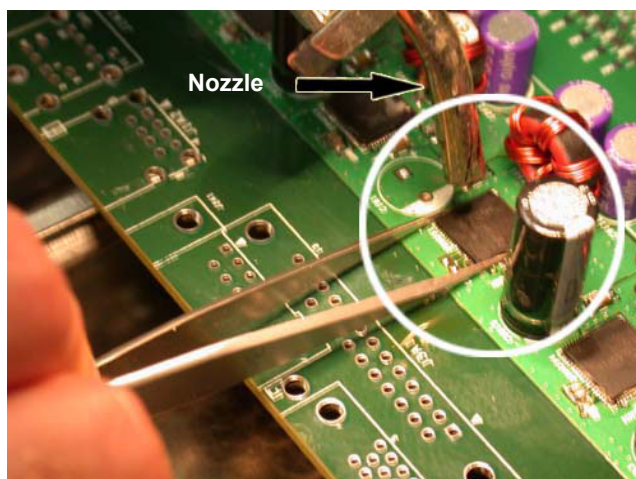


Figure 18. Component Replacement

You will feel the component drop when the large thermal pad reflows and solders the thermal land onto the circuit board. Remove the hot gas. The component is now in place. Clean off the flux residue and inspect for flatness and component termination/board land alignment. Apply fresh flux and reflow/adjust alignment as required using tweezers/probe and hot gas nozzle. Clean off flux residue.

Fourth, apply fresh flux to the circuit board lands around the periphery of the QFN terminations. Using a tinned hot iron, individually solder each board land/QFN termination solder joint (see [Figure 19](#)).

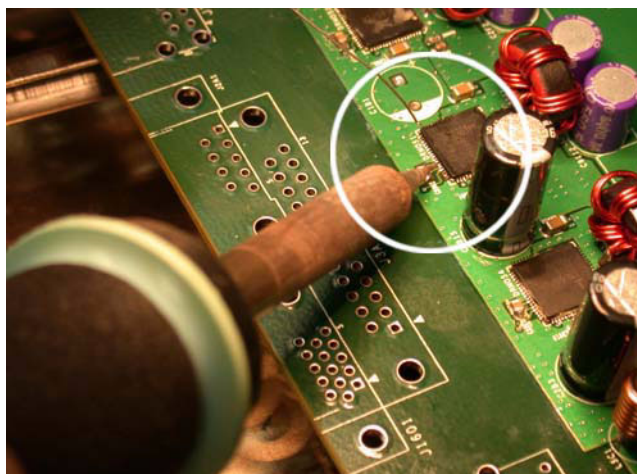


Figure 19. Individual Solder Joint Rework One by One

It is useful to tin the solder iron such that the solder to be used to form the board land/QFN termination solder joint is supplied from the solder iron tip as you first touch the QFN termination and then draw the solder down to the board land. Skilled operators sculpt a solder fillet to improve ease of post soldering visual inspection. This fillet makes visual inspection easier but is not required to produce a reliable solder joint. Clean off flux residue. Submit for inspection (see [Figure 20](#)).

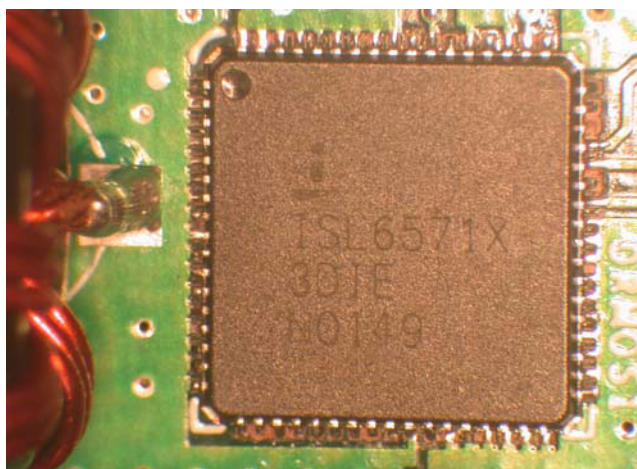


Figure 20. Finished QFN Component Replacement

10. Revision History

Revision	Date	Description
8.03	Mar 7, 2024	Updated the maximum force values in Table 5.
8.02	Jun 21, 2023	Updated Peripheral I/O Lands section changed 0.2mm to 0.15mm.
8.01	Jan 19, 2023	Applied new template. Added Maximum Downward Force section. Added Revision History section.

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