

Introduction

The Intersil HSP48908 2-D convolver has gained acceptance among customers as an excellent choice for implementing 8-bit 3x3 convolutional kernels. However, new applications in image processing, such as digital video broadcasting and medical imaging, demand higher bit resolutions. This technical brief shows how to implement a 3x3 10-bit kernel using the Intersil HSP43168 (Dual FIR Filter) and HSP9501 (Delay Buffer). This technique is also applicable, with appropriate modifications, to convolutions requiring greater than 10-bit resolution.

3x3 10-Bit Kernel

Figure 1 shows the block diagram of the 3x3 10-bit convolutional kernel. Use is made of two HSP43168s and two HSP9501s. This configuration will operate up to clock speeds of 32MHz.

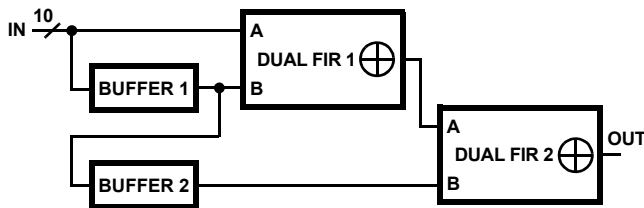


FIGURE 1. BLOCK DIAGRAM OF 3x3 10-BIT CONVOLUTIONAL KERNEL

Theory of Operation

A 3x3 convolution is implemented as the sum of three row vector dot products. Dual FIR 1 implements the top two row vector dot products and Dual FIR 2 implements the bottom row vector dot product. The convolution sum is facilitated via the A input of Dual FIR 2 and is available at the output of Dual FIR 2.

The row vector coefficients are programmed as the first 3 coefficients of Dual FIR 1 A and B and Dual FIR 2 B. The first coefficient of Dual FIR 2 A has a value of 1.0 with all other coefficients set to zero. Both dual FIRs have the output programmed to A + B (i.e. MUX1-0 is equal to 01).

Row buffer 1 is programmed for a length commensurate with the image row pixel length (e.g. 1024 pixels) while buffer 2 is programmed for the image row pixel length plus five additional delays. These five additional delays are needed to compensate for the pipeline delay associated with Dual FIR 1 (e.g. 1024 + 5 = 1029).

Because of the rounding feature in both dual FIRs, there is no need for shifting the MSB position at the output. The appropriate rounding value is programmed into control address 001H, bits 8-5, and is easily derived.

Summary

A solution is presented for implementing a 3x3 10-bit convolutional kernel which makes use of two HSP43168 dual FIRs, programmed for A + B output, and two HSP9501 row buffers. Dual FIR 1 A and B, in conjunction with Dual FIR 2 B, implement the row vector dot products, while Dual FIR 2 A provides a path for summing the three dot products to obtain the convolution sum.

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Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852-2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338