The NCO as a Stable, Accurate Synthesizer

Low Jitter Frequency Reference

In communication and other circuits, it is often necessary to produce an accurate reference signal whose frequency and phase can be precisely controlled in real time. The Numerically Controlled Oscillator (NCO) is ideally suited for this purpose. For some applications, the output reference signal is a square wave, so the temptation is to use only the MSB of the NCO output. This is useful in low frequency applications such as motor controllers, but is inadequate for most communications tasks. This is because the zero crossings of this signal can vary by one period of the input clock from one pulse to the next, which creates an unacceptable amount of jitter in the output. For example, if the NCO is clocked at 30MHz, the jitter is 33ns. For a 1MHz square wave, this results in 12° of phase jitter. The straightforward solution is to use an NCO with a much higher clock rate. This is not cost effective for applications requiring phase jitter of less than 5ns, however, since it requires a sample rate of 200 Mega Samples Per Second (MSPS), which drives the user to an ECL NCO.

A much less costly circuit which solves this problem is shown in Figure 1. The output of the comparator is a square wave with much less jitter than the NCO alone. The basic idea is that the sampled sine wave output of the NCO is converted to a smooth sine wave, which is converted back to a square wave with a comparator. In the circuit shown, the comparator drives a filter, which attenuates the odd order harmonics so that the final output of the circuit is a sine wave. The upper limit on the purity of the sine wave is also much better than that of the NCO, as will be seen below.
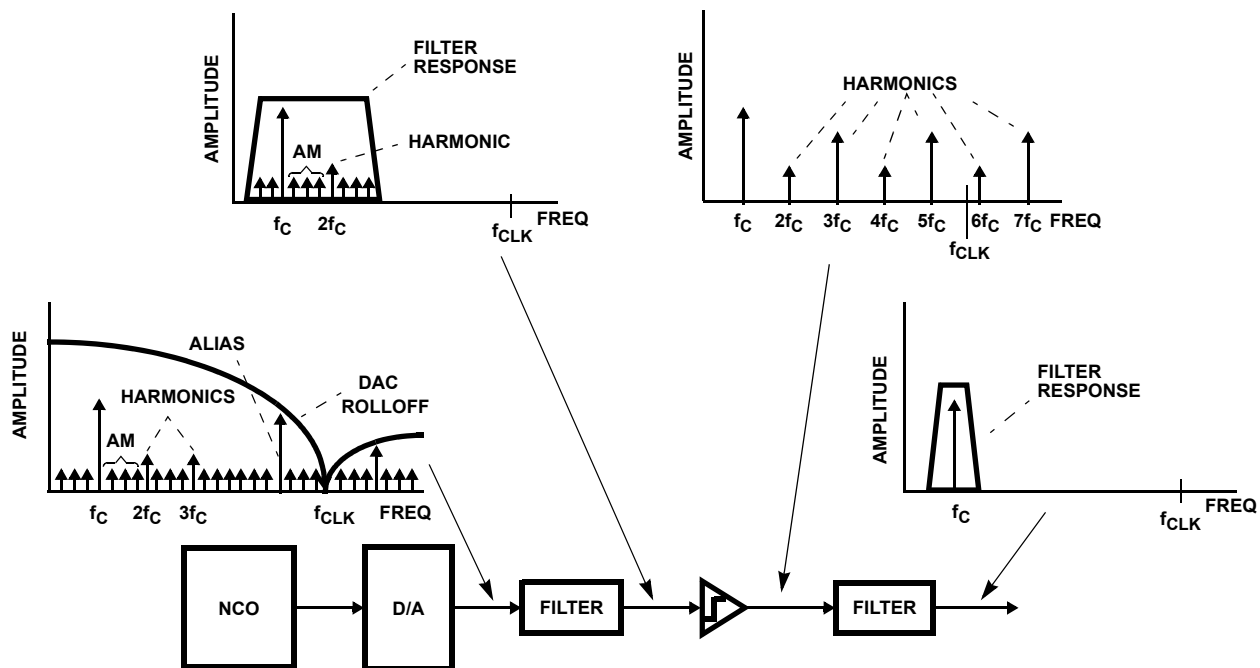

FIGURE 1. MINIMUM SPUR CIRCUIT

The primary sources of error in this circuit are:

In the NCO, spurs are classified as either AM or PM. PM spurs are due to truncation of the phase in calculating the sine and cosine. If M = number of bits into the input of the Sine/Cosine Generator, the PM spur level is -6M + 5.17dB[1]. The AM spurs are due to amplitude quantization on the output of the NCO. If the number of NCO output bits is N, the AM spur level is approximately equal to -6.02N - 1.76dB. [1] There will also be jitter due to the clock oscillator driving the NCO, but since it is only the short term jitter, not the long term stability of the oscillator that contributes to phase noise, this will be negligible if a reasonably good oscillator is used.

The DAC introduces additional spurs which come from three sources: Intermodulation spurs due to nonlinearities in the DAC; a spur at the clock oscillator frequency due to clock feed-through; and power supply noise. The DAC also faithfully reproduces the aliases and harmonics that are unavoidable products of the NCO due to the digital nature of the output.

The bandpass filter on the output of the DAC eliminates the clock feedthrough, aliases due to the sampled nature of the NCO output and most of the AM spurs. Spurs within the pass band are unchanged. The spectrum of the DAC output is a tone surrounded by spurs and noise in the frequency band corresponding to the pass band of the filter with negligible noise elsewhere. The area comprised of the tone, spurs and noise is known as the pedestal.

The input of the comparator is a relatively clean sine wave which the comparator converts into a square wave. This limiting action eliminates the AM spurs but has no effect on the PM spurs. For this reason, the number of bits used on the output of the NCO and the input of the DAC has little measurable effect on the output. The primary contributions to errors on the output of the comparator are the PM spurs on its input, which are passed through relatively unaffected, and power supply noise, which is attenuated by the power supply rejection of the comparator. If the filter on the input of the comparator did not remove the aliases and clock feed through, then the comparator will generate intermodulation components. This makes a good filter and a careful frequency plan essential.

If the desired output of the circuit is a sine wave rather than a square wave, the output of the comparator is filtered to extract the fundamental - that is, to suppress the odd order harmonics of the square wave signal. Note that this signal is much cleaner than the output of the first filter, since the comparator has removed the AM spurs.

The circuit shown here is often used to generate the reference tone for an indirect loop PLL synthesizer. In this case, the output of this circuit is fed into one input of a mixer, with the other input of the mixer driven by a high frequency VCO. The output of the mixer is a high frequency tone. The phase noise at the output of the mixer due to the noise in the reference circuit will be equal to the spur level of the reference circuit plus 20*log10(output frequency/NCO frequency). For example, using the 45106 as a 5MHz reference for a 1GHz synthesizer, the spurs on the output of the reference would increase by 20log10(200), so the output spur level would be -114 + 46 = -68dBc at 1GHz. The NCO frequency resolution is 0.008Hz at 33 MSPS, so the tuning resolution of the synthesizer is 200(0.008) = 1.6Hz. Finer resolution can be obtained by cascading the Time Accumulator with the Phase Accumulator. (See below).

Extended Frequency Resolution

The phase accumulator of the HSP45106 (NCO16) is 32 bits wide. This corresponds to a frequency resolution of (Sample Frequency)/2^{32}. For a 25 MSPS sample rate, this results in an output frequency resolution of 0.006Hz. In certain applications, there is a requirement for much greater resolution. The NCO16 can address these applications using the Time Accumulator as an extension of the Phase Accumulator. Frequency resolutions of up to 64 bits can be obtained in this configuration. Using the previous example of a 25MHz clock, the frequency resolution is 25MHz/2^{64} = 1.35pHz. Using the parts in this configuration requires a small change to the external control logic: The Timer Accumulator Register must be loaded over the control bus interface. This mode of operation has no effect on any of the other performance parameters, such as spurious free dynamic range, phase resolution, etc.

To configure the HSP45106 for this application, the setup shown in Figure 2. Note that the Timer Accumulator output, $\overline{\text{TICO}}$, is connected to the Phase Accumulator input, $\overline{\text{PACI}}$. To set the output frequency of the part, the Center Frequency Register and the Timer Accumulator must be loaded. Assuming that the Offset Register is not used, the equation for calculating the output frequency is now:

Center Frequency = f_{CLK} x (Center Frequency Register /2^{32})

+ (Timer Accumulator Register / 2^{64})

In this equation, the contents of the value in the Center Frequency Register is a two's complement number, meaning that the part tunes from -(CLK Frequency) / 2 to +(CLK Frequency) / 2. The value in the Timer Accumulator is an unsigned number. It is unsigned because it provides the carry in to the Phase Accumulator, which is always added to the LSB of the current phase value.
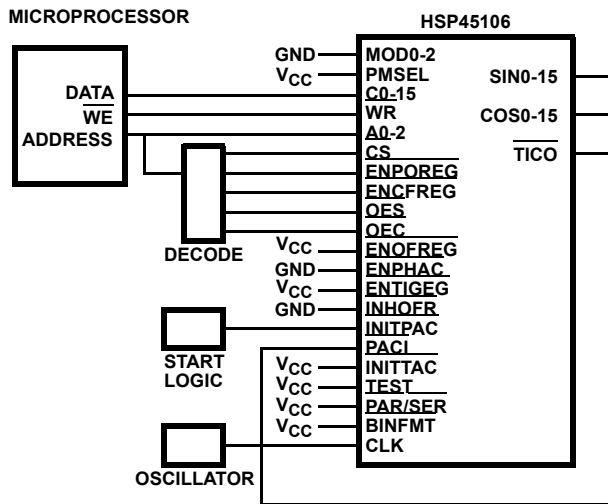
FIGURE 2. EXTENDED FREQUENCY RESOLUTION CIRCUIT

The user should note that there is a flip flop between the Time Accumulator carry out and the $\overline{\text{TICO}}$ pin, and another flip flop between the $\overline{\text{PACI}}$ pin and the Phase Accumulator carry input. This will cause a two clock cycle delay between the carry out of the timer into the carry in of the accumulator. This will only have an effect on the output when the frequency register is updated; in effect, the Time Accumulator lags the Phase Accumulator by two clock cycles. If this is a concern, this can be compensated for by loading the input registers for both accumulators, then toggling $\overline{\text{ENTIREG}}$ two clock cycles before $\overline{\text{ENCFREG}}$.

While the internal architecture of the HSP45116 NCOM and the HSP45106 NCO16 are very similar, this application works better with the NCO16 for two reasons. The first is that on the NCO16, the timer is loaded using a unique pin, rather than sharing this function with the ROM bypass line. This means that the output of the NCO16 is always valid, instead of having erroneous results on the output whenever the timer is updated. The second is that with the NCO16, the data for the various registers is downloaded into separate input registers, which can be downloaded into the operating registers with the $\overline{\text{ENXXREG}}$ pulses. With the NCOM, there is only one 32 bit input register, which must be downloaded into the appropriate operating register before the next value can be input into the part. In this application, it means that the user can adjust the phase between the register updates with the NCO16 but not with the NCOM.

Example

The circuit used to verify this equation is shown in Figure 2. The clock oscillator frequency was measured at 25.24102MHz. In order to achieve an output frequency of 1.000000Hz, the center frequency was set to hexadecimal AA, the offset frequency set to 0, and the Timer Accumulator set to hexadecimal 28880000. A frequency counter was attached to bit 15 of the cosine output. The actual frequency out varied from 0.9999999 to 1.0000003 as the oscillator drifted with time. A more stable oscillator would yield more predictable results. Note that going through the calculations results in an output frequency of 1.0000006Hz. The difference is due to the fact that the oscillator frequency measurement was only carried out to 7 digits, but the counter used in this example had 8 digits.

References

For Intersil documents available on the internet, see web site http://www.intersil.com.

Cercas, Francisco A. B., Tomlinson, M and Albuquerque, A. A. Designing with Digital Frequency Synthesizers, Proceedings of RF Expo East, 1990

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