Using the HDF Bypass of the HSP43220

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When operated in the High Decimating Filter (HDF) bypass mode, the HSP43220 Decimating Digital Filter (DDF) requires clock timing relationships that are different from the normal operation configurations.

Normal Operation

Figure 1 illustrates the timing relationship between CLK_IN, CK_DEC and FIR_CK with the HDF configured for a decimation of 2. This is considered a “normal” operation mode.

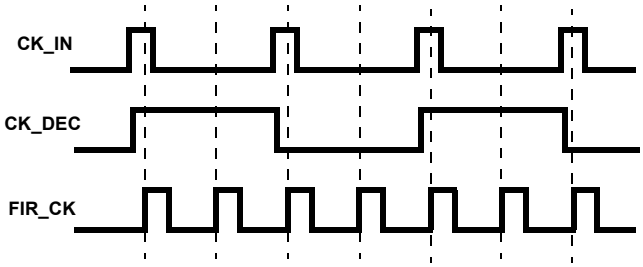

FIGURE 1. CIRCUIT TIMING WHEN H_D = 2

The frequency of the CK_IN signal is divided down by the HDF decimation counter to output CK_DEC, which is at the decimated rate. The rising edge of the CK_DEC is synchronized with FIR_CLK and indicates that new data is ready at the output of the HDF, for use in the FIR filter. Figure 2 illustrates the block diagram implementation of this control signal.

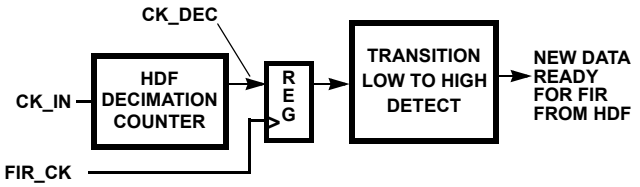

FIGURE 2. CK_DEC GENERATION AND DETECTION

There are two timing considerations that must be considered for normal operation:

1. $FIR\_CK \geq CK\_IN[(TAPS/2) + 4 + F_{DEC}]/[H_{DEC}F_{DEC}$
2. $CK\_IN/H_{DEC} \leq 4MHz$

HDF Bypass Operation

Figure 3 shows the detailed timing relationship between FIR_CLK and CK_IN required for the HDF bypass configuration. The HDF Section can be set for bypass operation (no decimation; H_D = 1) by either setting the H_BYP bit to 1 or by setting H_DRATE = 0. Six timing specifications apply in the HDF bypass mode. For the 33MHz version of the part, the value of these parameters are:

Clock Pulse Width High -

t_{SPWH} . . . . . 13ns minimum

Clock Skew Between CK_IN and FIR_CLK -

t_{SK} . . . . . $[t_{FIR}-15]$ ns maximum

CK_IN Setup To FIR_CLK -

t_{CIS} . . . . . 17ns minimum

CKIN Hold From FIR_CLK -

t_{CIH} . . . . . 2ns minimum

CK_IN Pulse Width Low -

t_{CH1L} . . . . . 19ns minimum

CK_IN Pulse Width High -

t_{CH1H} . . . . . 19ns minimum

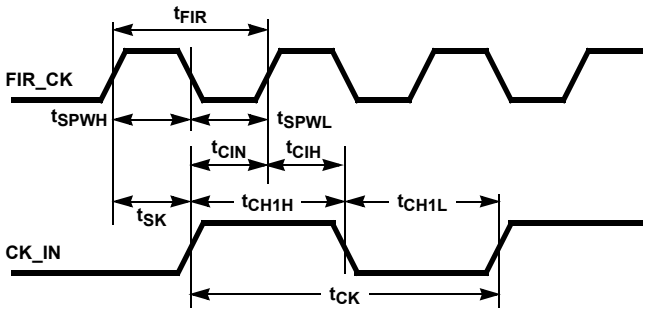

FIGURE 3. “NORMAL” OPERATION TIMING RELATIONSHIPS

Failure to meet the timing requirements on CK_IN when H_D = 1, results in either erratic or no DATA_RDY pulses being issued.

Proper operation when H_D = 1, requires two conditions:

1. **The FIR_CK should be at least 2 times the frequency of CK_IN.**
2. **FIR_CK must also be synchronous to, and obey the setup and hold timing constraints with CK_IN.**

Refer to the AC timing requirements table in the data sheet for values for t_{CIS} and t_{CIH}.

Ensuring that the CK_DEC signal is sampled in both its high and low state by the flipflop requires careful control of CK_IN. The most obvious solution is for the high or low time of CK_IN to be a minimum of one period of FIR_CK. This guarantees sampling both a 1 and a 0, no matter what the phase relation of FIR_CK and CK_IN is. Examples of timing that meet this condition are shown in Figures 5 and 6.

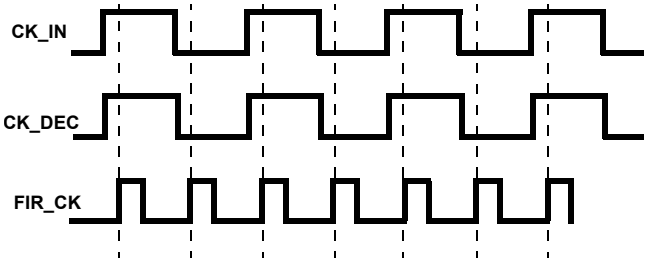

FIGURE 4. CIRCUIT TIMING - PROPER OPERATION (H_D = 1) WITH 50% DUTY CYCLE AND CK_IN FIR_CK/2

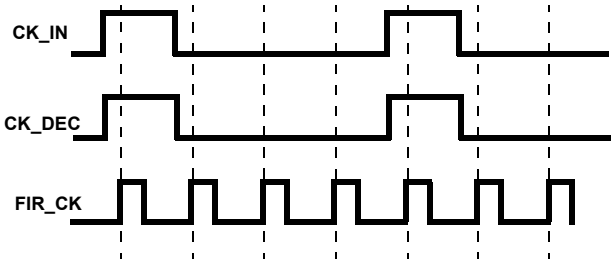

FIGURE 5. CIRCUIT TIMING - PROPER OPERATION (H_D = 1) WITH <50% DUTY CYCLE AND CK_IN ≤ FIR_CK/2

For applications where setting the period of CK_IN fixed is not desirable, there is a specified range of allowed phase offset between FIR_CK and CK_IN in which the filter will operate in the HDF bypass mode. These are given in the AC Specifications. For the 33MHz speed version of the part, the parameters are:

CK_IN Setup To FIR_CLK -

t_{CIS} . . . . . 17ns minimum

CKIN Hold From FIR_CLK -

t_{CIH} . . . . . 2ns minimum

CK_IN Pulse Width Low -

t_{CH1L} . . . . . .19ns minimum

CK_IN Pulse Width High -

t_{CH1H} . . . . . .19ns minimum

The phase difference between FIR_CK and CK_IN is defined as the clock skew, or t_{SK}. Using the t_{SK} specification and a 2ns margin, the minimum CK_IN high or low times with setup and hold can be derived. These are shown in Figure 6.

For the 33MHz part, the minimum CK_IN high or low time requirement is 19ns (when H_D = 1) given the above timing (independent of clock frequencies).

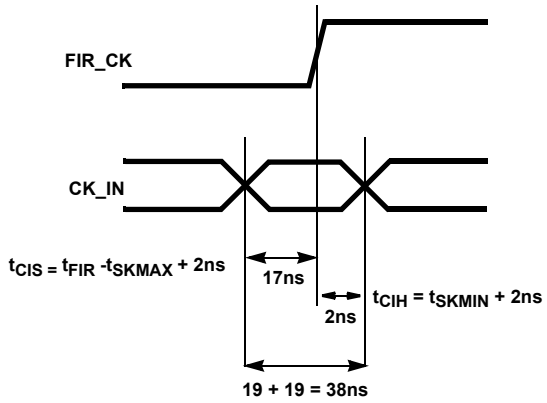

FIGURE 6.

Summary for HDF Bypass Operation

For the typical user, setting the CK_IN high and low times greater than or equal to the period of FIR_CK will be the most desirable solution in terms of hardware.

For the user with additional system constraints, such as those that vary the frequency of CK_IN, but hold constant the high or low time, the above timing yields the most flexible solution.

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